FAIRCHILD SEMICONDUCTOR™

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74FR573
Octal D-Type Latch with 3-STATE Outputs

General Description

The 74FR573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 74F573.

Features

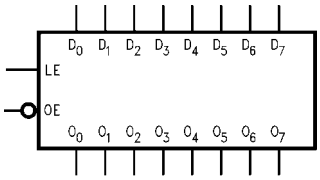
- Broadside pinout aids in PC layout
- Functionally identical to the 74F373, 74F573
- Outputs have current sourcing capability of 15 mA and current sinking capability of 64 mA
- Guaranteed pin-to-pin skew

Ordering Code:

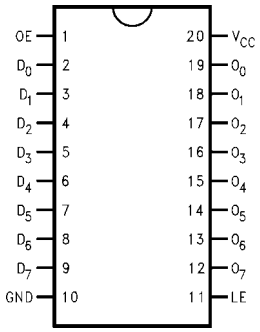
Order Number	Package Number	Package Description
74FR573SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74FR573PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active-LOW)
LE	Latch Enable Input (Active-HIGH)
D_0–D_7	Data Inputs
O_0–O_7	3-STATE Latch Outputs

Functional Description

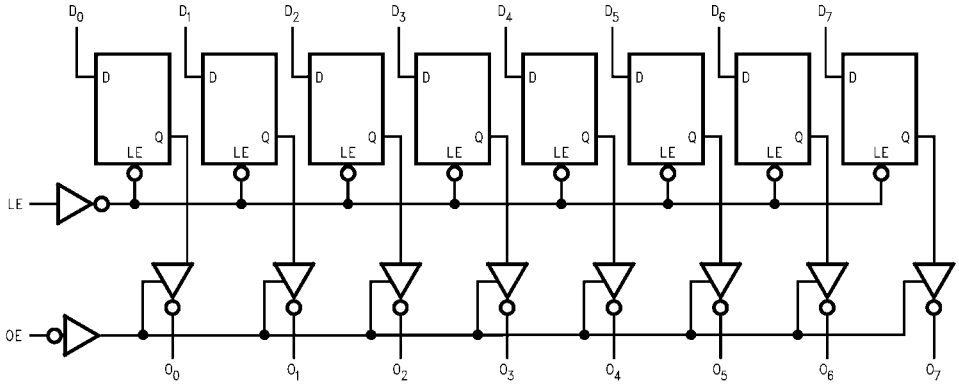
The 74FR573 contains eight D-type latches with 3-STATE output buffers. When the latch enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode, but this does not interfere with entering new data into the latches.

Function Table

Inputs			Output
$\overline{OE}$	LE	D_n	O_n
L	H	H	H
L	H	L	L
L	L	X	O_{n-1}
H	X	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to 125°C
Junction Temperature under Bias	−55° to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5 to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to 5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	2.4			V	Min	I_{OH} = −3 mA
	Voltage	2.0			V	Min	I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{IOL} = 64 mA
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−150	µA	Max	V_{IN} = 0.5V Data Inputs
				−100	µA	Max	V_{IN} = 0.5V Control Inputs
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Current			3.75	µA	0.0	μA_{IOD} = 150 mV, All Other Pins Grounded
I_{OZH}	Output Leakage Current			20	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test			100	µA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		26	32	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current		55	65	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current		32	40	mA	Max	Outputs 3-STATED
C_{IN}	Input Capacitance		8.0		pF	5.0	

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.7	2.9	4.5	1.7	4.5	ns
t_{PHL}	D_n to O_n	1.7	2.6	4.5	1.7	4.5	
t_{PLH}	Propagation Delay	2.6	6.0	8.5	2.6	8.5	ns
t_{PHL}	LE to O_n	2.6	4.3	8.5	2.6	8.5	
t_{PZH}	Output Enable Time	2.8	4.0	7.4	2.8	7.4	ns
t_{PZL}		2.8	5.0	7.4	2.8	7.4	
t_{PHZ}	Output Disable Time	2.2	4.0	6.3	2.2	6.3	ns
t_{PLZ}		2.2	3.5	6.3	2.2	6.3	

AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	1.0	–0.4		1.0		ns
$t_S(L)$	D_n to LE	1.0	–0.7		1.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.5	0.9		2.5		ns
$t_H(L)$	D_n to LE	2.5	0.6		2.5		
$t_W(H)$	LE Pulse Width HIGH	5.0	2.7		5.0		ns

Extended AC Electrical Characteristics

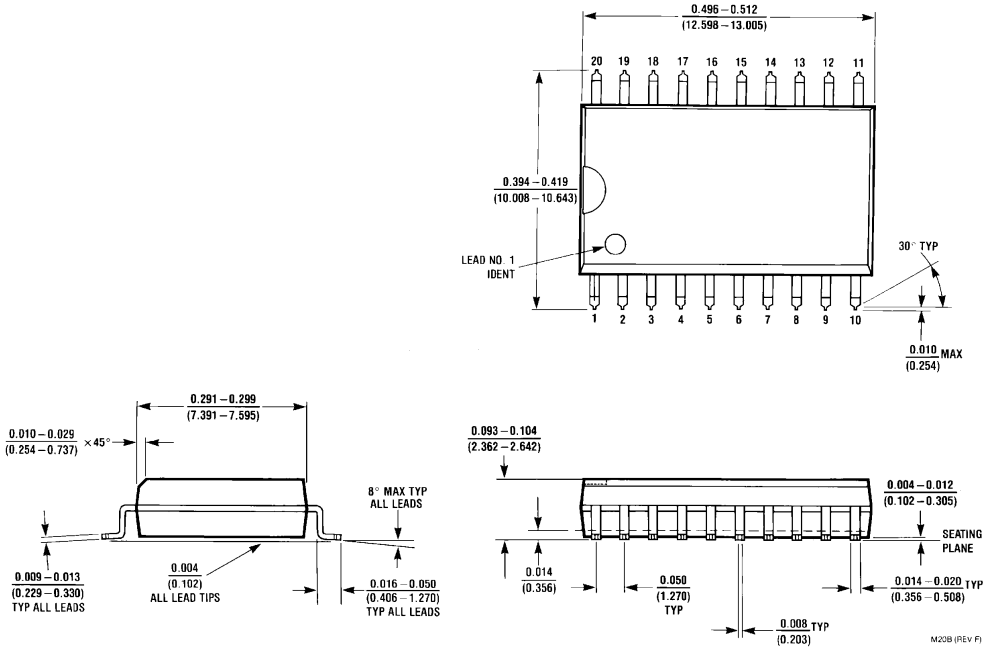
Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, Eight Outputs Switching (Note 3)		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 250$ pF (Note 4)		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.7	5.7	3.4	8.1	ns
t_{PHL}	D_n to O_n	1.7	5.7	3.4	8.1	
t_{PLH}	Propagation Delay	2.6	9.8	4.5	12.3	ns
t_{PHL}	LE to O_n	2.6	9.8	4.5	12.3	
t_{PZH}	Output Enable Time	2.8	9.6			ns
t_{PZL}		2.8	9.6			
t_{PHZ}	Output Disable Time	2.2	7.3			ns
t_{PLZ}		2.2	7.3			
t_{OSHL} (Note 5)	Pin-to-Pin Skew for HL Transitions		1.3			ns
t_{OSLH} (Note 5)	Pin-to-Pin Skew for LH Transitions		1.3			ns
t_{OST} (Note 5)	Pin-to-Pin Skew for HL/LH Transitions		3.0			ns

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e. all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

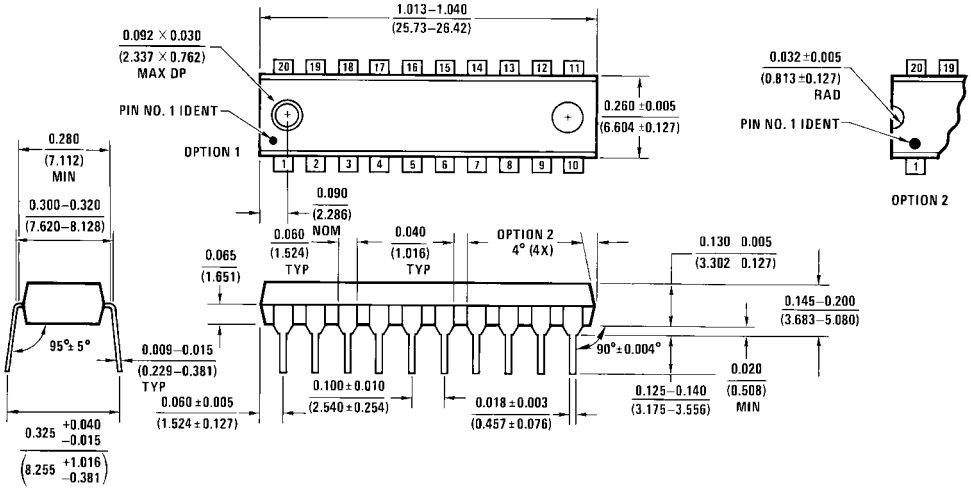
Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (t_{OSHL}), LOW-to-HIGH, (t_{OSLH}) or any combination of HIGH-to-LOW and/or LOW-to-HIGH, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A