

W24L010A



128K × 8 HIGH SPEED CMOS STATIC RAM

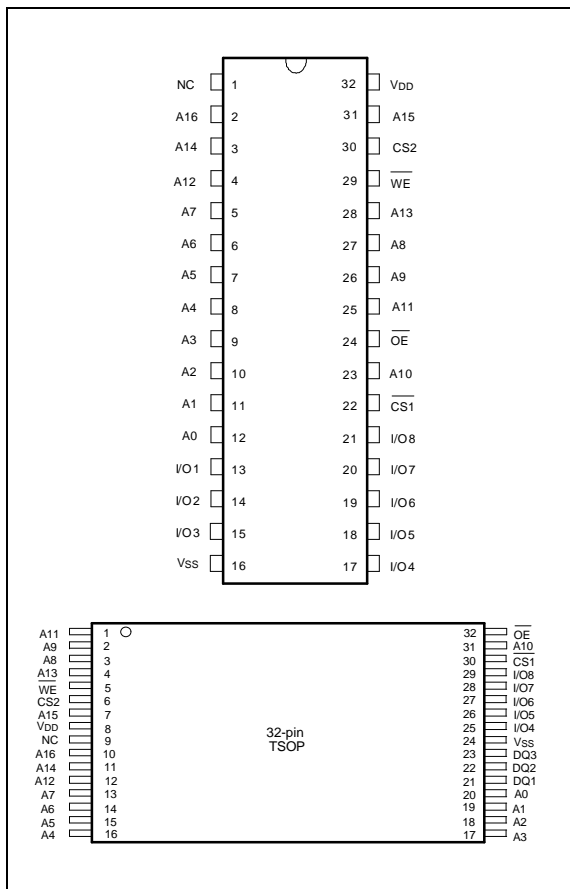
GENERAL DESCRIPTION

The W24L010A is a high speed, low power CMOS static RAM organized as 131072 × 8 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

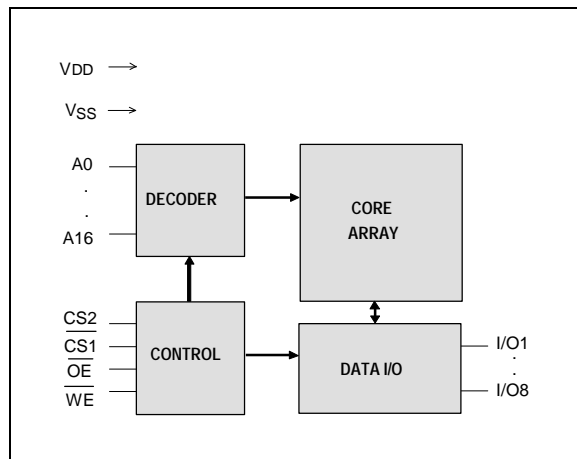
FEATURES

- High speed access time: 10/12/15 nS (max.)
- Low power consumption:
 - Active: 300 mW (typ.)
- Single +3.3V power supply
- Fully static operation
- All inputs and outputs directly TTL/LVTTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil SOJ, skinny DIP and TSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground
NC	No Connection



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +4.6	V
Input/Output to VSS Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

OPERATING CHARACTERISTICS

(VDD = 3.3V ±5%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Low Voltage	VIL	-	-0.5	-	+0.8	V	
Input High Voltage	VIH	-	+2.0	-	VDD +0.5	V	
Input Leakage Current	ILI	VIN = VSS to VDD	-10	-	+10	μA	
Output Leakage Current	ILO	VI/O = VSS to VDD CS1 = VIH or CS2 = VIL or OE = VIH or WE = VIL	-10	-	+10	μA	
Output Low Voltage	VOL	IOL = +8.0 mA	-	-	0.4	V	
Output High Voltage	VOH	IOH = -4.0 mA	2.4	-	-	V	
Operating Power Supply Current	IDD	CS1 = VIL, CS2 = VIH I/O = 0 mA Cycle = MIN Duty = 100%	10	-	-	130	mA
			12	-	-	120	mA
			15	-	-	100	mA
Standby Power	ISB	CS1 = VIH, or CS2 = VIL	-	-	15	mA	
Supply Current	ISB1	CS1 ≥ VDD -0.2V or CS2 ≤ 0.2V	-	-	5	mA	

Note: Typical characteristics are at VDD = 3.3V, TA = 25° C.



CAPACITANCE

(VDD = 3.3V, TA = 25° C, f = 1 MHz)

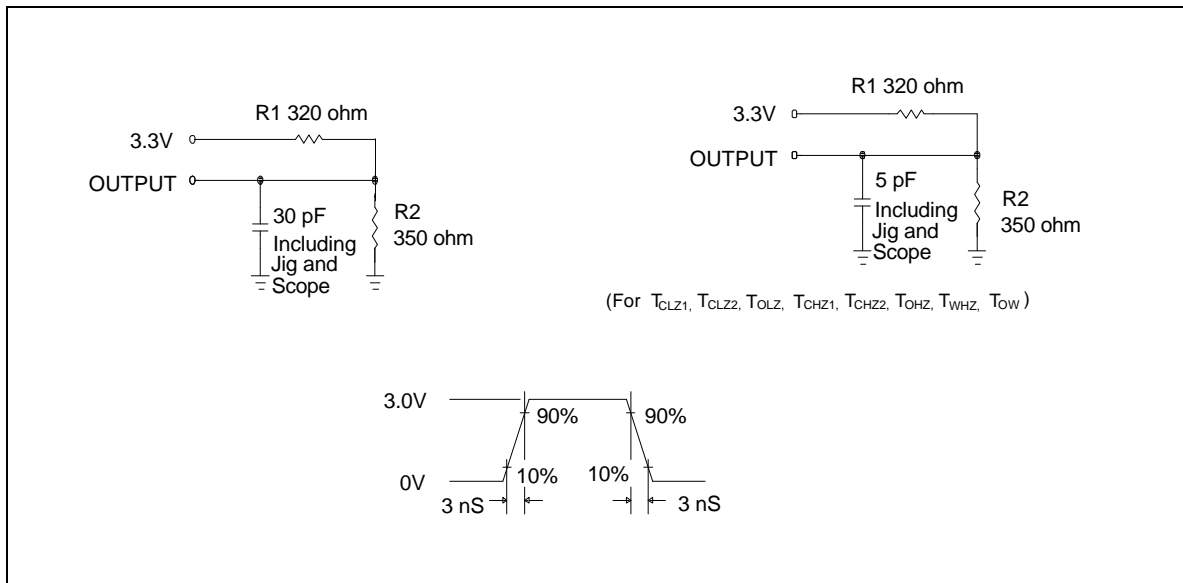
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	8	pF
Input/Output Capacitance	CI/O	VOUT = 0V	10	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 nS
Input and Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, IOH/IOL = -4 mA/8 mA

AC TEST LOADS AND WAVEFORM



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AC CHARACTERISTICS

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	W24L010A-10		W24L010A-12		W24L010A-15		UNIT	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Cycle Time	TRC	10	-	12	-	15	-	nS	
Address Access Time	TAA	-	10	-	12	-	15	nS	
Chip Select Access Time	$\overline{\text{CS1}}$	TACS1	-	10	-	12	-	15	nS
	CS2	TACS2	-	10	-	12	-	15	nS
Output Enable to Output Valid	TAOE	-	5	-	6	-	7	nS	
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	TCLZ1*	3	-	3	-	3	-	nS
	CS2	TCLZ2*	3	-	3	-	3	-	nS
Output Enable to Output in Low Z	TO LZ*	0	-	0	-	0	-	nS	
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	TCHZ1*	-	5	-	6	-	7	nS
	CS2	TCHZ2*	-	5	-	6	-	7	nS
Output Disable to Output in High Z	TOHZ*	-	5	-	6	-	7	nS	
Output Hold from Address Change	TOH	3	-	3	-	3	-	nS	

* These parameters are sampled but not 100% tested.

Write Cycle

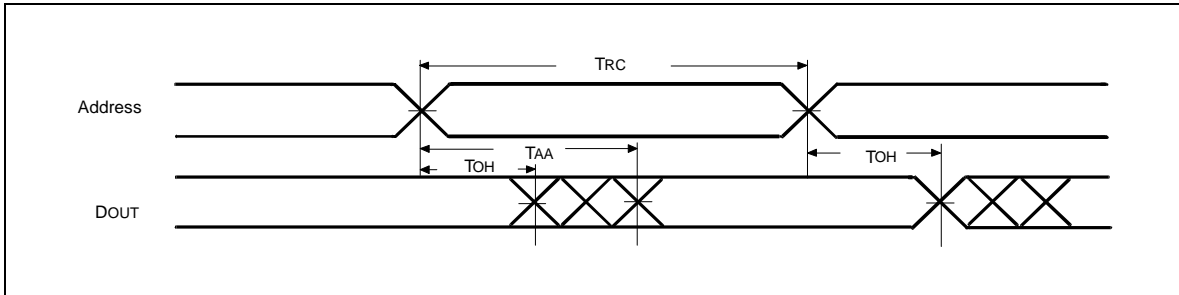
PARAMETER	SYM.	W24L010A-10		W24L010A-12		W24L010A-15		UNIT	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Cycle Time	TWC	10	-	12	-	15	-	nS	
Chip Selection to End of Write	$\overline{\text{CS1}}$	TCW1	9	-	10	-	13	-	nS
	CS2	TCW2	9	-	10	-	13	-	nS
Address Valid to End of Write	TAW	9	-	10	-	13	-	nS	
Address Setup Time	TAS	0	-	0	-	0	-	nS	
Write Pulse Width	TWP	9	-	10	-	10	-	nS	
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	TWR1	0	-	0	-	0	-	nS
	CS2	TWR2	0	-	0	-	0	-	nS
Data Valid to End of Write	TDW	5	-	7	-	9	-	nS	
Data Hold from End of Write	TDH	0	-	0	-	0	-	nS	
Write to Output in High Z	TWHZ*	-	5	-	6	-	8	nS	
Output Disable to Output in High Z	TOHZ*	-	5	-	6	-	8	nS	
Output Active from End of Write	TOW	0	-	0	-	0	-	nS	

* These parameters are sampled but not 100% tested.

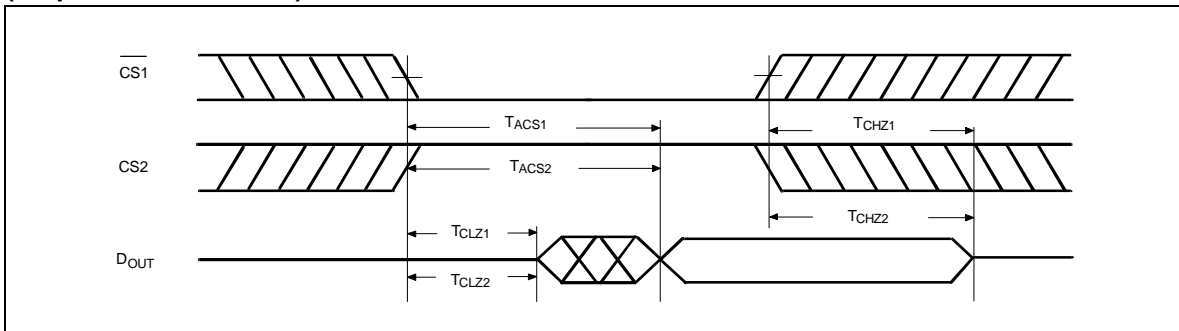


TIMING WAVEFORMS

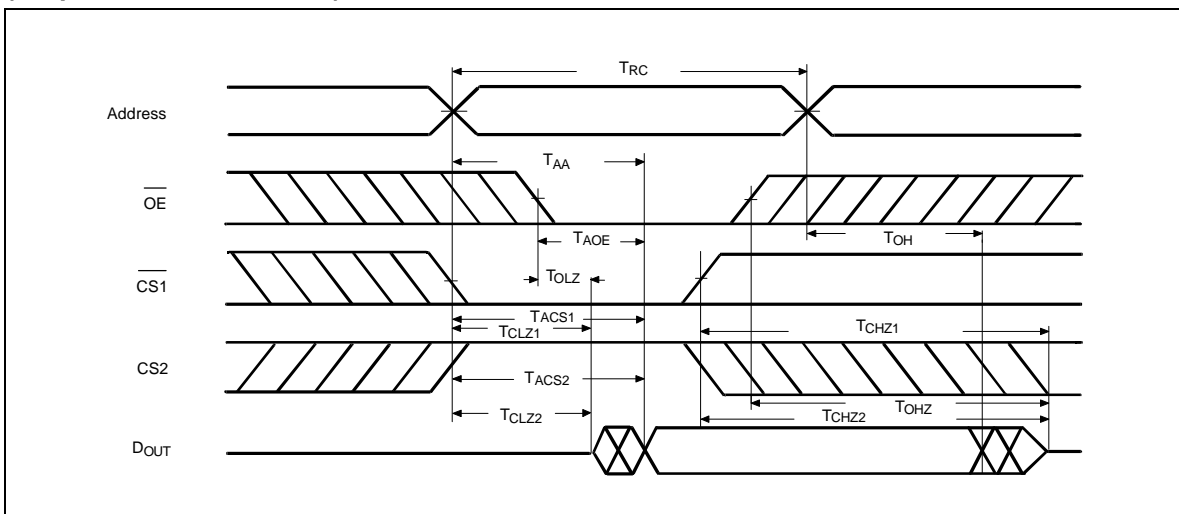
**Read Cycle 1
(Address Controlled)**



**Read Cycle 2
(Chip Select Controlled)**



**Read Cycle 3
(Output Enable Controlled)**

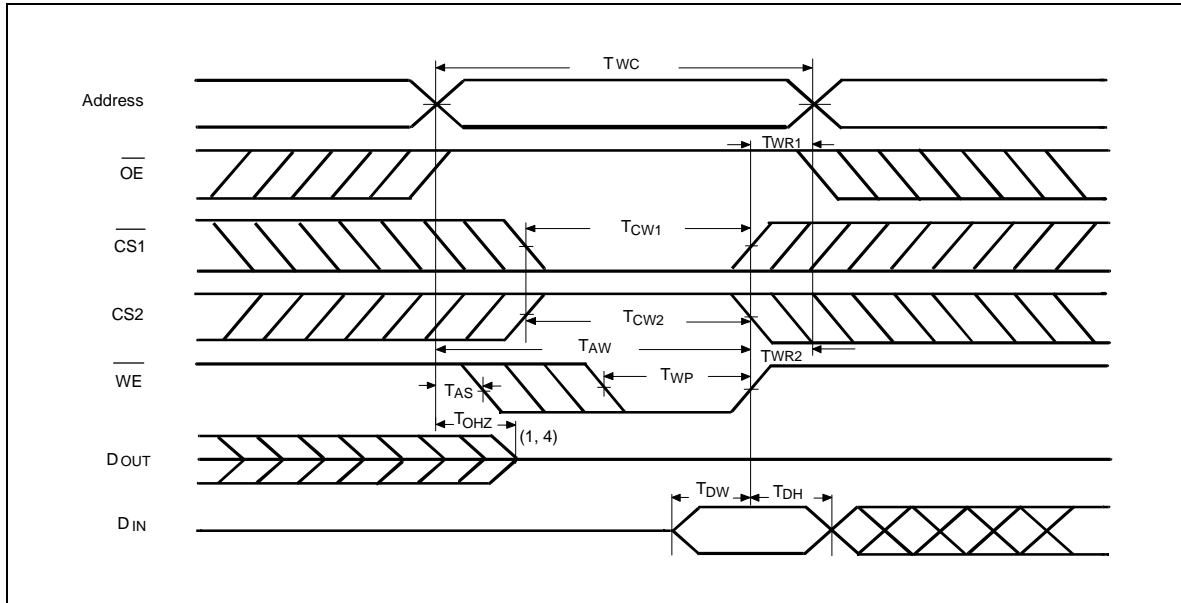




Timing Waveforms, continued

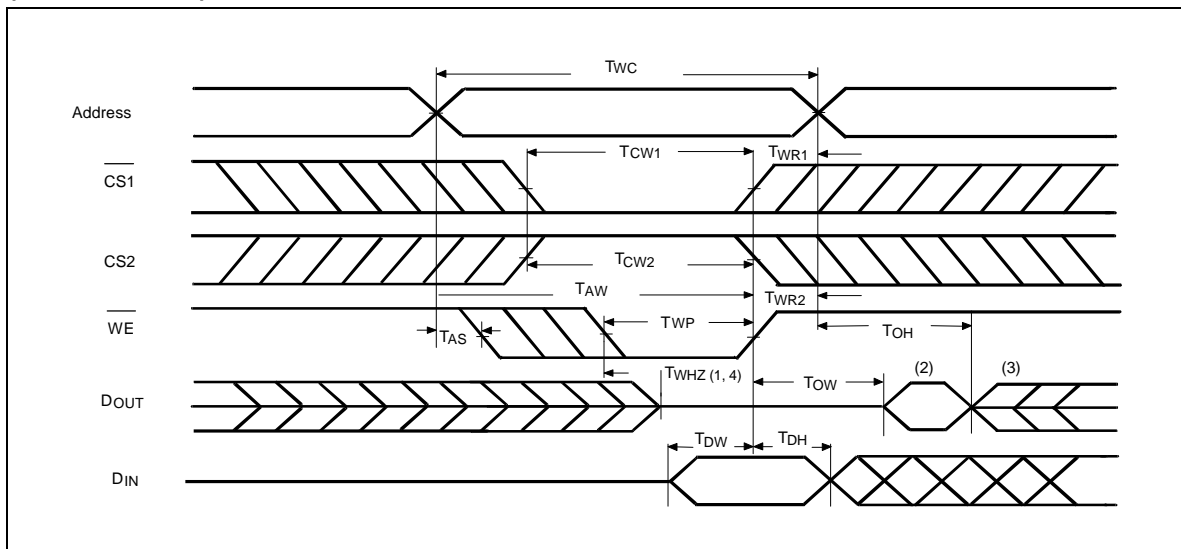
Write Cycle 1

(OE Clock)



Write Cycle 2

(OE = V_{IL} Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{out} provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with C_L = 5 pF. This parameter is guaranteed but not 100% tested.

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ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24L010AK-10	10	130	5	300 mil skinny DIP
W24L010AK-12	12	120	5	300 mil skinny DIP
W24L010AK-15	15	100	5	300 mil skinny DIP
W24L010AJ-10	10	130	5	300 mil SOJ
W24L010AJ-12	12	120	5	300 mil SOJ
W24L010AJ-15	15	100	5	300 mil SOJ
W24L010AT-10	10	130	5	Type one TSOP
W24L010AT-12	12	120	5	Type one TSOP
W24L010AT-15	15	100	5	Type one TSOP

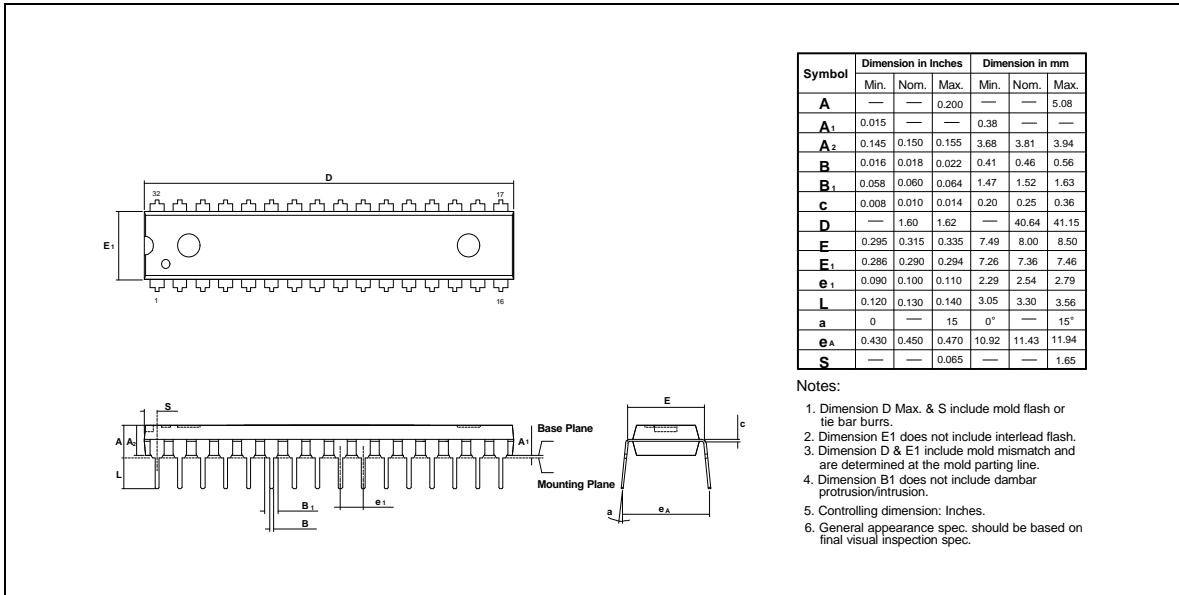
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

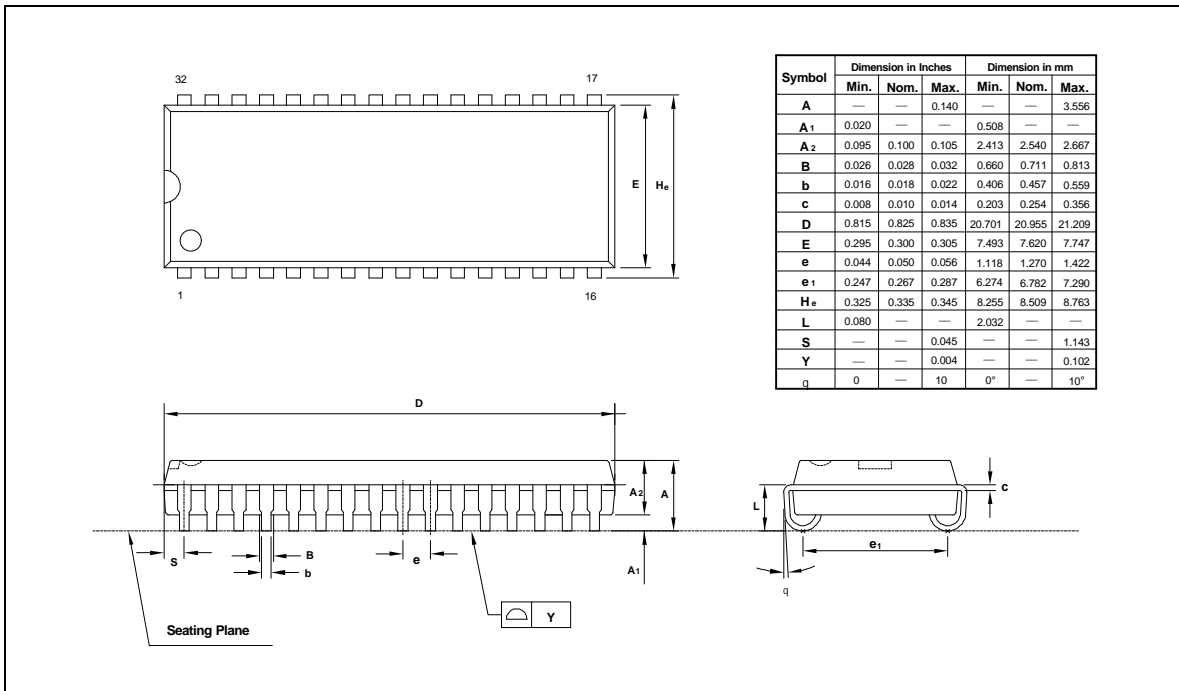


PACKAGE DIMENSIONS

32-pin P-DIP Skinny (300 mil)



32-pin SOJ

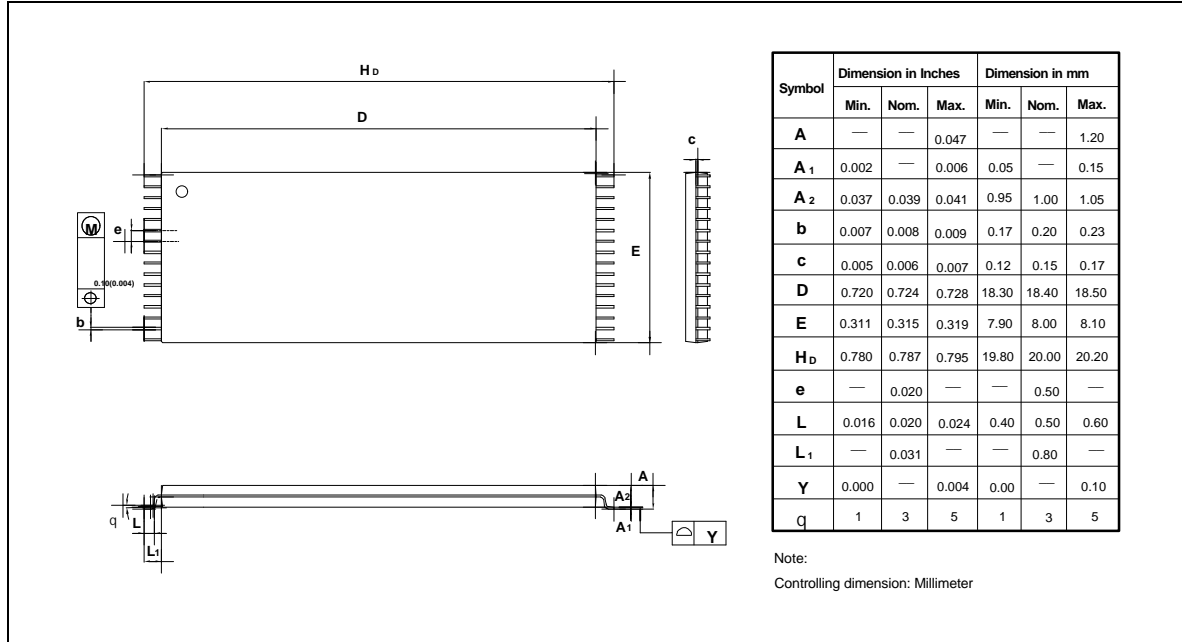


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Package Dimensions, continued

32-pin TSOP



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Note: All data and specifications are subject to change without notice.

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