NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1678G

5 V-BIAS, +17.5 dBm OUTPUT, 2.0 GHz WIDEBAND Si MMIC AMPLIFIER

DESCRIPTION

The μPC1678G is a silicon monolithic integrated circuit designed as medium output power amplifier for high frequency system applications. Due to +17.5 dBm TYP. output at 2 GHz, this IC is recommendable for transmitter stage amplifier of L BAND wireless communication systems. This IC is packaged in 8-pin plastic SOP.

This IC is manufactured using NEC's 20 GHz f_T NESAT™IV silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Supply voltage : V_{CC} = 4.5 to 5.5 V
- Saturated output power : $P_{O(sat)}$ = +17.5 dBm TYP. @ f = 500 MHz with external inductor
- Wideband response : f_u = 2.0 GHz TYP. @ 3 dB bandwidth
- Power gain : G_P = 23 dB TYP. @ f = 500 MHz
- Isolation : ISL = 35 dB TYP. @ f = 500 MHz

APPLICATIONS

- PA driver for high frequency system.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC1678G	8-pin plastic SOP (225 mil)	1678	Plastic magazine case
μPC1678G -E1			Embossed tape 12 mm wide. 1 pin is tape pull-out direction. Qty 2.5 kp/reel.
μPC1678G -E2			Embossed tape 12 mm wide. 1 pin is tape roll-in direction. Qty 2.5 kp/reel.

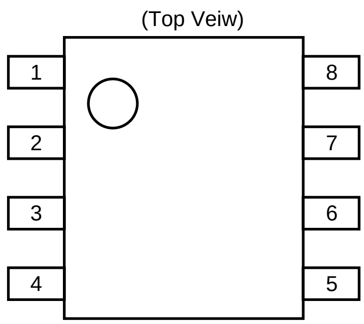
Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC1678G)

Caution Electro-static sensitive devices

Document No. P11491EJ4V0DS00 (4th edition)
Date Published September 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

PIN CONNECTIONS



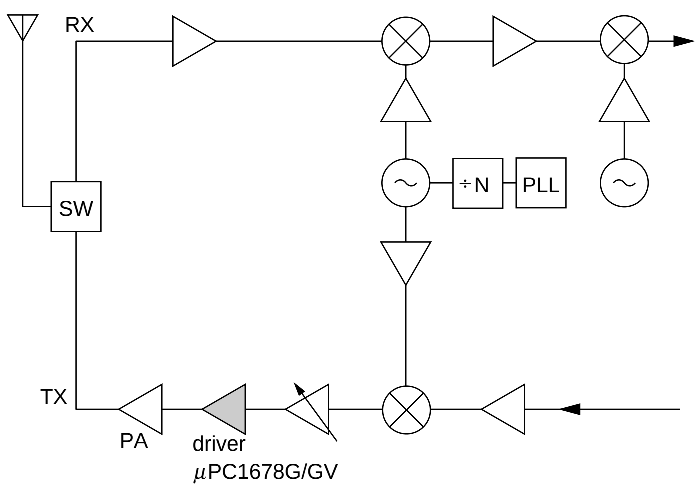
Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	GND
5	OUTPUT
6	GND
7	GND
8	V_{CC}

PRODUCT LINE-UP (T_A = +25 °C, V_{CC} = V_{out} = 5.0 V, Z_L = Z_S = 50 Ω)

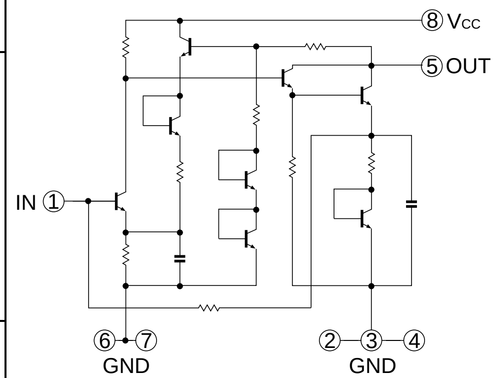
Part Number	f_u (GHz)	$P_{O(sat)}$ (dBm)	G_P (dB)	NF (dB)	I_{CC} (mA)	Package
μPC1678G	2.0	+17.5	23	6.0	49	8-pin plastic SOP (225 mil)
μPC1678GV	2.0	+17.5	23	6.0	49	8-pin plastic SSOP (175 mil)

Remark Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

SYSTEM APPLICATION EXAMPLE



PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Function and Applications	Internal Equivalent Circuit
1	INPUT	–	Signal input pin. A internal matching circuit, configured with resisters, enables 50 Ω connection over a wide band. A multi-negative feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to signal source with capacitor for DC cut.	 2, 3, 4, 6 and 7 are shorted by a lead frame.
2 3 4 6 7	GND	0	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as widely as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	
5	OUTPUT	Voltage as same as V_{CC} through external inductor	Signal output pin. The inductor must be attached between V_{CC} and output pins to supply current to the internal output transistors.	
8	V_{CC}	4.5 to 5.5	Power supply pin, which biases the internal input transistors. This pin should be externally equipped with bypass capacitor to minimize its impedance.	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	T_A = +25 °C, pin 5 and 8	6	V
★ Power Dissipation	P_D	Mounted on double copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T_A = +85 °C)	360	mW
Operating Ambient Temperature	T_A		–45 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Input Power	P_{in}	T_A = +25 °C	+10	dBm

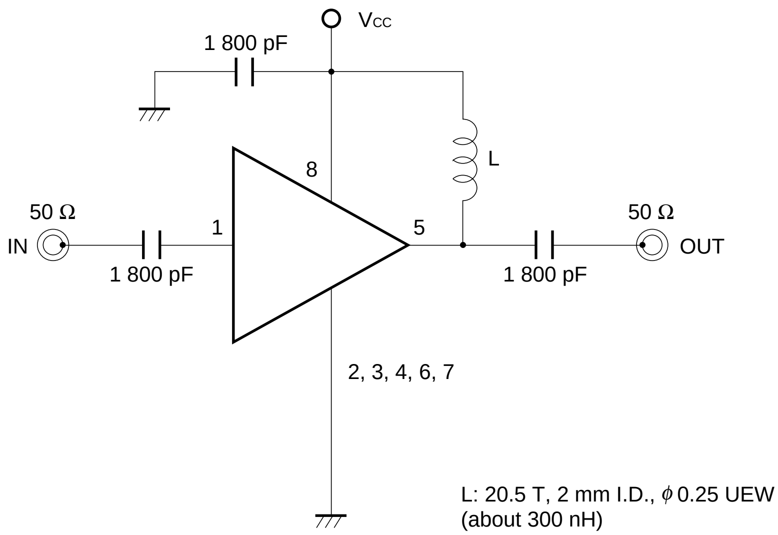
RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notice
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	The same voltage should be applied to pin 5 and 8
Operating Ambient Temperature	T_A	–45	+25	+85	°C	

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = V_{out} = 5.0 V, Z_S = Z_L = 50 Ω)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal	40.0	49.0	60.0	mA
Power Gain	G_P	f = 500 MHz	21	23	25	dB
Noise Figure	NF	f = 500 MHz	–	6.0	8.0	dB
Upper Limit Operating Frequency	f_u	3 dB down below the gain at 0.1 GHz	1.7	2.0	–	GHz
Isolation	ISL	f = 500 MHz	30	35	–	dB
Input Return Loss	RL_{in}	f = 500 MHz	11	14	–	dB
Output Return Loss	RL_{out}	f = 500 MHz	1	4	–	dB
Saturated Output Power	$P_{O(sat)}$	f = 500 MHz	+15.5	+17.5	–	dBm

TEST CIRCUIT



INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 30 mA, to output medium power. To supply current for output transistor, connect an inductor between the V_{CC} pin (pin 8) and output pin (pin 5).

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

CAPACITORS FOR THE V_{CC}, INPUT AND OUTPUT PINS

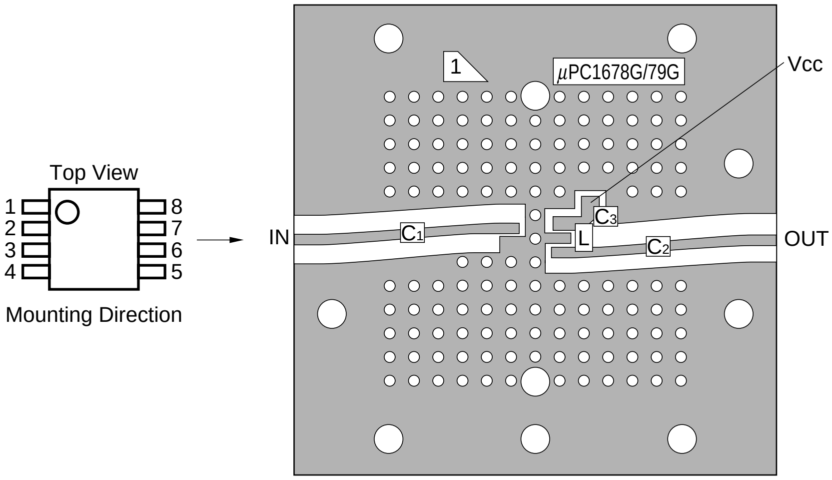
Capacitors of 1 800 pF are recommendable as the bypass capacitor for the V_{CC} pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the V_{CC} pin is used to minimize ground impedance of V_{CC} pin. So, stable bias can be supplied against V_{CC} fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 800 pF capacitors are used in the test circuit. In the case of under 100 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation, $C = 1/(2\pi Rfc)$.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

	Value
C_1 to C_3	1 800 pF
L	300 nH

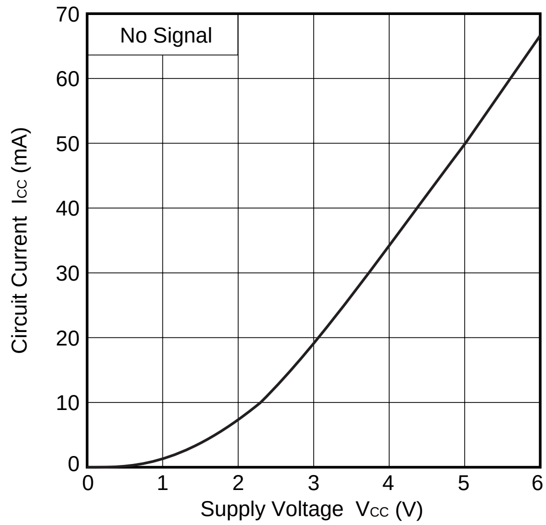
Notes

1. 50 × 50 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○ ◯ : Through holes

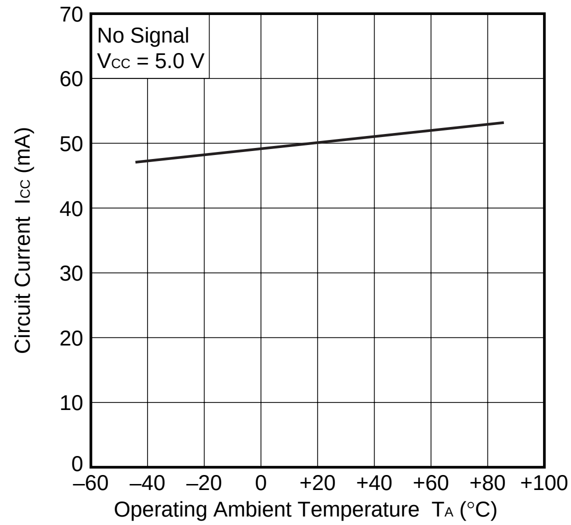
For more information on the use of this IC, refer to the following application note: USAGE AND APPLICATION OF SILICON MEDIUM-POWER HIGH-FREQUENCY AMPLIFIER MMIC (P12152E).

TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25 °C)

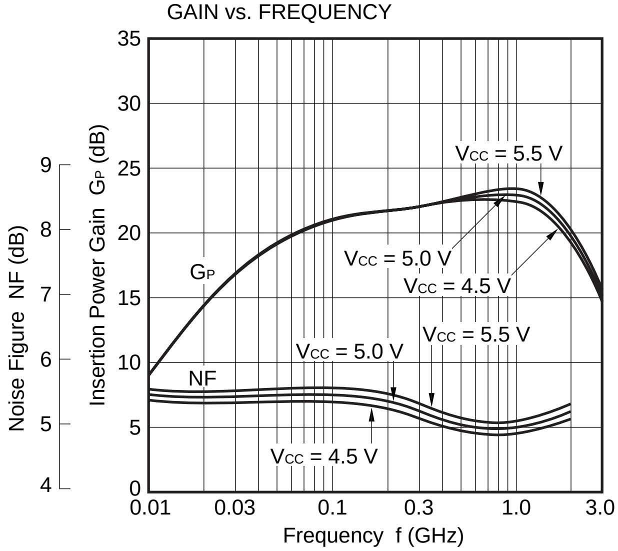
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



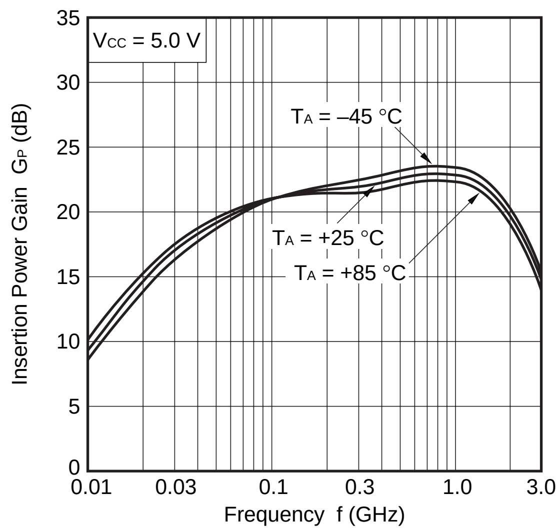
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



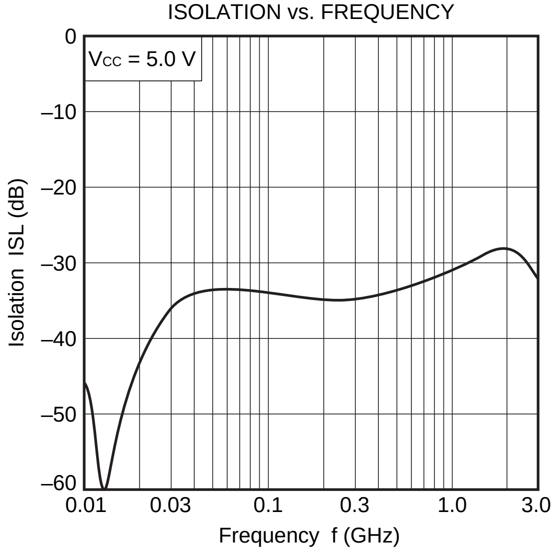
NOISE FIGURE AND INSERTION POWER GAIN vs. FREQUENCY



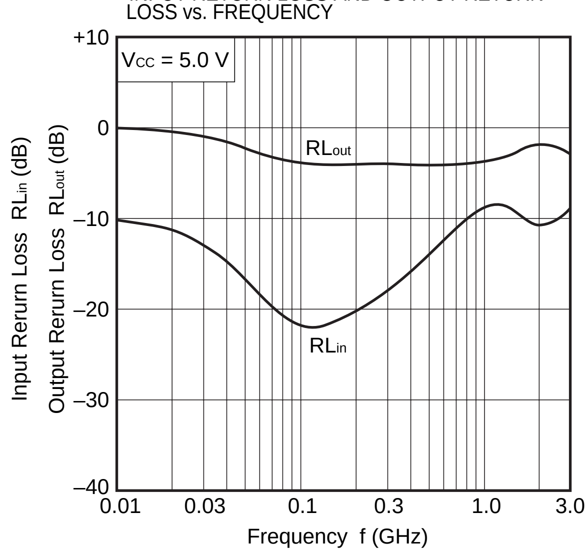
INSERTION POWER GAIN vs. FREQUENCY

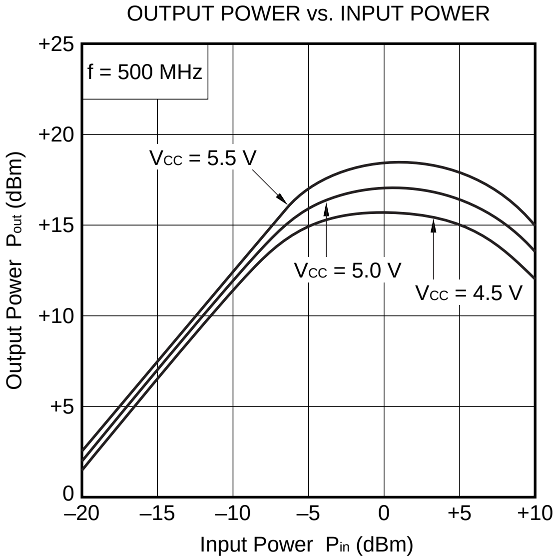


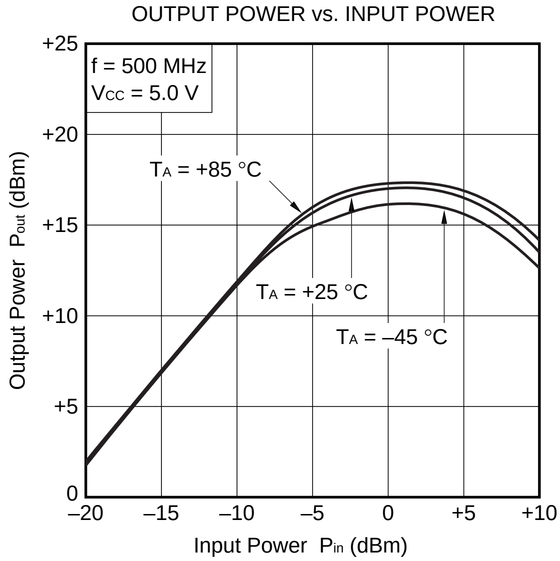
ISOLATION vs. FREQUENCY

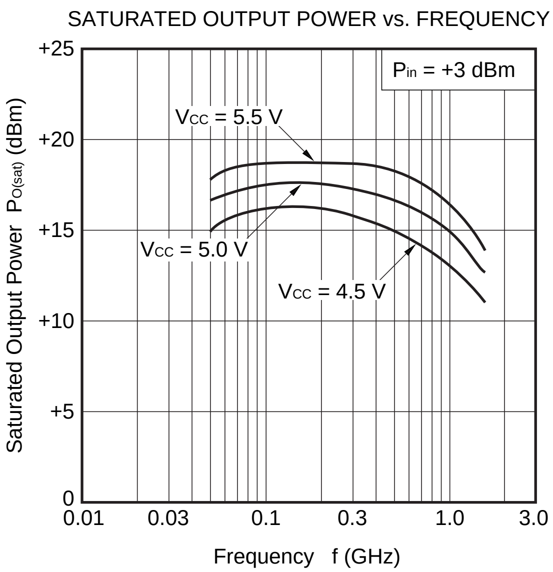


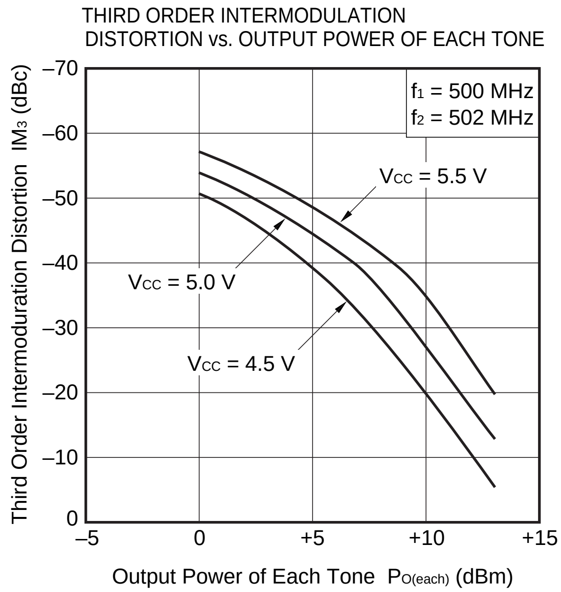
INPUT RETURN LOSS AND OUTPUT RETURN LOSS vs. FREQUENCY




OUTPUT POWER vs. INPUT POWER
f = 500 MHz
Vcc = 5.5 V
Vcc = 5.0 V
Vcc = 4.5 V
Output Power Pout (dBm)
Input Power Pin (dBm)
+25
+20
+15
+10
+5
0
–20
–15
–10
–5
0
+5
+10

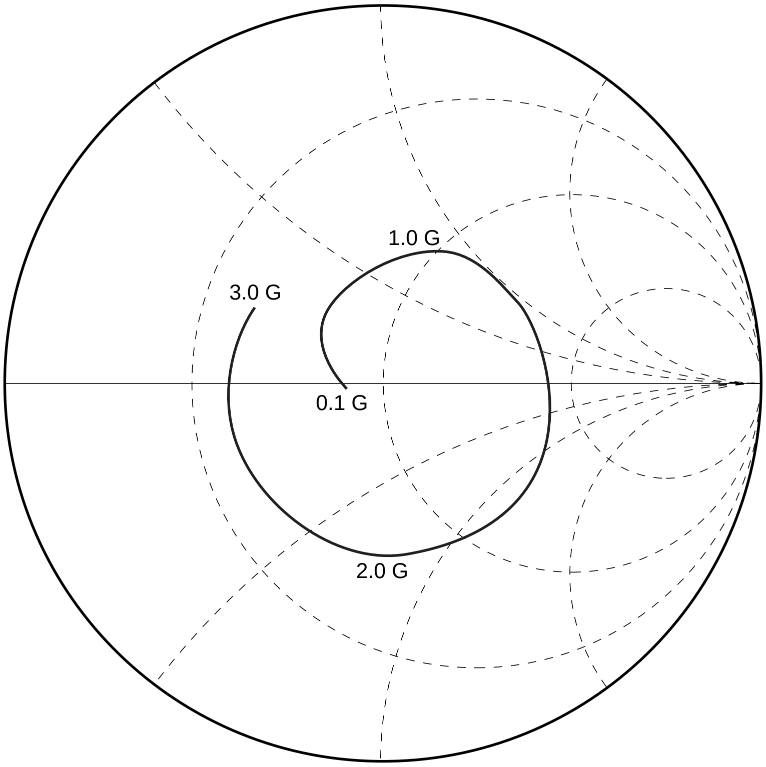

OUTPUT POWER vs. INPUT POWER
f = 500 MHz
Vcc = 5.0 V
TA = +85 °C
TA = +25 °C
TA = –45 °C
Output Power Pout (dBm)
Input Power Pin (dBm)


SATURATED OUTPUT POWER vs. FREQUENCY
Pin = +3 dBm
Vcc = 5.5 V
Vcc = 5.0 V
Vcc = 4.5 V
Saturated Output Power PO(sat) (dBm)
Frequency f (GHz)
0.01
0.03
0.1
0.3
1.0
3.0

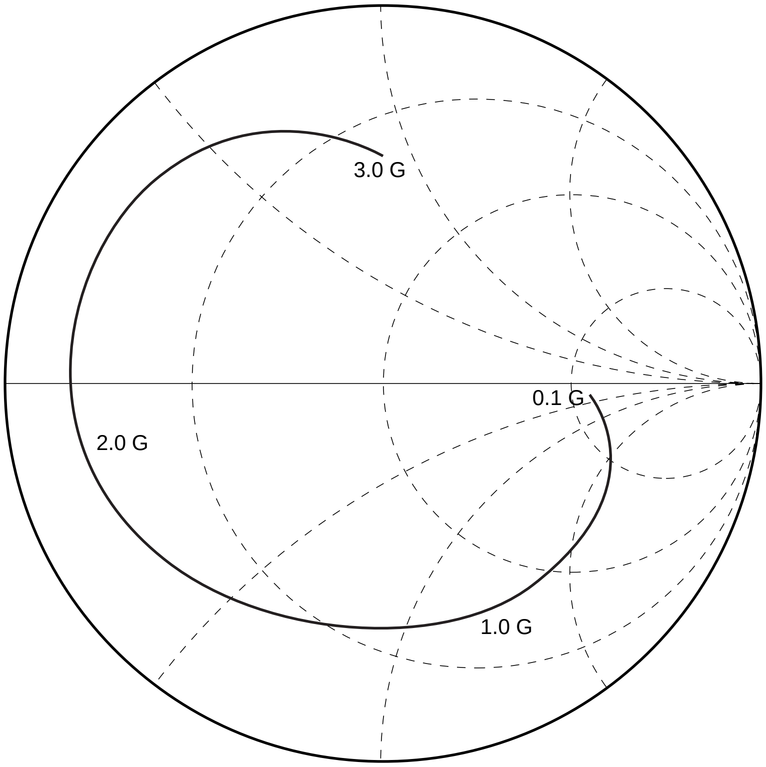

THIRD ORDER INTERMODULATION
DISTORTION vs. OUTPUT POWER OF EACH TONE
f1 = 500 MHz
f2 = 502 MHz
Vcc = 5.5 V
Vcc = 5.0 V
Vcc = 4.5 V
Third Order Intermoduration Distortion IM3 (dBc)
Output Power of Each Tone PO(each) (dBm)
–70
–60
–50
–40
–30
–20
–10
0
–5
0
+5
+10
+15

S-PARAMETER (T_A = +25 °C, V_{CC} = V_{out} = 5.0 V)

S_{11}-FREQUENCY



S_{22}-FREQUENCY



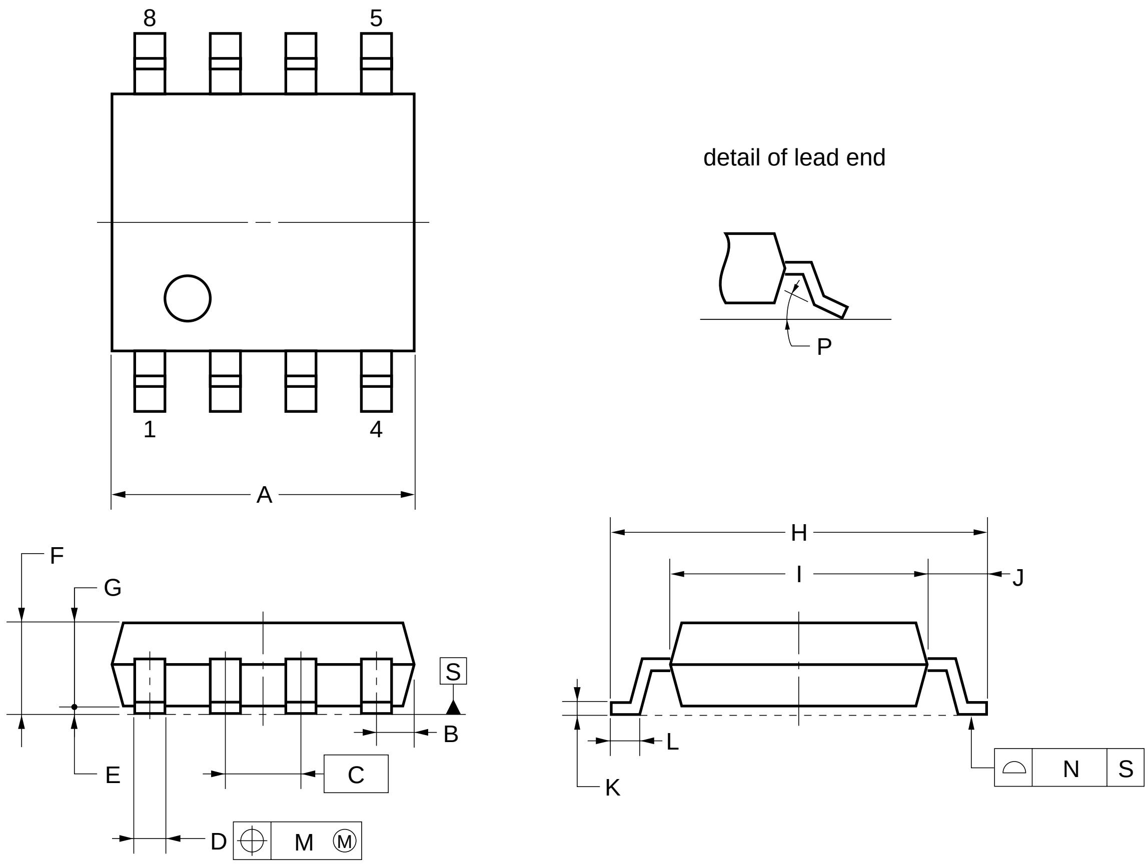
TYPICAL S-PARAMETER VALUES (T_A = +25 °C)

μPC1678G
$V_{CC} = V_{out}$ = 5.0 V, I_{CC} = 49 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}		K
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100.0000	0.078	–173.8	12.298	–4.0	0.023	–6.4	0.555	–3.2	1.40
200.0000	0.106	–179.1	12.891	–8.6	0.020	–7.3	0.593	–8.7	1.43
300.0000	0.140	166.3	13.625	–14.8	0.016	–4.7	0.630	–16.4	1.59
400.0000	0.176	150.2	14.453	–22.6	0.014	6.4	0.657	–25.3	1.53
500.0000	0.212	132.9	15.257	–31.5	0.014	23.1	0.673	–35.4	1.38
600.0000	0.246	115.5	15.663	–40.8	0.017	35.1	0.676	–45.1	1.05
700.0000	0.275	99.2	16.156	–51.3	0.020	41.0	0.669	–55.0	0.86
800.0000	0.304	83.2	16.291	–60.7	0.024	42.4	0.654	–64.0	0.71
900.0000	0.323	68.2	16.289	–71.0	0.027	41.8	0.627	–72.4	0.65
1000.0000	0.403	53.3	17.096	–80.2	0.030	47.1	0.660	–76.7	0.45
1100.0000	0.408	37.1	16.669	–90.7	0.036	43.0	0.646	–85.4	0.44
1200.0000	0.421	22.2	16.591	–100.7	0.036	41.3	0.639	–93.7	0.44
1300.0000	0.436	6.4	16.370	–111.2	0.041	36.5	0.660	–101.7	0.41
1400.0000	0.449	–8.4	16.056	–121.8	0.042	33.9	0.670	–109.8	0.40
1500.0000	0.463	–25.0	15.852	–131.6	0.045	28.3	0.690	–118.7	0.40
1600.0000	0.474	–41.5	15.332	–142.8	0.049	25.9	0.717	–127.0	0.41
1700.0000	0.472	–58.3	14.865	–154.2	0.048	22.1	0.734	–136.6	0.45
1800.0000	0.468	–76.1	14.169	–164.9	0.049	15.7	0.763	–146.9	0.48
1900.0000	0.457	–92.5	13.229	–176.8	0.048	13.7	0.783	–156.8	0.54
2000.0000	0.447	–109.6	12.144	172.6	0.048	8.1	0.806	–167.8	0.58
2100.0000	0.447	–126.4	10.947	162.7	0.049	4.0	0.830	–178.6	0.64
2200.0000	0.434	–142.6	9.853	153.4	0.047	–2.0	0.843	170.2	0.69
2300.0000	0.429	–158.5	8.796	146.3	0.044	–6.7	0.842	159.4	0.77
2400.0000	0.427	–173.0	7.894	139.7	0.040	–9.9	0.843	148.2	0.86
2500.0000	0.422	172.5	7.048	133.3	0.036	–12.5	0.825	137.4	0.99
2600.0000	0.419	158.3	6.363	128.8	0.027	–17.6	0.785	125.7	1.34
2700.0000	0.416	145.6	5.881	125.1	0.023	–17.2	0.744	117.2	1.71
2800.0000	0.400	136.1	5.387	121.3	0.018	4.5	0.701	109.7	2.34
2900.0000	0.402	126.2	5.223	116.2	0.018	11.0	0.681	103.0	2.53
3000.0000	0.406	118.1	5.030	113.5	0.020	28.2	0.645	96.5	2.45
3100.0000	0.397	109.8	4.675	107.3	0.022	35.3	0.616	90.7	2.47

★ **PACKAGE DIMENSIONS**

8 PIN PLASTIC SOP (225 mil) (Unit: mm)



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2±0.2
B	0.85 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.57±0.2
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as possible to keep mininum ground impedance (to prevent undesired oscillation).
All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
(3) The bypass capacitor should be attached to V_{CC} line.
(4) The inductor must be attached between V_{CC} and output pins. The inductance value should be determined in accordance with desired frequency.
(5) The DC cut capacitor must be each attached to the input and output pins.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit[Note]: None	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit[Note]: None	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit[Note]: None	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit[Note]: None	–

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

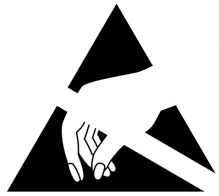
Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]

[MEMO]

[MEMO]



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

NESAT (NEC Silicon Advanced Technology) is a trademark of NEC Corporation.