

P-CHANNEL MOS FIELD EFFECT TRANSISTOR  
 FOR SWITCHING

DESCRIPTION

The  $\mu$ PA1912 is a switching device which can be driven directly by a 2.5-V power source.

The  $\mu$ PA1912 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- Can be driven by a 2.5-V power source
- Low on-state resistance  
 $R_{DS(on)1} = 50 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -2.5 \text{ A)}$   
 $R_{DS(on)2} = 52 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -2.5 \text{ A)}$   
 $R_{DS(on)3} = 70 \text{ m}\Omega \text{ MAX. (} V_{GS} = -2.5 \text{ V, } I_D = -2.5 \text{ A)}$

ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1912TE	6-pin Mini Mold (Thin Type)

ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

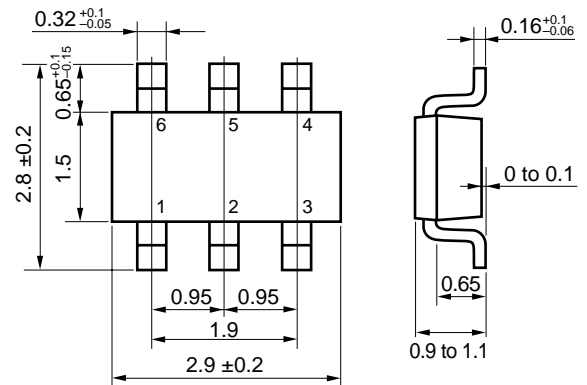
Drain to Source Voltage	V <sub>DSS</sub>	-12	V
Gate to Source Voltage	V <sub>GSS</sub>	±10	V
Drain Current (DC)	I <sub>D(DC)</sub>	±4.5	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±18	A
Total Power Dissipation	P <sub>T1</sub>	0.2	W
Total Power Dissipation <sup>Note2</sup>	P <sub>T2</sub>	2	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1 %  
**2.** Mounted on FR-4 board, t ≤ 5 sec.

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

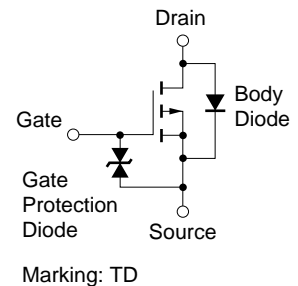
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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PACKAGE DRAWING (Unit : mm)



- 1, 2, 5, 6 : Drain  
 3 : Gate  
 4 : Source

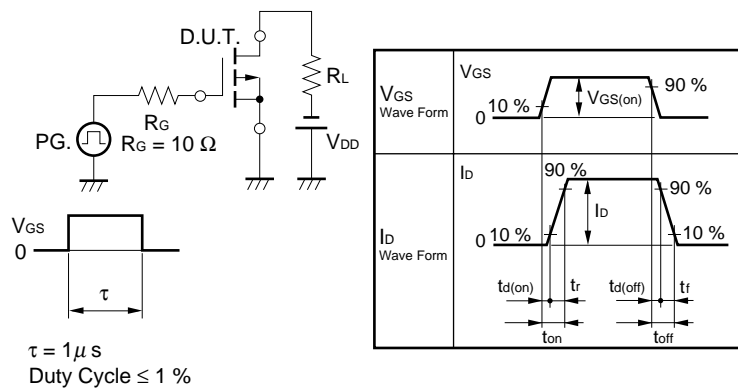
EQUIVALENT CIRCUIT



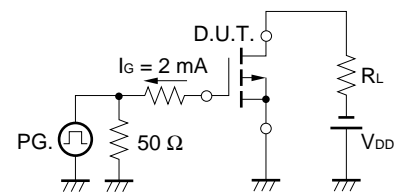
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-0.5	-0.90	-1.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.5 A	3	9.3		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.5 A		39	50	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -2.5 A		40	52	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.5 A		53	70	mΩ
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = -10 V		810		pF
Output Capacitance	C <sub>oSS</sub>	V <sub>GS</sub> = 0 V		241		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>	f = 1 MHz		122		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -6 V		304		ns
Rise Time	t <sub>r</sub>	I <sub>D</sub> = -2.5 A		532		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>GS(on)</sub> = -4.0 V		406		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		796		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -10 V		5.6		nC
Gate to Source Charge	Q <sub>GS</sub>	I <sub>D</sub> = -4.5 A		2.2		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = -4.0 V		2.6		nC
Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 4.5 A, V <sub>GS</sub> = 0 V		0.86		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4.5 A, V <sub>GS</sub> = 0 V		1.1		μs
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 10 A/μs		4.3		μC

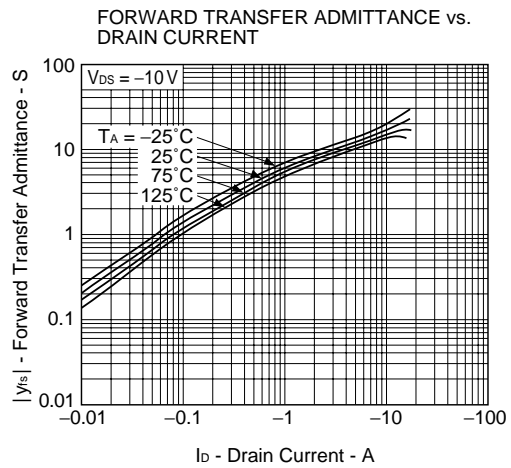
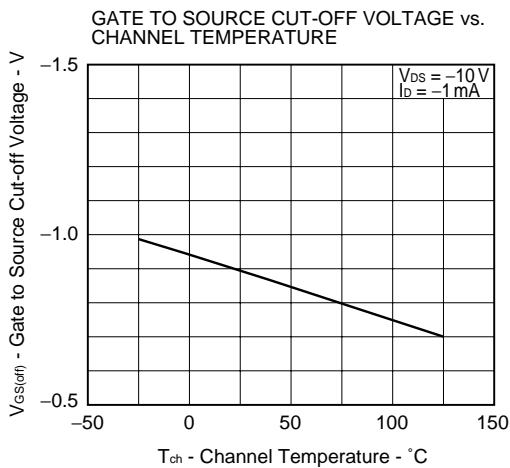
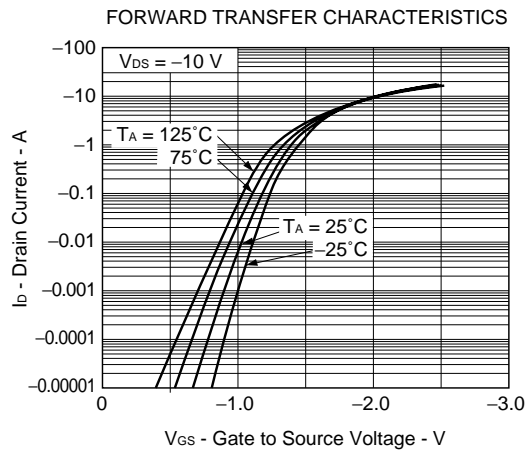
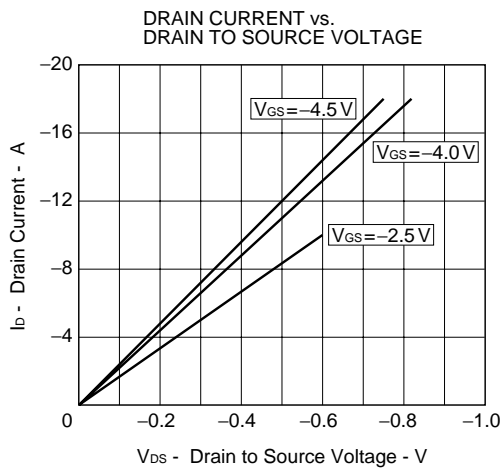
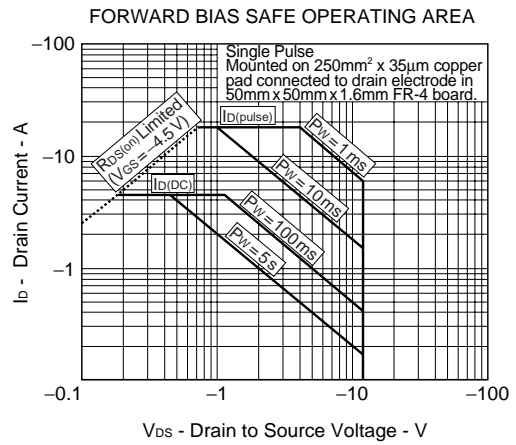
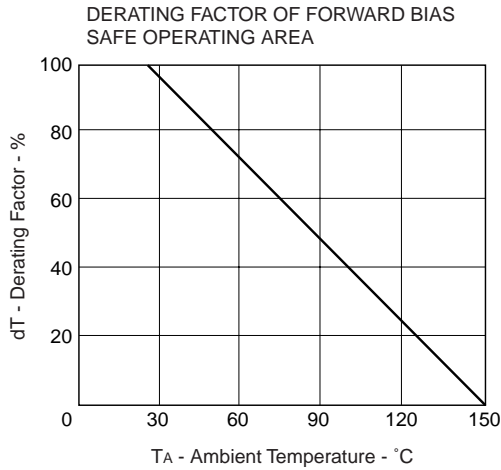
**TEST CIRCUIT 1 SWITCHING TIME**

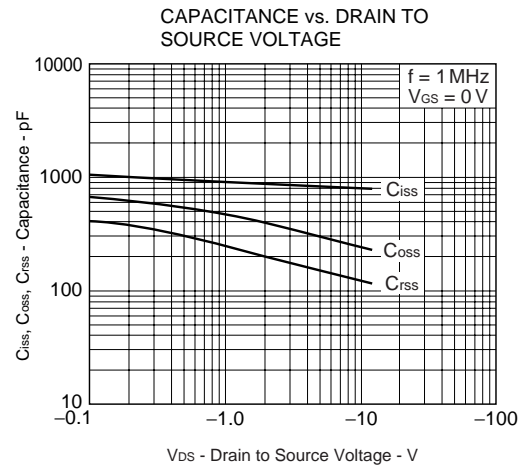
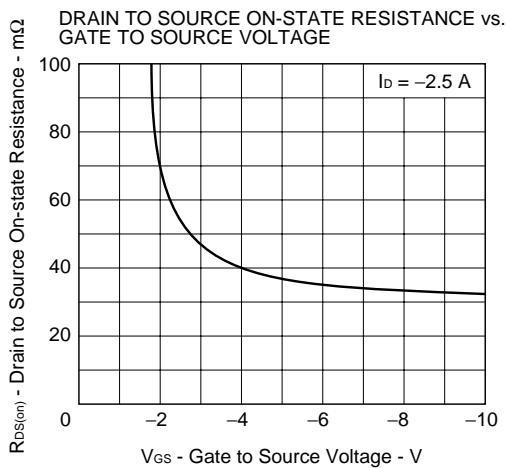
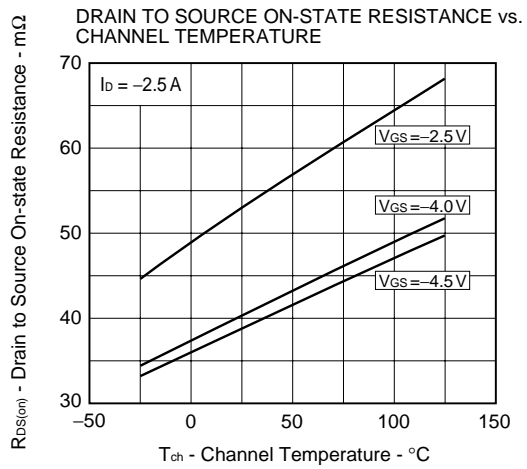
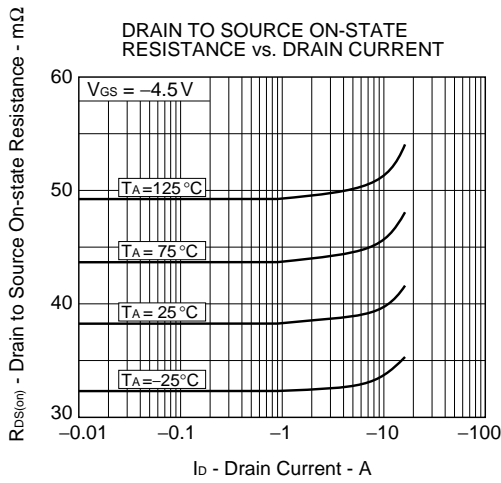
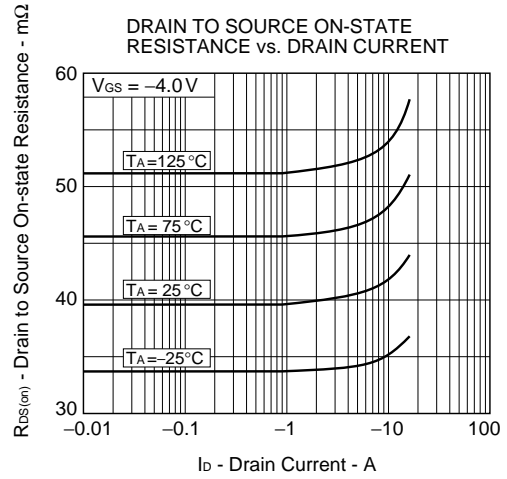
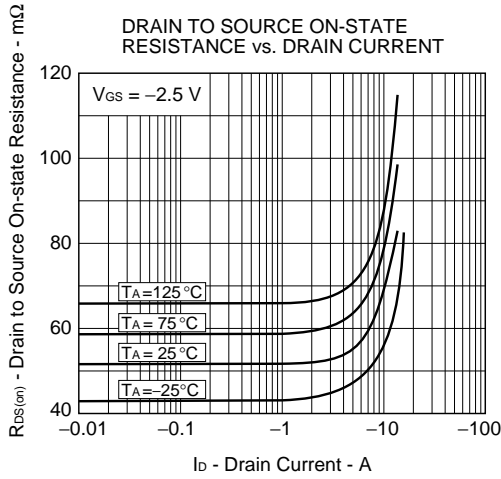


**TEST CIRCUIT 2 GATE CHARGE**

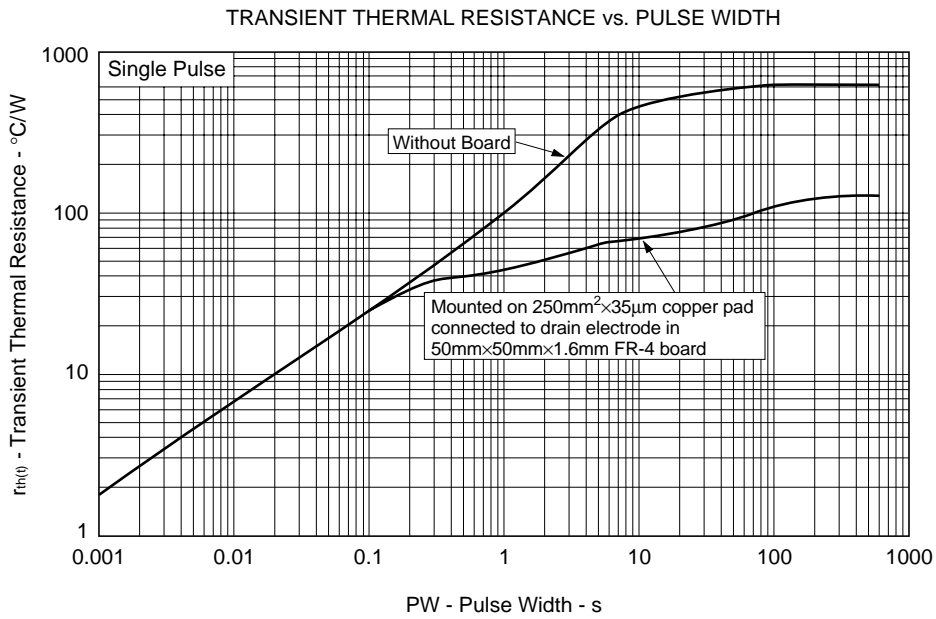
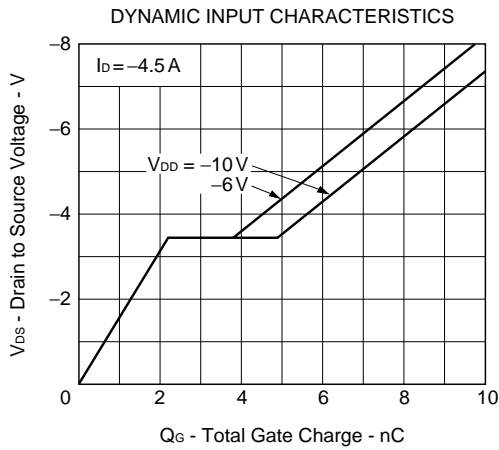
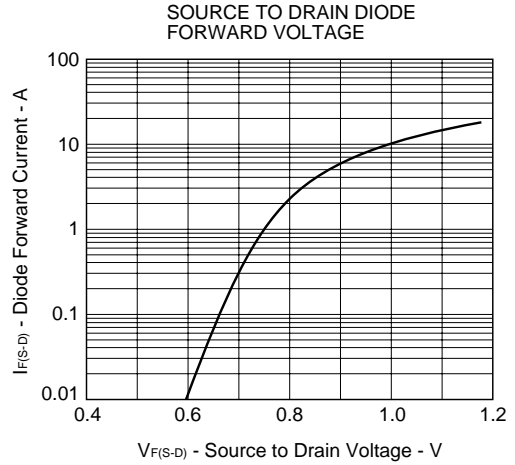
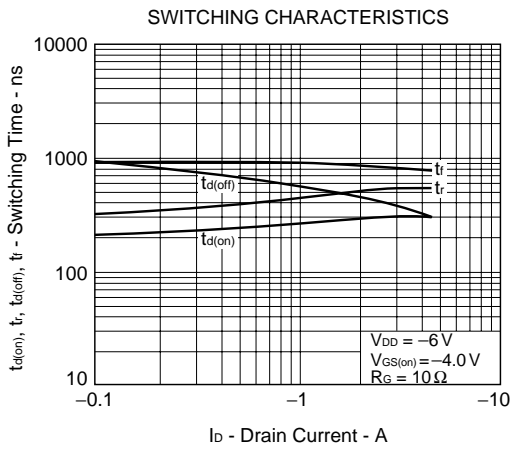


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )





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