

**SANYO**No. ~~X~~ 5398**LC361000AMLL, ATLL, ARLL-70/10****1 MEG (131072 words × 8 bits) SRAM****Preliminary****Overview**

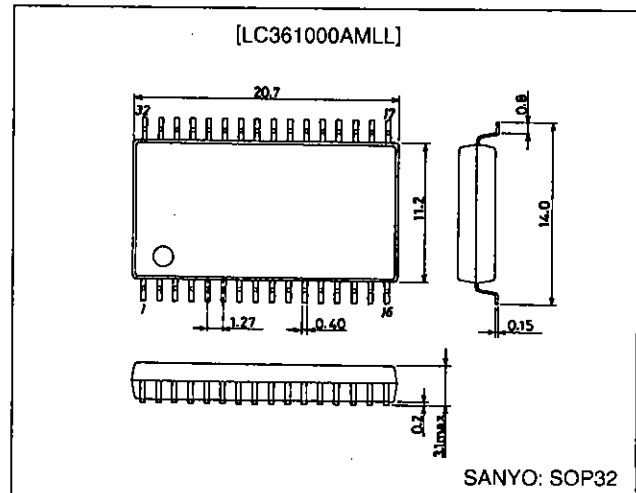
The LC361000AMLL, ATLL, and ARLL are 131072 words × 8 bits asynchronous silicon gate CMOS static RAMs. These SRAMs have two chip enable pins (CE1 and CE2) for controlling the device selected/unselected state and one output enable pin ( $\overline{OE}$ ) for output control and feature high speed and low power. This makes these SRAMs optimal for systems that require high speed, low power, and battery backup, and they furthermore allow easy expansion of memory capacity.

**Features**

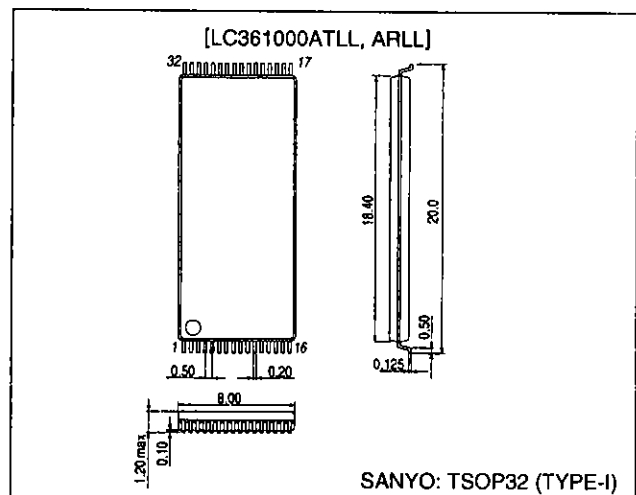
- Access time
  - 70 ns (max.): LC361000AMLL, ATLL, ARLL-70
  - 100 ns (max.): LC361000AMLL, ATLL, ARLL-10
- Low current drain
  - During standby
    - 2.0  $\mu$ A (max.)/ $T_a = 25^\circ\text{C}$
    - 4.0  $\mu$ A (max.)/ $T_a = 0$  to  $+40^\circ\text{C}$
    - 20.0  $\mu$ A (max.)/ $T_a = 0$  to  $+70^\circ\text{C}$
  - During data retention
    - 1.2  $\mu$ A (max.)/ $T_a = 25^\circ\text{C}$
    - 2.4  $\mu$ A (max.)/ $T_a = 0$  to  $+40^\circ\text{C}$
    - 12.0  $\mu$ A (max.)/ $T_a = 0$  to  $+70^\circ\text{C}$
  - During operating (DC)
    - 15 mA (max.)
- Single 5 V power supply: 5 V  $\pm$ 10%
- Data retention supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, three output states
- Package
  - SOP 32-pin (525 mil) plastic package:
    - LC361000AMLL
  - TSOP 32-pin (8 mm × 20 mm) plastic package, normal:
    - LC361000ATLL
  - TSOP 32-pin (8 mm × 20 mm) plastic package, reversed:
    - LC361000ARLL

**Package Dimensions**

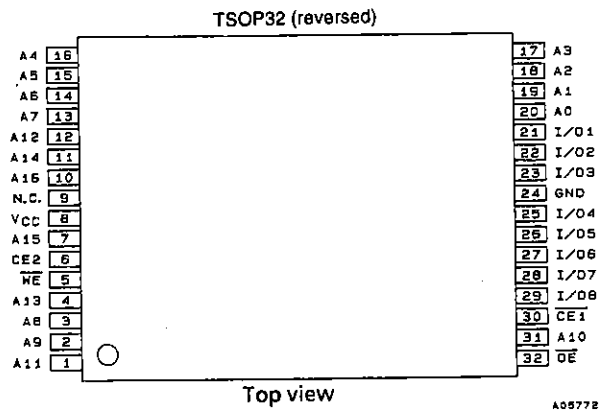
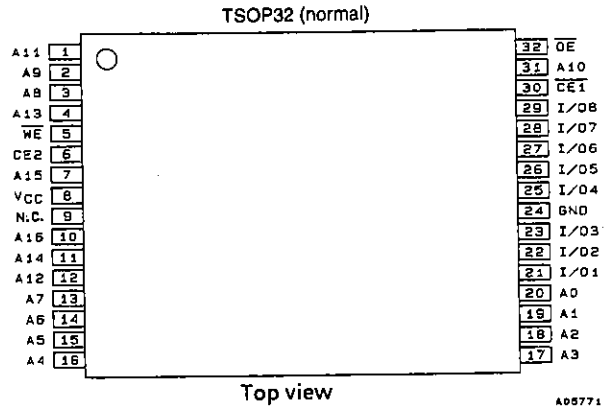
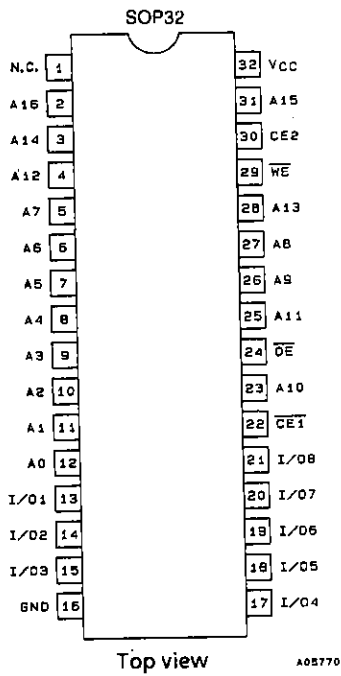
unit: mm

**3205-SOP32**

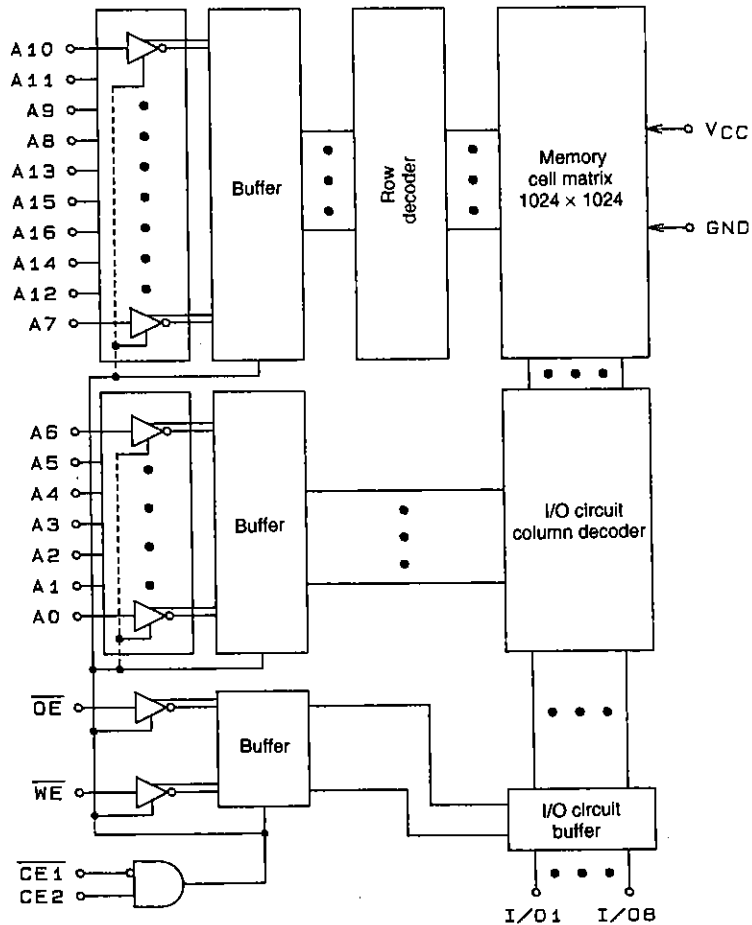
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**3224-TSOP32**

Pin Assignments



Block Diagram



### Pin Functions

A0 to A16	Address inputs
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE1}$ , CE2	Chip enable input
I/O1 to I/O8	Data input/output
$V_{CC}$ , GND	Power supply pins

### Function Logic

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	H	L	H	Data output	$I_{CCA}$
Write cycle	L	H	X	L	Data input	$I_{CCA}$
Output disable	L	H	H	H	High impedance	$I_{CCA}$
Nonselect	H	X	X	X	High impedance	$I_{CCS}$
	X	L	X	X	High impedance	$I_{CCS}$

X: H or L

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$	7.0	V
Input pin voltage	$V_{IN}$	-0.5* to $V_{CC}+0.5$	V
I/O pin voltage	$V_{I/O}$	-0.5* to $V_{CC}+0.5$	V
Allowable power dissipation	$P_d\ max$	0.7	W
Operating temperature	$T_{opr}$	0 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Note: \* -3.0 V when pulse width is less than 50 ns.

Stresses greater than the above listed maximum value may result in damage to the device.

#### DC Recommended Operating Ranges at $T_a = 0$ to $+70^\circ\text{C}$

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input high level voltage	$V_{IH}$	2.2		$V_{CC}+0.3$	V
Input low level voltage	$V_{IL}$	-0.3*		+0.8	V

Note: \* -3.0 V when pulse width is less than 50 ns.

## LC361000AMLL, ATLL, ARL-70/10

### DC Electrical Characteristics at Ta = 0 to +70°C

Parameter	Symbol	Conditions	min	typ*	max	Unit
Operating supply current (DC)	I <sub>CCA1</sub>	V <sub>CE1</sub> ≤ 0.2 V, V <sub>CE2</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, I <sub>I/O</sub> = 0 mA			10	mA
	I <sub>CCA2</sub>	V <sub>CE1</sub> = V <sub>IL</sub> , V <sub>CE2</sub> = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA		7	15	mA
Average operating supply current	I <sub>CCA3</sub>	V <sub>CE1</sub> = V <sub>IL</sub> , V <sub>CE2</sub> = V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA, min cycle	70 ns	40	70	mA
			100 ns	35	60	
Standby supply current	I <sub>CCS1</sub>	{V <sub>CE2</sub> ≤ 0.2 V} or {V <sub>CE1</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>CE2</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>CE2</sub> ≤ 0.2 V}	0 to +70°C		20	μA
			0 to +40°C		4	
			25°C	0.7	2	
	I <sub>CCS2</sub>	V <sub>CE2</sub> = V <sub>IL</sub> or V <sub>CE1</sub> = V <sub>IH</sub>		0.6	3	mA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1		+1	μA
I/O leakage current	I <sub>LO</sub>	V <sub>CE1</sub> = V <sub>IH</sub> or V <sub>CE2</sub> = V <sub>IL</sub> , or V <sub>OE</sub> = V <sub>IH</sub> or V <sub>WE</sub> = V <sub>IL</sub> , I <sub>I/O</sub> = 0 to V <sub>CC</sub>	-1		+1	μA
Output high level voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4			V
Output low level voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA			0.4	V

Note: \* Reference value at V<sub>CC</sub> = 5 V, Ta = 25°C.

### Input/Output Capacitances at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			7	pF
Input/output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			8	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

### AC Electrical Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ±10%

#### AC Test Conditions

Parameter	Conditions
Input pulse voltage level	0.8 V, 2.2 V
Input rise and fall time	5 ns
Input and output timing level	1.5 V
Output load	1 TTL gate + C <sub>L</sub> = 100 pF (70 ns/100 ns) (including scope and jig capacitances)

**Read Cycle**

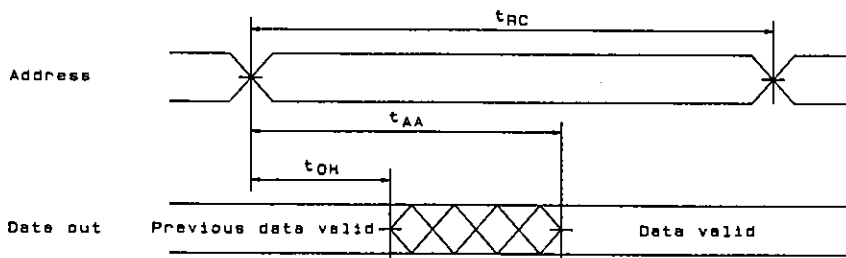
Parameter	Symbol	LC361000AMLL, ATLL, ARL				Unit
		-70		-10		
		min	max	min	max	
Read cycle time	$t_{RC}$	70		100		ns
Address access time	$t_{AA}$		70		100	ns
$\overline{CE1}$ access time	$t_{CA1}$		70		100	ns
CE2 access time	$t_{CA2}$		70		100	ns
$\overline{OE}$ access time	$t_{OA}$		40		50	ns
Output hold time	$t_{OH}$	15		15		ns
$\overline{CE1}$ output enable time	$t_{COE1}$	10		10		ns
CE2 output enable time	$t_{COE2}$	10		10		ns
$\overline{OE}$ output enable time	$t_{OOE}$	5		5		ns
$\overline{CE1}$ output disable time	$t_{COD1}$		25		35	ns
CE2 output disable time	$t_{COD2}$		25		35	ns
$\overline{OE}$ output disable time	$t_{OOD}$		25		35	ns

**Write Cycle**

Parameter	Symbol	LC361000AMLL, ATLL, ARL				Unit
		-70		-10		
		min	max	min	max	
Write cycle time	$t_{WC}$	70		100		ns
Address valid to end of write	$t_{AW}$	60		70		ns
Address setup time	$t_{AS}$	0		0		ns
Write pulse width	$t_{WP}$	50		70		ns
$\overline{CE1}$ setup time	$t_{CW1}$	60		70		ns
CE2 setup time	$t_{CW2}$	60		70		ns
Write recovery time	$t_{WR}$	0		0		ns
$\overline{CE1}$ write recovery time	$t_{WR1}$	0		0		ns
CE2 write recovery time	$t_{WR2}$	0		0		ns
Data setup time	$t_{DS}$	30		40		ns
Data hold time	$t_{DH}$	0		0		ns
$\overline{CE1}$ data hold time	$t_{DH1}$	0		0		ns
CE2 data hold time	$t_{DH2}$	0		0		ns
$\overline{WE}$ output enable time	$t_{WOE}$	10		10		ns
$\overline{WE}$ output disable time	$t_{WOD}$		25		30	ns

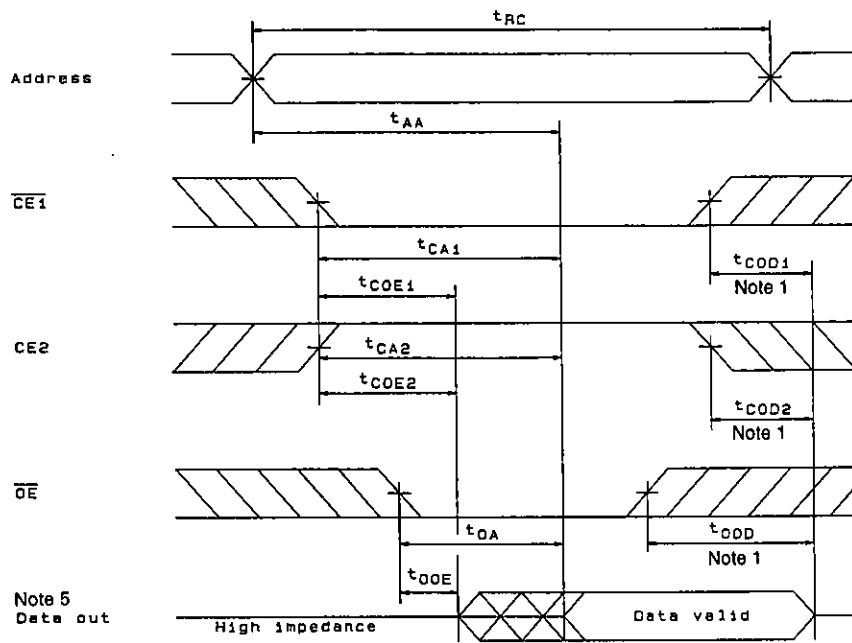
**Timing Chart**

Read Cycle (1):  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



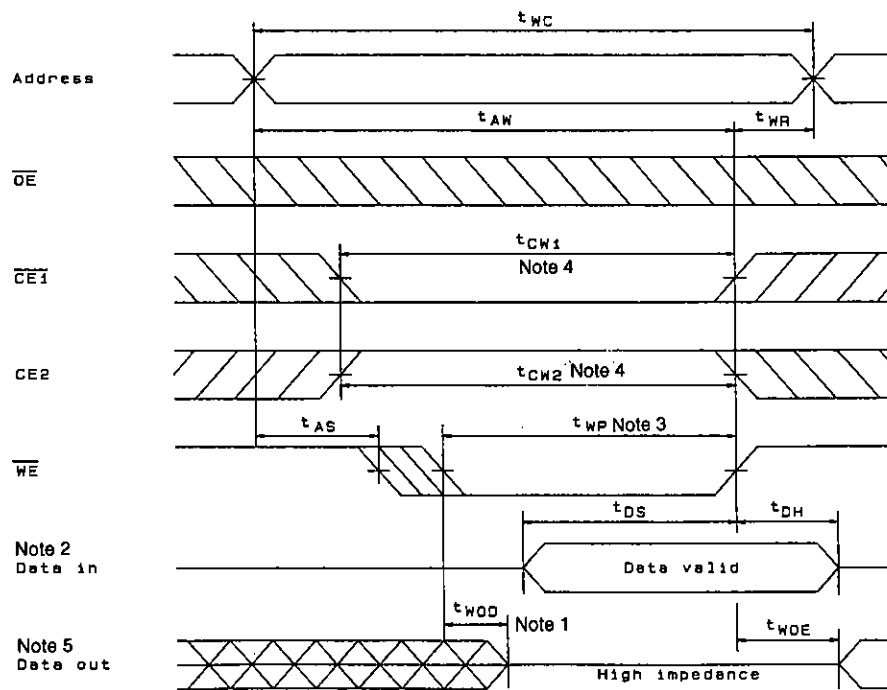
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Read Cycle (2):  $\overline{WE} = V_{IH}$



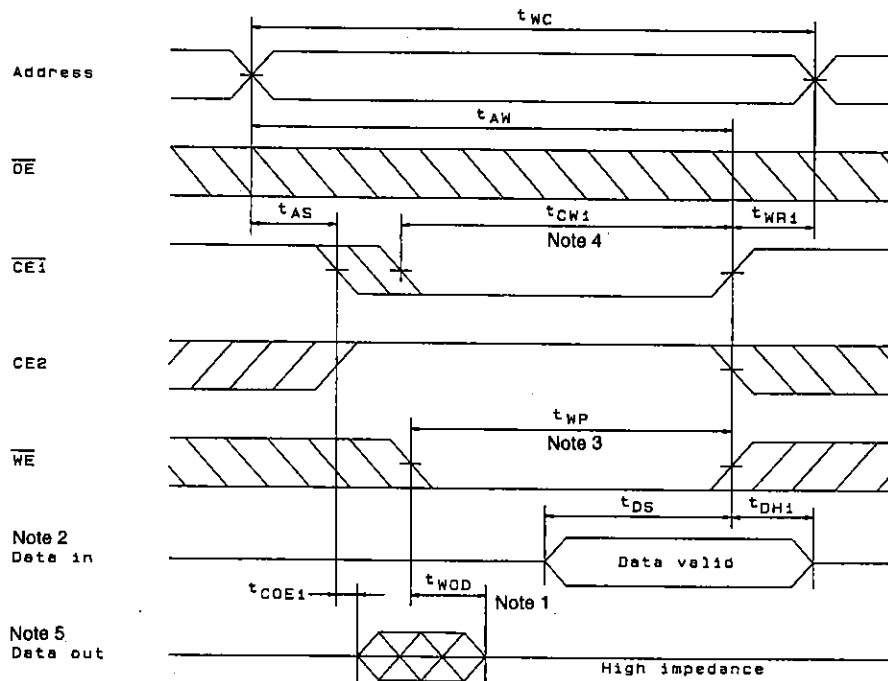
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Write Cycle (1):  $\overline{WE}$  control (Note 6)



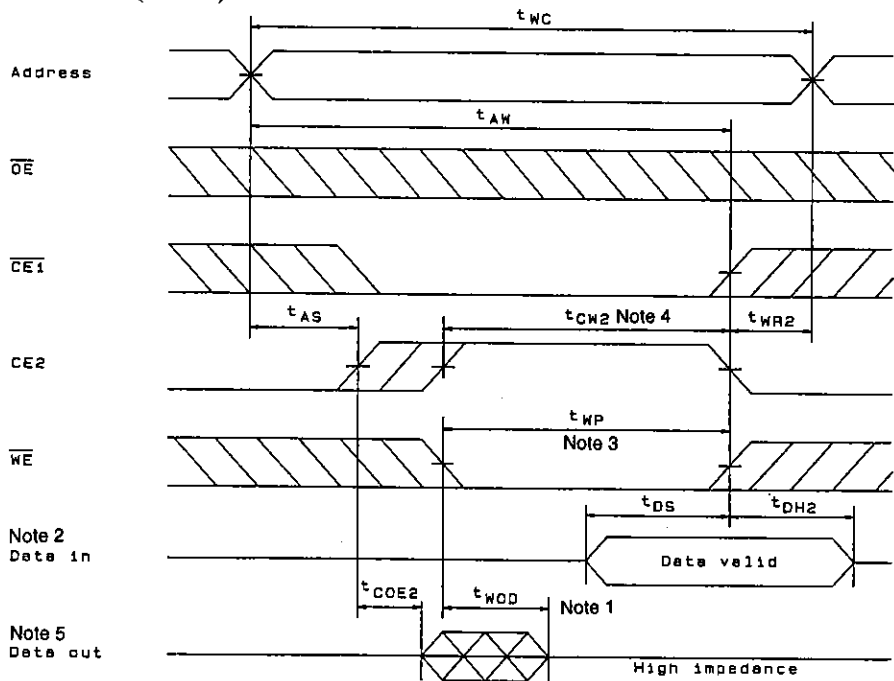
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Write Cycle (2):  $\overline{CE1}$  control (Note 6)



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Write Cycle (3):  $\overline{CE2}$  control (Note 6)



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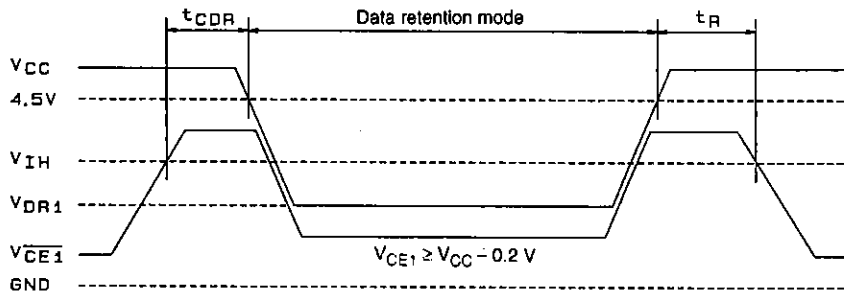
- Note: 1.  $t_{COD1}$ ,  $t_{COD2}$ ,  $t_{OOD}$ , and  $t_{WOD}$  are stipulated as the time until the outputs reach the high-impedance state, and are not determined by the output voltage levels.  
 2. Reverse phase signals must not be applied externally when the data outputs are in the output state.  
 3.  $t_{WP}$  is defined as the period when  $\overline{CE1}$  and  $\overline{WE}$  are low and  $\overline{CE2}$  is high, from the falling edge of  $\overline{WE}$  until either a rising edge of  $\overline{CE1}$  or  $\overline{WE}$  or a falling edge of  $\overline{CE2}$ , whichever of these happens first.  
 4.  $t_{WC1}$  and  $t_{WC2}$  are defined as the periods when  $\overline{CE1}$  and  $\overline{WE}$  are low and  $\overline{CE2}$  is high, from either a falling edge of  $\overline{CE1}$  or a rising edge of  $\overline{CE2}$ , until a rising edge of  $\overline{CE1}$  or  $\overline{WE}$ , or a falling edge of  $\overline{CE2}$ , whichever happens first.  
 5. The data outputs will be in the high-impedance state if either  $\overline{OE}$  is high,  $\overline{CE1}$  is high,  $\overline{CE2}$  is low, or  $\overline{WE}$  is low.  
 6. If  $\overline{OE}$  goes high during a write cycle, the data outputs will go to the high-impedance state.

Data Retention Characteristics at Ta = 0 to +70°C

Parameter	Symbol	Conditions	min	typ*	max	Unit
Data retention supply voltage	V <sub>DR1</sub>	V <sub>CE1</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>CE2</sub> ≥ V <sub>CC</sub> - 0.2 V, or V <sub>CE2</sub> ≤ 0.2 V	2.0		5.5	V
	V <sub>DR2</sub>	V <sub>CE2</sub> ≤ 0.2 V	2.0		5.5	V
Data retention supply current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3.0 V, V <sub>CE1</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>CE2</sub> ≥ V <sub>CC</sub> - 0.2 V, or V <sub>CE2</sub> ≤ 0.2 V	0 to +70°C		12	μA
			0 to +40°C		2.4	
			25°C	0.4	1.2	
	I <sub>CCDR2</sub>	V <sub>CC</sub> = 3.0 V, V <sub>CE2</sub> ≤ 0.2 V	0 to +70°C		12	μA
			0 to +40°C		2.4	
			25°C	0.4	1.2	
Chip enable setup time	t <sub>CDR</sub>		0			ns
Chip enable hold time	t <sub>R</sub>		5			ms

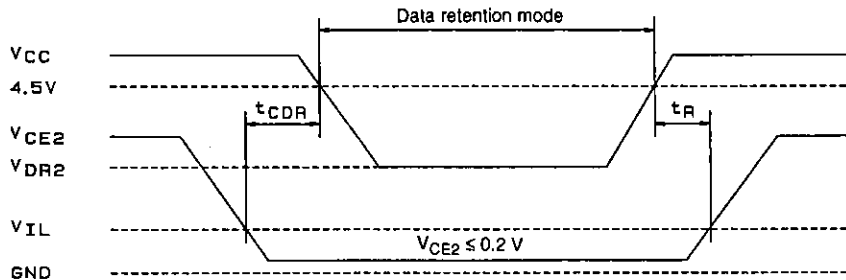
Note: \* Reference value at Ta = 25°C.

Data Retention Waveforms (1): (CE1 control)



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Data Retention Waveforms (2): (CE2 control)



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