HD74LS259 ●8-bit Addressable Latches

This 8-bit addressable latch is designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. This is multifunctional device capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

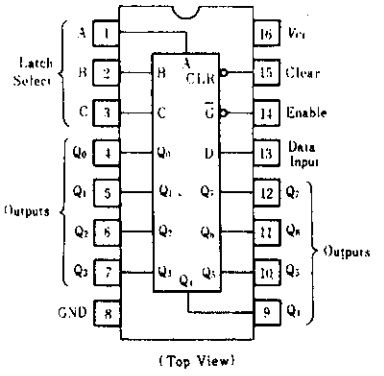
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch.

The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, latch remains in their previous states and is unaffected by the data or address inputs.

To eliminate the possibility of entering erroneous data in the latch, the enable should be held high (inactive) while the address lines are changing.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

■PIN ARRANGEMENT



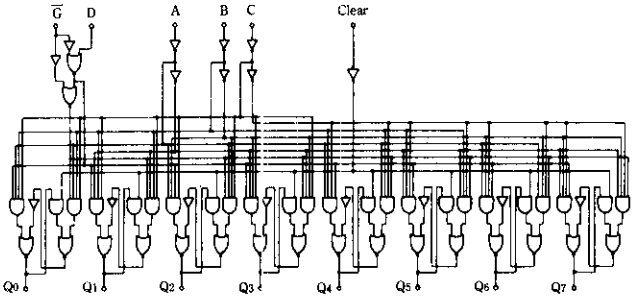
■FUNCTION TABLE

Input		Output of addressed latch	Each other output	Function
CLR	$\bar{G}$			
H	L	D	Qio	Addressable latch
H	H	Qio	Qio	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

Select inputs			Latch addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Notes) 1. H; high level, L; low level
2. D; the level at the data input
3. O_{io}; the level of Q_i (i=0, 1, ... 7, as apropriate) before the indicated steady-state input conditions were established.

■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Pulse width		t_w	15	—	—	ns
Setup time	Data	t_{su}	20 ↑	—	—	ns
	Address		20 ↑	—	—	
Hold time	Data	t_h	0 ↑	—	—	ns
	Address		0 ↑	—	—	

↑; The arrow indicates that the rising edge of the enable pulse is used for reference.

■ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2	—	—	V
	V_{IL}			—	—	0.8	V
Output voltage	V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400μA		2.7	—	—	V
	V_{OL}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V	I_{OL} = 4mA	—	—	0.4	V
			I_{OL} = 8mA	—	—	0.5	
Input current	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V		—	—	20	μA
	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V		—	—	−0.4	mA
	I_I	V_{CC} = 5.25V, V_I = 7V		—	—	0.1	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25V		−20	—	−100	mA
Supply current**	I_{CC}	V_{CC} = 5.25V		—	22	36	mA
Input clamp voltage	V_{IK}	V_{CC} = 4.75V, I_{IN} = −18mA		—	—	−1.5	V

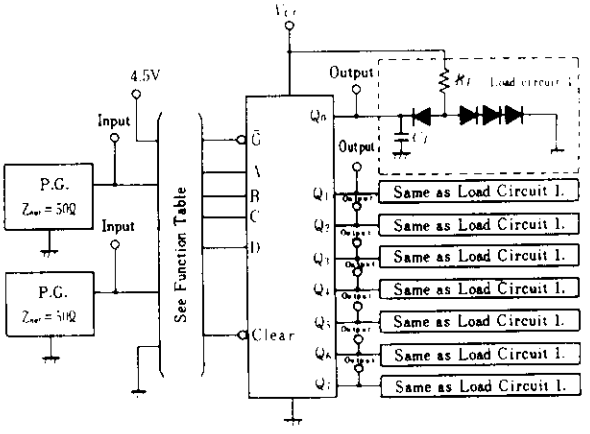
* V_{CC}=5V, Ta=25°C
** I_{CC} is measured with all outputs open and all inputs grounded.

■SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃)

Item	Symbol	Inputs	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PHL}	Clear	Q_0 ~ Q_7	C_L = 15pF, R_L = 2kΩ	—	17	27	ns
	t_{PLH}	Data	Q_0 ~ Q_7		—	20	32	ns
	t_{PHL}				—	13	21	
	t_{PLH}	Address	Q_0 ~ Q_7		—	24	38	ns
	t_{PHL}				—	18	29	
	t_{PLH}	Enable	Q_0 ~ Q_7		—	22	35	ns
	t_{PHL}				—	15	24	

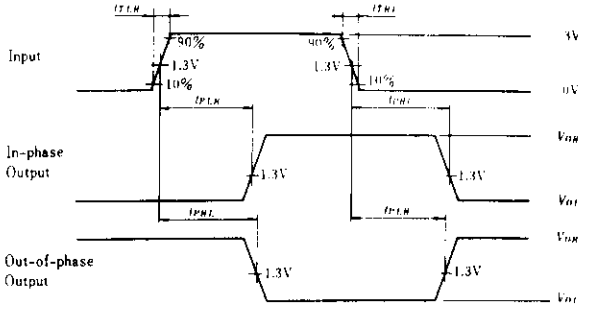
■TESTING METHOD

1) Test Circuit



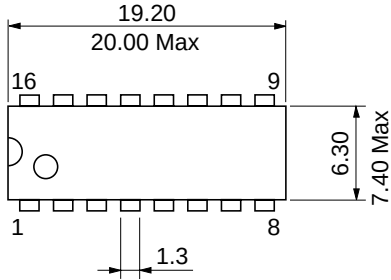
Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

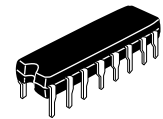
Waveform

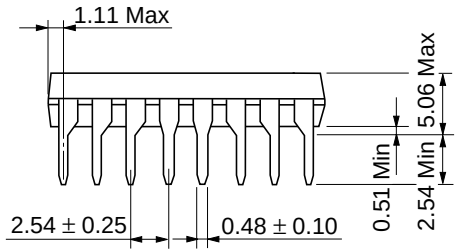


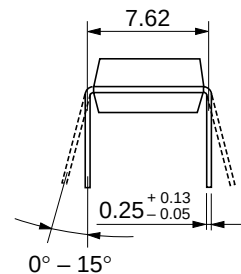
Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR=1MHz
duty cycle 50%.

Unit: mm



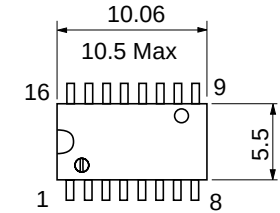


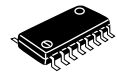


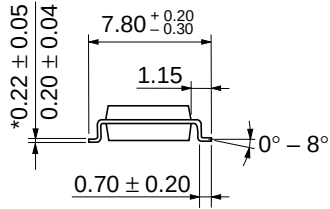


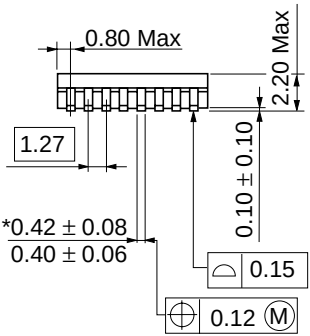
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





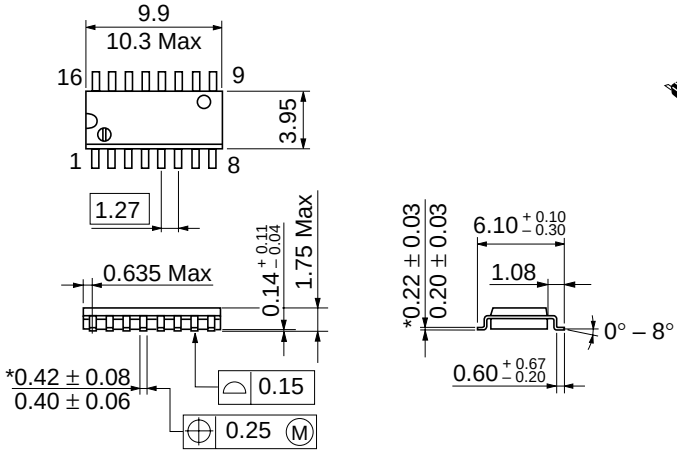


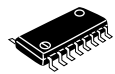


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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