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# HD74BC640A

## Octal Bus Transceivers With 3 State Outputs

# HITACHI

ADE-205-026 (Z)

Rev.0

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### Description

The HD74BC640A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC. When the frequency is 10 MHz. The device has eight bus transceivers with three state outputs in a 20 pin package. Each device has an active low enable input ( $\overline{G}$ ) and a direction control input, DiR. When DiR is high, data flows from the A inputs to the B outputs. When DiR is high, data flows from the B inputs to the A outputs. When enable inputs ( $\overline{G}$ ) is high, disables both A and B ports by placing them in a high impedance.

### Features

- Input/Output are at high impedance state when power supply is off.
- Input pins can be open, when not used, owing to built in input pull up circuit.
- Input is TTL level.
- Wide operating temperature range  
Ta = -40 to +85°C.

### Function Table

#### Control Inputs

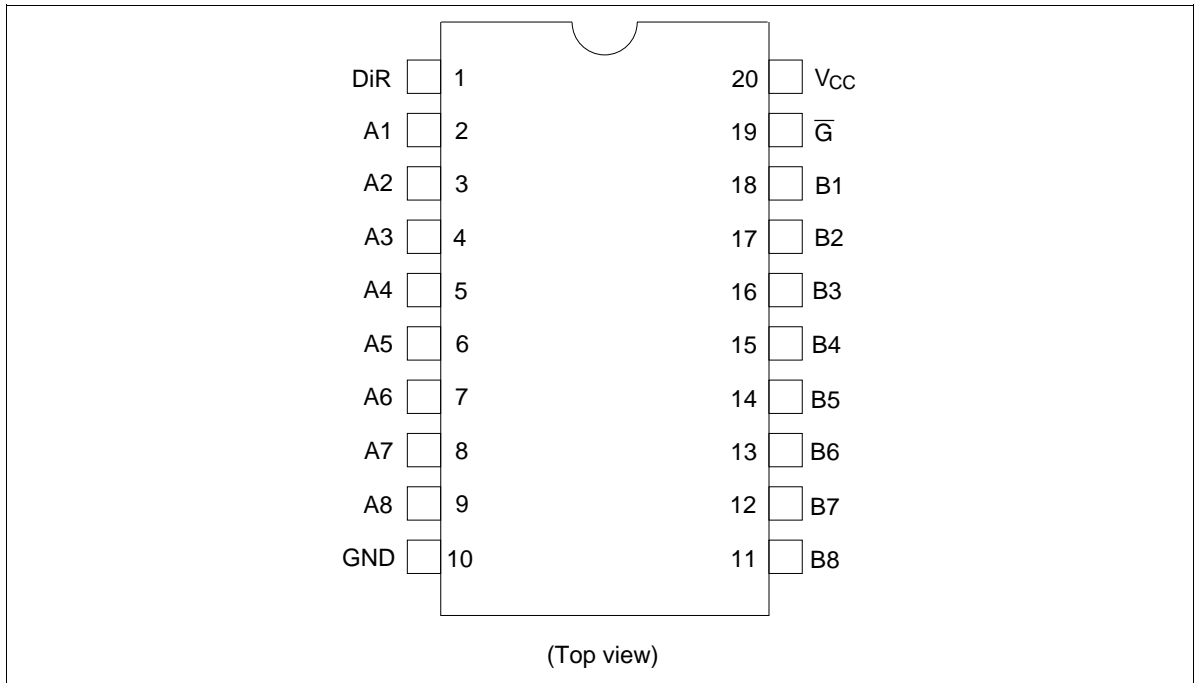
$\overline{G}$	DIR	Operation
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

H : High level

L : Low level

X : Immaterial

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	-0.5 to +7.0	V
Input diode current	$I_{IK}$	$\pm 30$	mA
Input voltage	$V_{IN}$	-0.5 to +7.5	V
Output voltage	$V_{OUT}$	-0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	-0.5 to +5.5	V
Storage temperature	Tstg	-65 to +150	°C

Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

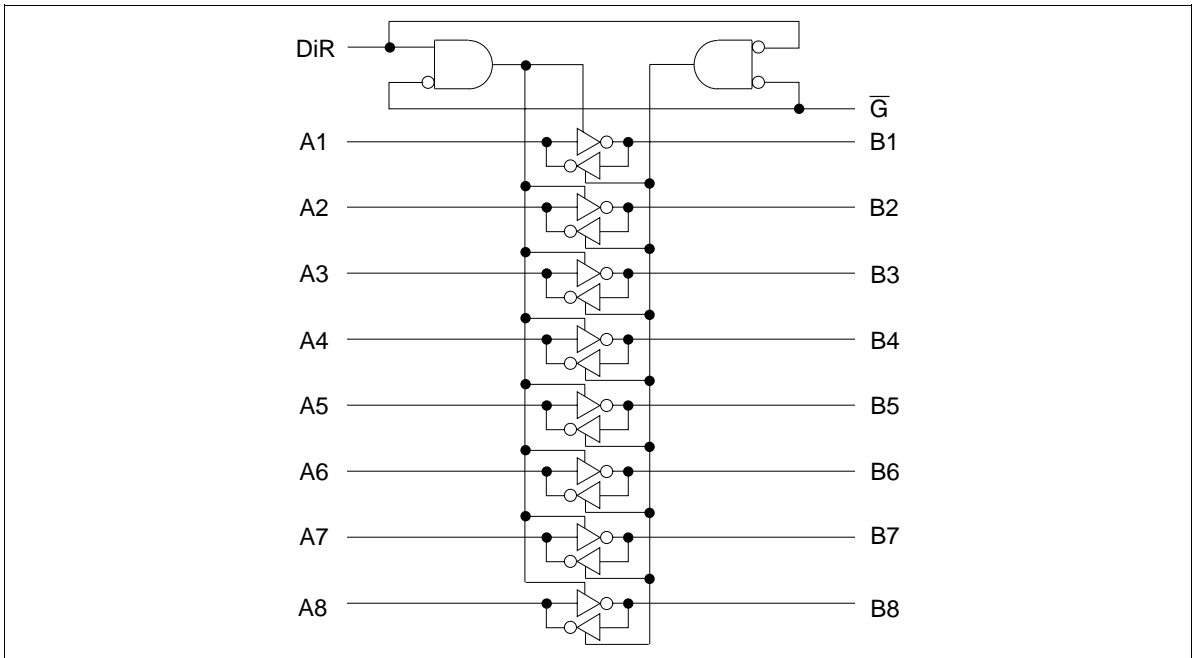
**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	$V_{IN}$	0	—	$V_{CC}$	V
Ouput voltage	$V_{OUT}$	0	—	$V_{CC}$	V
Operating temperature	$T_{opr}$	-40	—	85	°C
Input rise/fall time*1	$t_r, t_f$	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

**Logic Diagram**



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## Electrical Characteristics (Ta = -40 to +85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>		2.0	—	V	
	V <sub>IL</sub>		—	0.8	V	
Output voltage	V <sub>OH</sub>	4.5	2.4	—	V	I <sub>OH</sub> = -3 mA
		4.5	2.0	—	V	I <sub>OH</sub> = -15 mA
	V <sub>OL</sub>	4.5	—	0.5	V	I <sub>OL</sub> = 48 mA
		4.5	—	0.55	V	I <sub>OL</sub> = 64 mA
Input diode voltage	V <sub>IK</sub>	4.5	—	-1.2	V	I <sub>IN</sub> = -18 mA
Input current	I <sub>I</sub>	5.5	—	-250	μA	V <sub>IN</sub> = 0 V
		5.5	—	100	μA	An or Bn, V <sub>IN</sub> = 5.5 V
		5.5	—	1.0	μA	DiR or $\overline{G}$ , V <sub>IN</sub> = 5.5 V
		5.5	—	100	μA	DiR or $\overline{G}$ , V <sub>IN</sub> = 7 V
Output short circuit current* <sup>1</sup>	I <sub>OS</sub>	5.5	-100	-225	mA	V <sub>O</sub> = 0 V, V <sub>IN</sub> = 0 or 5.5 V
Off state output current	I <sub>OZH</sub>	5.5	—	-100	μA	V <sub>O</sub> = 2.7 V
	I <sub>OZL</sub>	5.5	—	-250	μA	V <sub>O</sub> = 0.5 V
Supply current	I <sub>CCL</sub>	5.5	—	29.5	mA	V <sub>IN</sub> = 0 or 5.5 V All outputs is "L"
	I <sub>CCH</sub>	5.5	—	2.5	mA	V <sub>IN</sub> = 0 or 5.5 V All outputs is "H"
	I <sub>CCZ</sub>	5.5	—	4.5	mA	V <sub>IN</sub> = 0 or 5.5 V All outputs is "Z"
	I <sub>CCT</sub> * <sup>2</sup>	5.5	—	1.5	mA	V <sub>IN</sub> = 3.4 or 0.5 V

Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

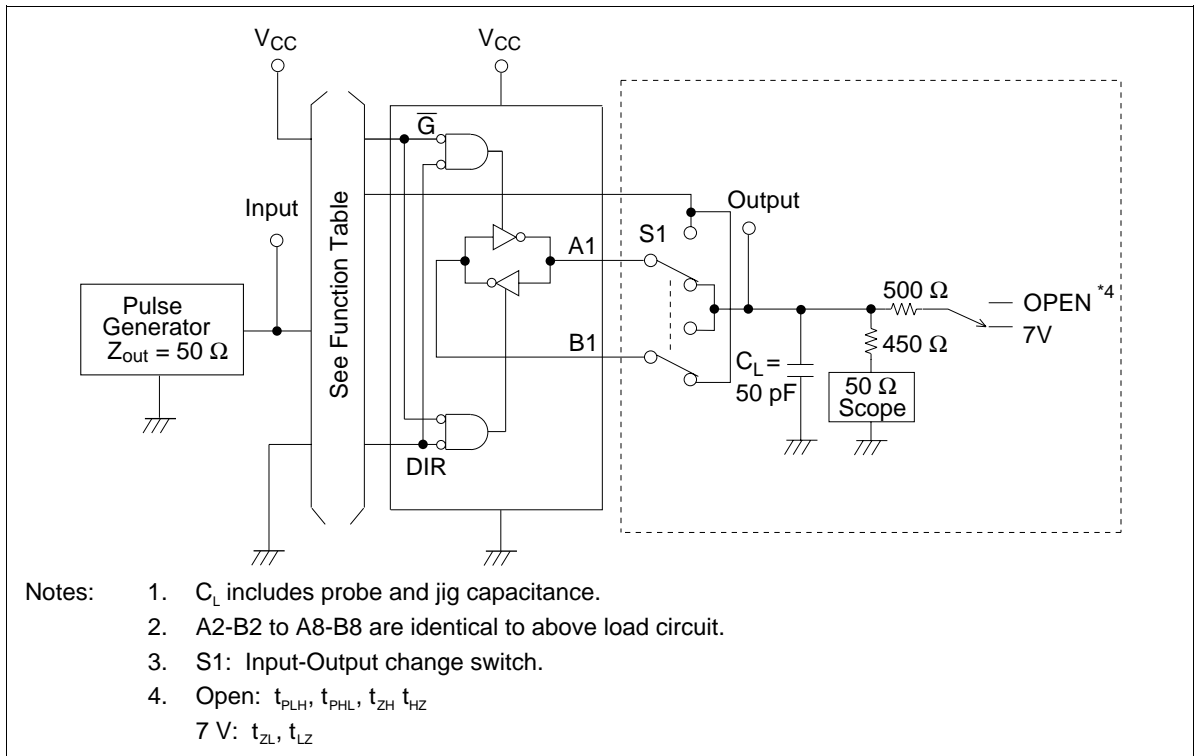
2. When input by the TTL level, it shows I<sub>CC</sub> increase at per one input pin.

**Switching Characteristics** ( $C_L = 50 \text{ pF}$ )

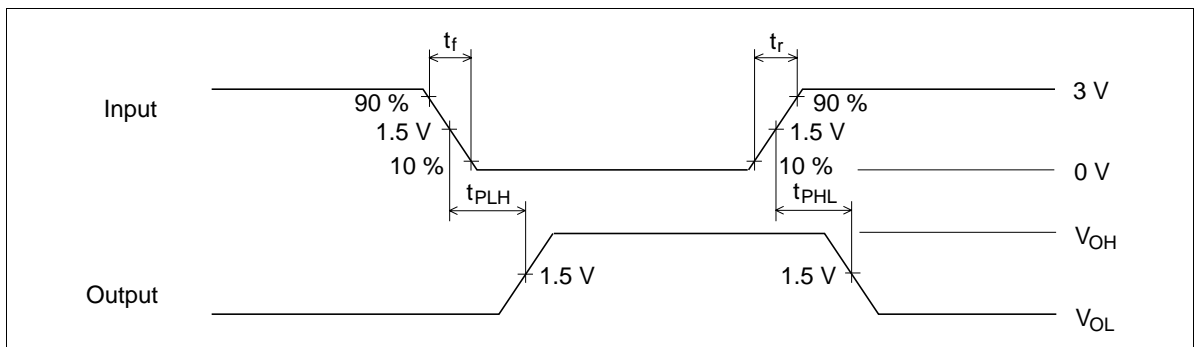
Item	Symbol	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0 \text{ V}$		$T_a = -40 \text{ to } +85^\circ\text{C}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$		Unit	Test Conditions
		Min	Max	Min	Max		
Propagation delay time	$t_{PLH}$	3.0	6.0	3.0	7.0	ns	An to Bn
	$t_{PHL}$	3.0	6.0	3.0	7.0		
	$t_{PLH}$	3.0	6.0	3.0	7.0	ns	Bn to An
	$t_{PHL}$	3.0	6.0	3.0	7.0		
Output enable time	$t_{ZH}$	3.0	9.0	3.0	11.0	ns	$\overline{G}$ to Bn
	$t_{ZL}$	3.0	9.0	3.0	11.0		
	$t_{ZH}$	3.0	9.0	3.0	11.0	ns	$\overline{G}$ to An
	$t_{ZL}$	3.0	9.0	3.0	11.0		
Output disable time	$t_{HZ}$	3.0	8.0	3.0	10.0	ns	$\overline{G}$ to Bn
	$t_{LZ}$	3.0	8.0	3.0	10.0		
	$t_{HZ}$	3.0	8.0	3.0	10.0	ns	$\overline{G}$ to An
	$t_{LZ}$	3.0	8.0	3.0	10.0		
Input capacitance	$C_{IN}$	3.0 (Typ)		—		pF	$V_{IN} = V_{CC}$ or GND
Output capacitance	$C_{IO}$	15.0 (Typ)		—		pF	$V_{IO} = V_{CC}$ or GND

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## Test Circuit

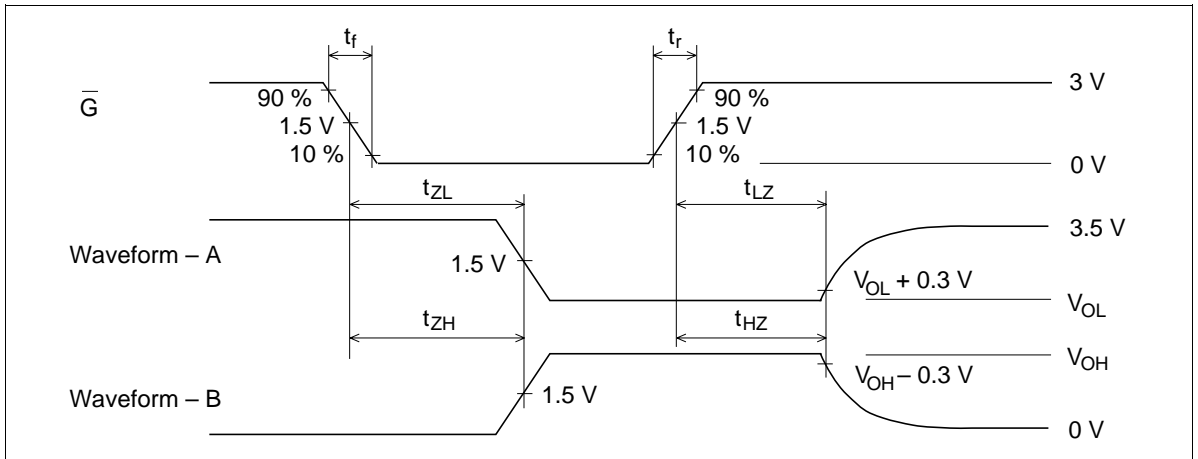


## Waveforms-1



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Waveforms-2



- Notes:
1.  $t_r = 2.5 \text{ ns}$ ,  $t_f = 2.5 \text{ ns}$
  2. Input waveforms: PRR = 1 MHz, duty cycle 50%
  3. Waveform-A shows input conditions such that the output is "L" level when enable by the output control.
  4. Waveform-B shows input conditions such that the output is "H" level when enable by the output control.

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## Package Dimensions

Unit: mm





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