élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7243C
Dual Input, High Speed, Dual Channel CCD Driver

Features
- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 20 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage— 4.5V–16V

Applications
- CCD Drivers
- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7243CM	−40°C to +85°C	20-Lead Thermal SOL	MDP0027*

General Description

The EL7243C dual input, 2-channel driver achieves the same excellent switching performance of the EL7212 family while providing added flexibility. The power package makes this part extremely well suited for high frequency and heavy loads as in CCD applications. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7243C is excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

Connection Diagram

20-Lead Thermal SOL Package
EL7243C
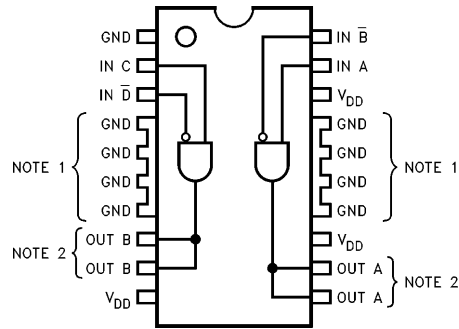
7243–1

Note 1: Pins 4–7 and 14–17 are electrically connected.
Note 2: Output pins must be tied together.

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

EL7243C
Dual Input, High Speed, Dual Channel CCD Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	20-pin "Batwing" SOIC	1500 mW
Storage Temperature Range	−65°C to +150°C		
Ambient Operating Temperature	−40°C to +85°C		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $T_A = 25°C$, $V_{DD} = 15V$ unless otherwise specified

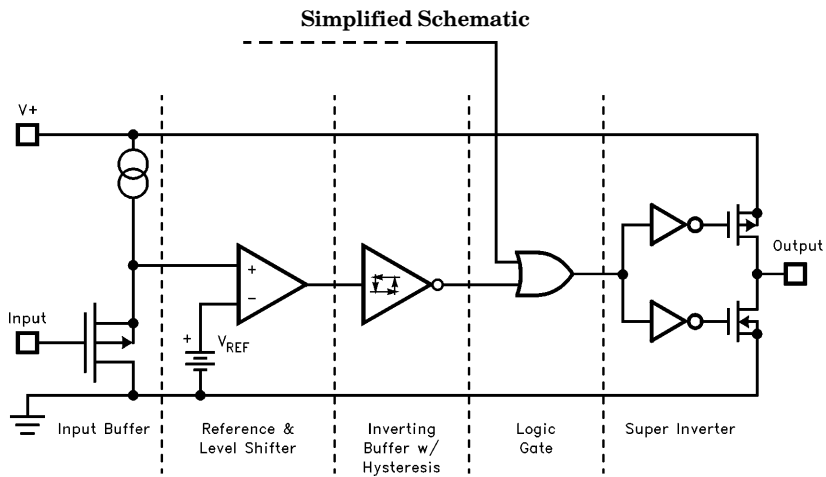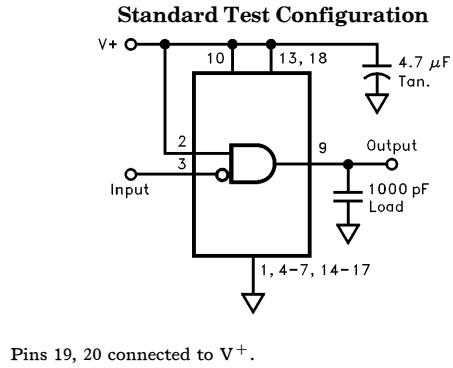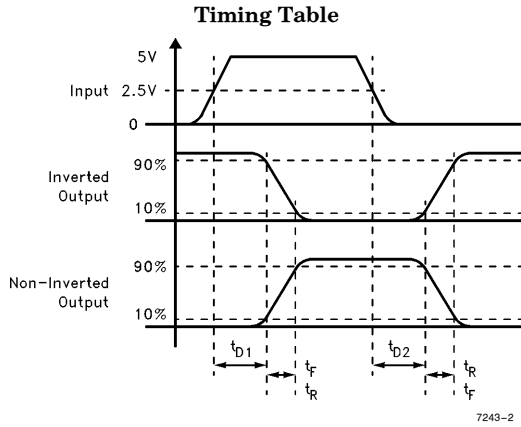| Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V_{DD}		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100\,mA$		3	6	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100\,mA$		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

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AC Electrical Characteristics $T_A = 25°C$, $V = 15V$ unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	$C_L = 500$ pF $C_L = 1000$ pF			10 20	IV	ns
t_F	Fall Time	$C_L = 500$ pF $C_L = 1000$ pF			10 20	IV	ns
t_{D-ON}	Turn-On Delay Time			20	25	IV	ns
t_{D-OFF}	Turn-Off Delay Time			20	25	IV	ns

TD is 1.5in

Timing Table

7243-2

Standard Test Configuration

Pins 19, 20 connected to V^+.

7243-3

Simplified Schematic

7243-4

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Typical Performance Curves

Max Power/Derating Curves

$\theta_{JA} = 60°C/W$

Power (W) vs Temperature (°C)

7243–5

Switch Threshold vs Supply Voltage

High Limit = 2.4V

Hysteresis

Low Limit = 0.8V

Input Voltage vs Supply Voltage

7243–6

Input Current vs Voltage

I_{IN} (mA) — 2.000/div

V_{IN} 2.500/div (V)

7243–7

Peak Drive vs Supply Voltage

V – Supply

I Sink

N–CHANNEL

P–CHANNEL

I Source

V – Supply

7243–8

Quiescent Supply Current

Supply Current (mA) vs Supply Voltage (V)

A, B, C, D, E
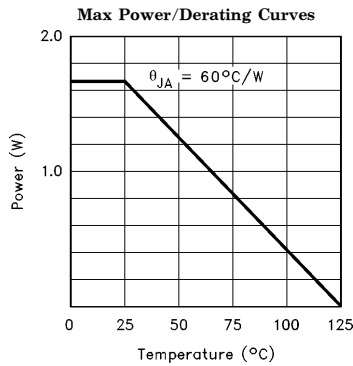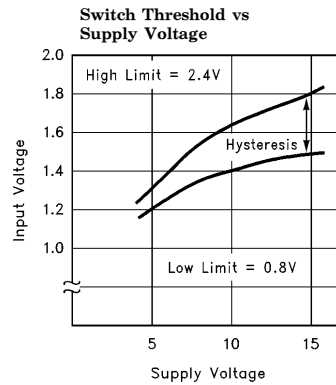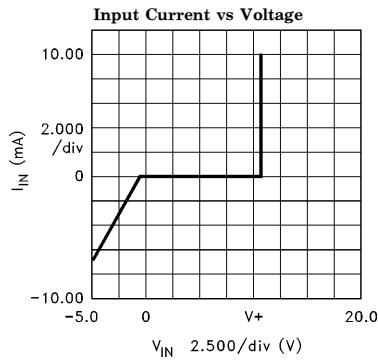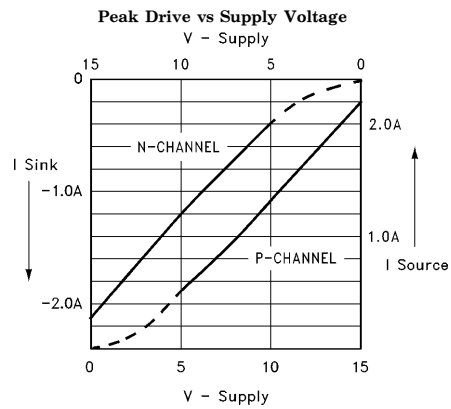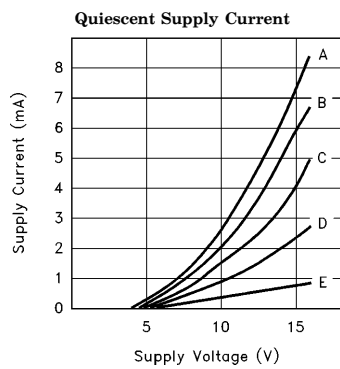
CASE:	
A	ALL INPUTS GND
B	3 INPUTS GND
C	2 INPUTS GND
D	1 INPUT GND
E	ALL INPUTS V+
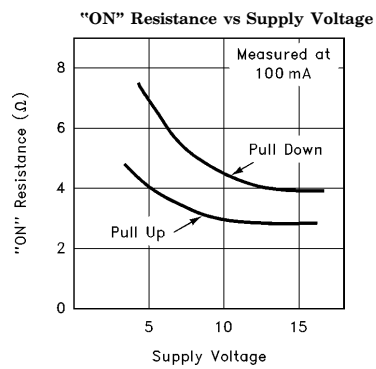
7243–9

"ON" Resistance vs Supply Voltage

Measured at 100 mA

Pull Down

Pull Up

"ON" Resistance (Ω) vs Supply Voltage

7243–10

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Typical Performance Curves — Contd.

Average Supply Current vs Voltage and Frequency

7243–11

Average Supply Current vs Capacitive Load

7243–12

Rise/Fall Time vs Load

7243–13

Rise/Fall Time vs Supply Voltage

7243–14

Typical Performance Curves — Contd.

Rise/Fall Time vs Temperature

7243-15

Propagation Delay vs Supply Voltage

7243-16

Delay vs Temperature

7243-17

6
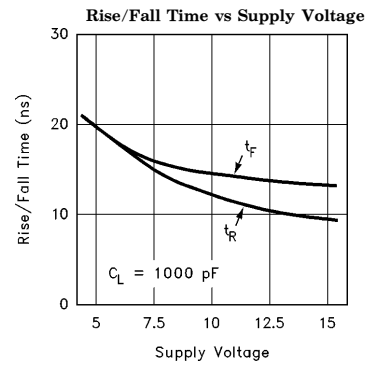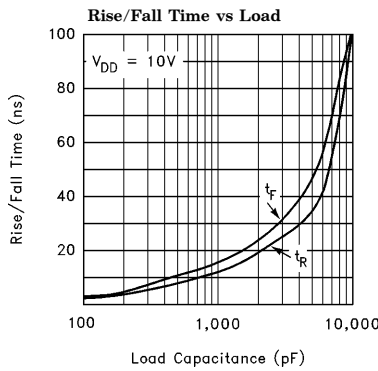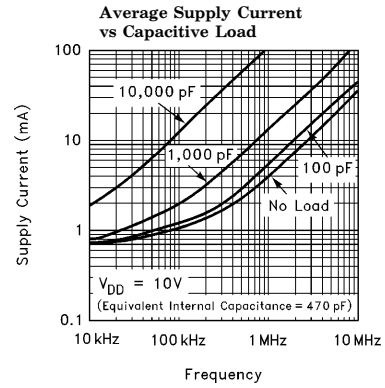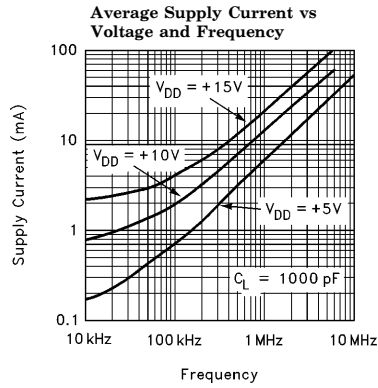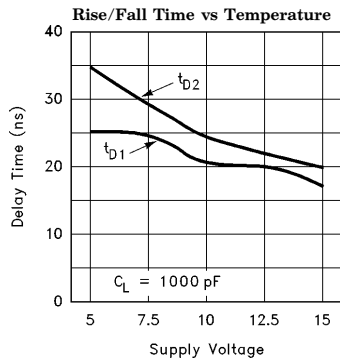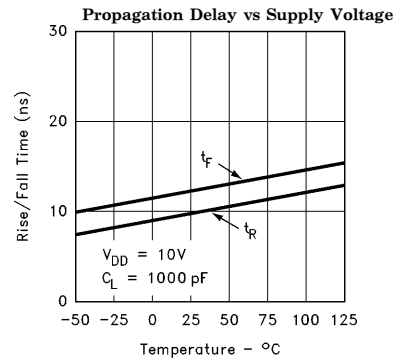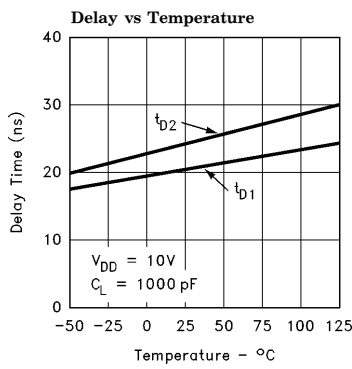
Applications Information

Typical CCD Configuration
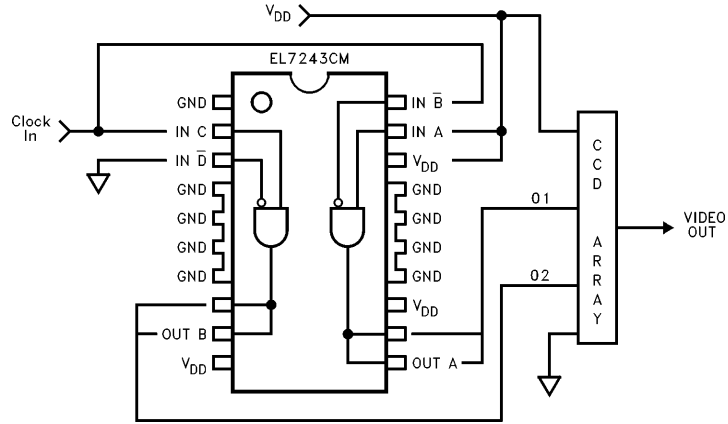
7243–18

EL7243 Macromodel

7243–19

EL7243 Macromodel

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* EL7243 Macromodel
* Revision A, January 1996
* Connections          Gnd
*                       |    Inp+
*                       |    |    Inp−
*                       |    |    |    out
*                       |    |    |    |    V_CC
.subckt M7243           1    2    3    8    10
V1 12 1 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 1 43.3pF
D1 14 13 dmod
X1 13 11 2 1 comp1
X2 16 12 15 1 comp1
V2 22 1 1.6
R6 23 25 1K
R7 24 25 5K
R8 21 22 100
C2 25 1 43.3pF
D2 24 23 dmod
X3 23 21 3 1 comp1
X4 26 25 22 1 comp1
X5 16 26 17 1 And-gate
sp 10 8 17 1 spmod
sn 8 1 17 1 snmod
g1 11 1 13 1 938u
g2 21 1 23 1 938u
.model dmod d
.model spmod vswitch ron=3 roff=2meg von=1 voff=1.5
.model snmod vswitch ron=4 roff=2meg von=3 voff=2
.ends M7243
* AND Gate Subcircuit*
.subckt And-gate inp1 inp2 out-AS Vss-A
el out-A Vss-A table {v(inp1)*v(inp2)} = (0, 3.2) (3.2, 0)
Rout-a out-a vss-a 10 meg
rinpa inp1 vss-a 10 meg
rinpb inp2 vss-a 10 meg
.ends and-gate
* Comparator Subcircuit *
.subckt comp1 out inp inm vss
el out vss table {(v(inp)−v(inm))*5000} = (0,0) (3.2, 3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends omp1
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January 1996 Rev B

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