Digital multistandard TV decoder SAA9051

FEATURES

- All operations based on a sampling frequency of 13.5 MHz, providing:
  - full adaptability to all transmission standards
  - capability for memory-based features
- Separate chrominance and luminance input (Y/C)
- CVBS input for standard applications
- CVBS throughput capability for SECAM application
- Luminance signal processing for all TV standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical synchronization detection for all standards
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals
- Requires only one crystal
- Controlled via the I²C-bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filter (NTSC)
- Wide range hue control

GENERAL DESCRIPTION

The SAA9051 digital multistandard decoder (S-DMSD) performs demodulation and decoding of all quadrature modulated colour TV standards, as well as performing luminance processing for all TV standards with CVBS or Y/C input signals.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9051	68	PLCC	plastic	SOT188AGA, CG

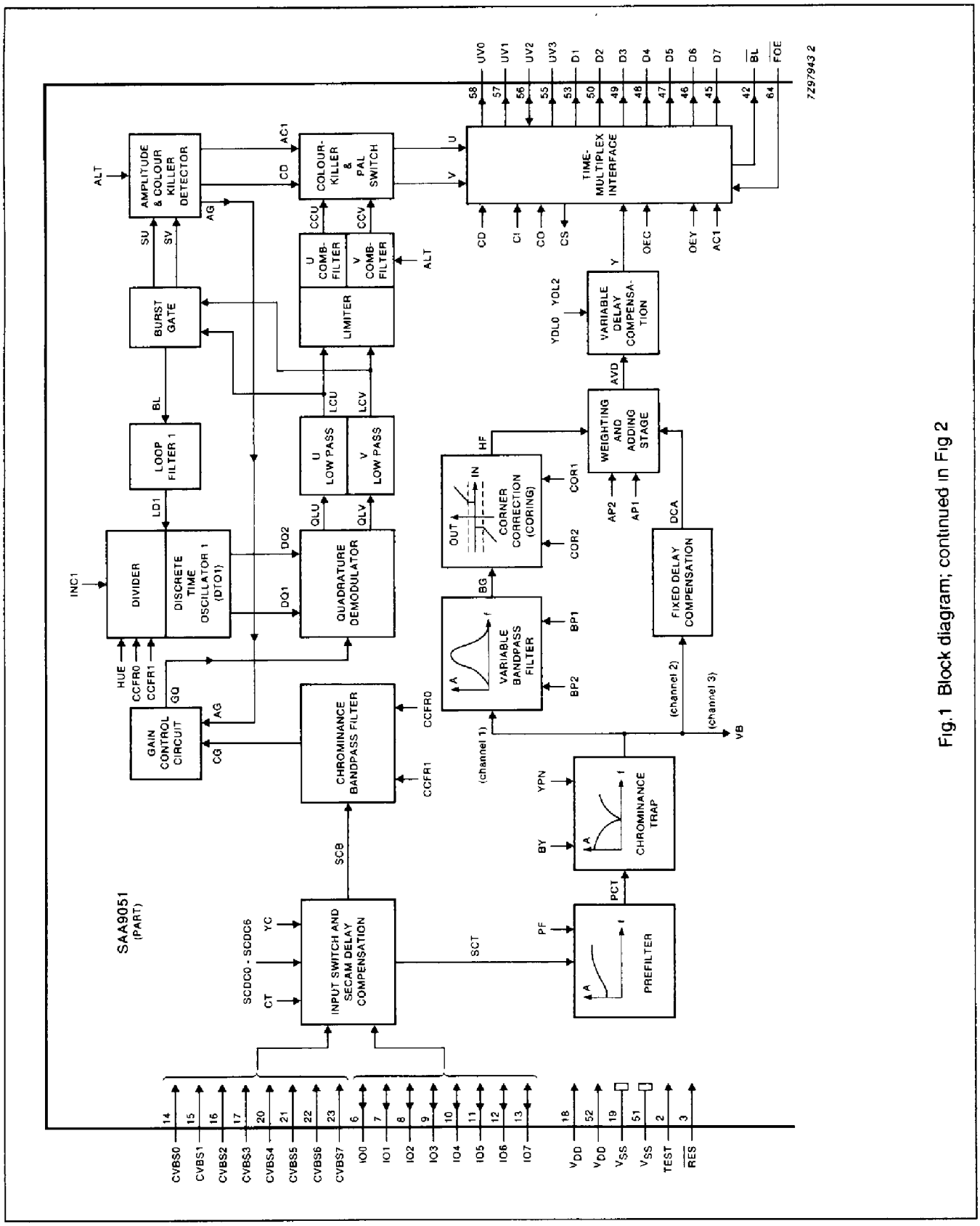


Fig.1 Block diagram; continued in Fig 2

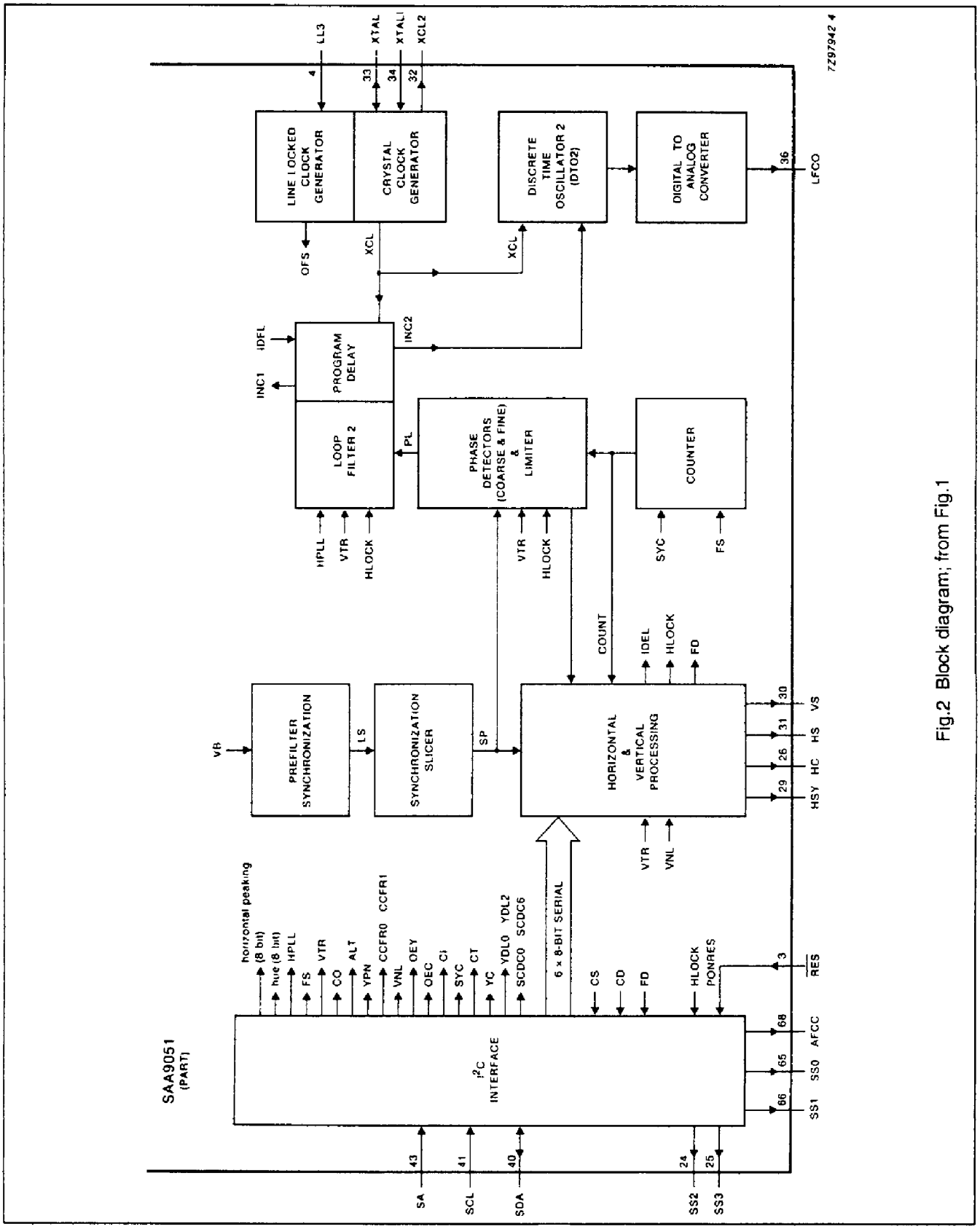


Fig.2 Block diagram; from Fig.1

PIN CONFIGURATION

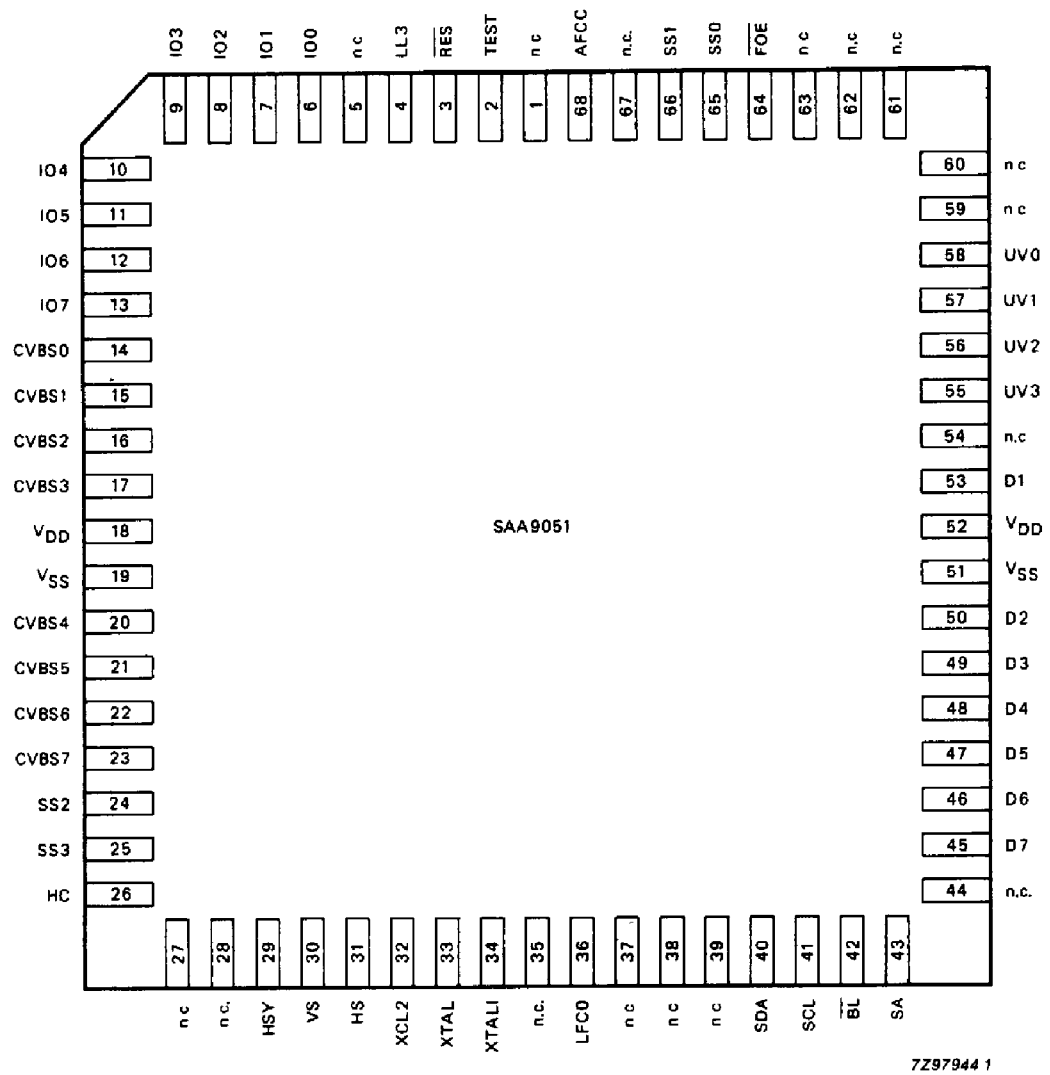


Fig.3 Pinning configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
TEST	2	test input (active HIGH); when HIGH enables scan-test mode, always connected to ground
$\overline{RES}$	3	reset input (active LOW); results in the I²C-bus control registers 1 to 3 and internal stages being reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clock cycles
LL3	4	13.5 MHz line-locked system clock
n.c.	5	not connected
IO0 (LSB) - IO7 (MSB)	6 - 13	bidirectional data path; chrominance input for separate luminance and chrominance input (Y/C) or CVBS output for SECAM decoder SAA9056. Two's complement format (IO0 is only used internally for CVBS throughput)
CVBS0 (LSB) - CVBS7 (MSB)	14 - 17, 20 - 23	digitalized composite video blanking and synchronization signals; containing luminance, chrominance and all synchronization information or luminance, blanking and synchronization signals in the event of separate luminance and chrominance (Y/C) input. Two's complement format (CVBS0 is only used internally for CVBS throughput)
V_{DD}	18	positive supply voltage (+5 V)
V_{SS}	19	ground (0 V)
SS2 - SS3	24 - 25	source select output signals; I²C-bus controlled, TTL compatible switches
HC	26	programmable horizontal output pulse; when used in conjunction with input circuits (e.g. ADC) indicates the black-level position before analog-to-digital conversion. The start and stop times are programmable, between –9.4 µs and +9.5 µs in steps of 74 ns, via the I²C-bus
n.c.	27 - 28	not connected
HSY	29	programmable horizontal output pulse; when used in conjunction with input circuits (e.g. an ADC). It indicates the synchronization pulse position before analog-to-digital conversion The start and stop times are programmable, between –14.2 µs and +4.7 µs in steps of 74 ns, via the I²C-bus
VS	30	vertical synchronization output; indicates the vertical position of the picture for 50/60 Hz field frequency

PINNING (continued)

SYMBOL	PIN	DESCRIPTION
HS	31	horizontal synchronization pulse output (duration = 64 LL3 clock cycles). HS is programmable, between −32 µs and +32 µs in steps of 300 ns, via the I²C-bus
XCL2	32	clock output; half of the crystal clock frequency (12.288 MHz). In phase with crystal (pin 33)
XTAL	33	crystal oscillator input/inverting amplifier output; input to the internal clock generator from an external oscillator or output of the inverting amplifier to an external crystal (24.576 MHz)
XTALI	34	input to the inverting amplifier from an external crystal (24.576 MHz); connect to ground if an external oscillator is used
n.c.	35	not connected
LFCO	36	line frequency control; analog output representing a multiple of the line frequency (6.75 MHz) with 4-bit resolution, the phase of which is compared to the system clock by the CGC (SAA9057A)
n.c.	37 - 39	not connected
SDA	40	I²C-bus serial data input/output
SCL	41	I²C-bus serial clock input
$\overline{BL}$	42	blanking signal output (active LOW); indicates the active video and line blanking periods. $\overline{BL}$ also synchronizes the data multiplexers/demultiplexers
SA	43	I²C-bus select address; input for selection of the appropriate I²C-bus slave address
D7 (MSB) - D1 (LSB)	45 - 50, 53	luminance data output
V_{SS}	51	ground (0 V)
V_{DD}	52	positive supply voltage (+5 V)
n.c.	54	not connected
UV3 - UV0	55 - 58	multiplexed PAL or NTSC colour difference signal output or SECAM CS input signal from the SECAM decoder. Output data format is two's complement. The multiplexer is synchronized to the rising-edge of $\overline{BL}$
n.c.	59 - 63	not connected
$\overline{FOE}$	64	fast output enable signal (active LOW); sets D1 - D7 and UV0 - UV3 outputs to the HIGH-impedance Z-state
SS0 - SS1	65 - 66	source select output signals, set via the I²C-bus; used to control the input switch (e.g. TDA8708)
n.c.	67	not connected
AFCC	68	additional output for circuit control; activated via the I²C-bus

FUNCTIONAL DESCRIPTION (see Fig.1)

The S-DMSD performs the demodulation and decoding for all quadrature modulated colour TV standards (PAL-B, G, H, I, M, N, NTSC 4.43 MHz and NTSC-M), as well as performing luminance, and parts of the synchronization, processing for TV standards (PAL, NTSC and SECAM). All of the controllable functions, user as well as factory adjustments, are accessed via I²C-bus thereby enhancing the adaptability of the digital TV concept.

Operation is based on a line-locked sampling frequency of 13.5 MHz, thus making the system fully adaptable to all line frequencies. Only one crystal is required for all TV standards.

The S-DMSD is designed to operate in conjunction with the SAA9057A Clock Generating Circuit (CGC). If the CGC is not utilized the designer must ensure:

- a reset pulse is applied to the S-DMSD after a power failure

Y/C processing

In the Y/C mode:

- The chrominance signal is input at the IO port (IO0 - IO7) and transmitted via the input switch/SECAM delay compensation circuit (multiplexer) to the chrominance bandpass filter, 'see section Chrominance path'.
- The other components, Y signal and synchronization pulse, are input via inputs CVBS0 - CVBS7 and transmitted via the input switch/SECAM delay compensation circuit to the luminance prefilter.

CVBS processing

In the CVBS mode:

- The CVBS signal is separated into its luminance (VBS) and chrominance (CG) parts by the chrominance trap and bandpass circuits. These circuits can be switched by the standard identification signals (CCFR0, CCFR1/YPN) according to the detected colour-carrier frequency, 3.58 MHz or 4.43 MHz.
- On reception of a SECAM signal the signal is transmitted to the SECAM decoder (SAA9056) via the IO port (IO0 - IO7). Bit CT enables the 3-state buffer between both parts.

Luminance path

After the chrominance trap stage (see Fig.1), the luminance path is separated into three Channels as follows:

Channel 1 signal

The Channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed (centre frequency is programmable via bits BP1 and BP2). The BC signal is transmitted to the coring (corner correction) stage where low amplitude noise is removed (amount of low amplitude noise removal is programmable via bits COR1 and COR2). The HF signal is transmitted to the weighting and adding stage, see section 'Combining Channel 1 and Channel 2 signals'.

Channel 2 signal

The Channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black-level adjustment occurs. The DCA signal is transmitted to the weighting and adding stage, see section 'Combining Channel 1 and Channel 2 signals'.

Combining Channel 1 and Channel 2 signals

The Channel 1 HF signal is weighted and added to the Channel 2 DCA signal. The combined signals are matched to the specified amplitude and the word size is reduced to 7 bits. The AVD signal is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from –4 to +3 LL3 clock cycles, see note) via bits YDL0 - YDL2. The Y signal is transmitted to the time multiplexed interface where the signal is output via D1 - D7.

Channel 3 signal

The Channel 3 VB signal is transmitted to the prefilter synchronization stage, see section 'Synchronization path'.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

Chrominance path (see Fig.1)

The chrominance CG signal is transmitted from the chrominance bandpass stage to the gain control circuit (see note 1). The gain control stage ensures that the chrominance signal has constant burst amplitude. The GQ signal is transmitted to the quadrature demodulator, where demodulation of the quadrature modulated chrominance GQ signal to colour difference signals occurs.

The QLU and QLV signals are transmitted to a low-pass filter. The LCU and LCV signals are transmitted to the limiter and comb-filter stage. The comb-filter stage (see note 2) separates the remaining vertically correlated luminance components for NTSC (for PAL, the signals are phase corrected). The CCU and CCV signals are transmitted to the colour-killer and PAL switch stage (see note 3). At this stage signals which do not comply with the selected standard are removed. In the PAL mode this stage restores the correct phase of the V signal. The signals are then transmitted to the time multiplexed interface and output via UV0 - UV3.

Notes

1. The gain control stage is controlled by the AG signal which is derived from the amplitude and colour-killer detector stage (ACKD). A non-standard burst-to-amplitude ratio results in the automatic colour-leveling stage functioning as an amplitude detector to ensure correct amplitude and avoid overflow/limiter defects.
2. The comb-filter can be altered from alternate to non-alternate mode by the ALT signal.
3. The colour-killer and PAL switching stages are controlled by the amplitude and colour-killer detection circuit using the AC1 and CD signals.

COLOUR-CARRIER FREQUENCY REGENERATION

The regeneration of the colour-carrier frequency is performed by the phase-locked-loop (PLL) which comprises a quadrature demodulator, low-pass filter, burst gate, loop filter 1 and divider/discrete time oscillator (DTO1). The DTO1 is controlled by the standard identification signals CCFR0 - CCFR1 and the Hue signal which influences the demodulation phase of the chrominance signal.

Synchronization path

In the synchronization circuit, prefilter synchronization is implemented to normalize the synchronization pulse slopes. A synchronization-slicer provides the detected synchronization pulses (SP) to the horizontal and vertical processing and phase detector stages.

HORIZONTAL AND VERTICAL PROCESSING

The horizontal and vertical processing comprises part of a PLL circuit for regeneration of the horizontal synchronization (HS) and an adaptive filter for detection of the vertical synchronization (VS). The horizontal and vertical processing also generates:

- coincidence signal (HLOCK) which controls the mute function
- standard identification signal (FD) which identifies nominal 525 or 625 lines per picture.

PHASE DETECTORS

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a variable bandwidth, dependent on the time constant signal (VTR), generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment delay signal (IDEL). INC1 corrects the regenerated subcarrier frequency at DTO1 and INC2 performs phase incrementing of DTO2. The crystal clock generator provides a stable 24.576 MHz clock input to DTO2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429 times the line frequency. The analog output LFCO, from the DAC, is transmitted to the SAA9057A (CGC).

Output interface

The signals OEY, OEC, CO, CI and CD control the output interface (see Fig.6). All but one of these signals are received via the I²C-bus, except the CD signal which is detected in the S-DMSD. A power-ON reset results in these signals being set to zero.

Table 1 Vertical Noise limiter (VNL) signal

VNL	OUTPUT
0	VNL bypassed
1	VNL active

Table 2 CO, CI and CD signals

CO	CI	CD	OUTPUTS	OUTPUT STATUS
0	X	X	UV0 - UV3	colour OFF (zero)
1	0	0	UV0 - UV3	colour OFF (controlled by CD)
1	0	1	UV0 - UV3	colour ON (controlled by CD)
1	1	X	UV0 - UV3	colour forced ON

Where:

X = don't care.

Table 3 OEC, OEY, $\overline{FOE}$, $\overline{BL}$, D1 - D7 and UV0 - UV3 signals

OEC	OEY	$\overline{FOE}$	$\overline{BL}$, VS, HS	D1 - D7	UV0 - UV3	REMARKS
0	0	X	HIZS	HIZS	HIZS	status after power-ON reset
1	1	1	active	HIZS	HIZS	
1	1	0	active	active	active	
0	1	1	active	HIZS	HIZS	
0	1	0	active	active	active	

Where:

X = don't care
HIZS = HIGH-impedance Z-state.

Note to Table 3

Combinations other than those shown in Table 3 are not allowed.

$\overline{FOE}$ signal

In PIPCO (picture-in-picture controller, SAA9068) applications, the PIPCO requires access to the digital YUV-bus on a pixel time-base. This requirement is catered for by PIPCO generated signal $\overline{FOE}$, which forces all data output of the S-DMSD and DSD (SAA9056) into the HIGH-impedance Z-state. The $\overline{FOE}$ signal does not affect the synchronization data lines (HS and VS) or the blanking data line ($\overline{BL}$), see Fig.7.

CS signal

The CS signal is transmitted from the digital SECAM decoder (DSD) during the horizontal-blanking period and is received via the UV2 input (see Fig.6). The CS bit is read by the S-DMSD once per line at LL3 clock cycle number 748 (see Fig.8).

I²C bus interface (see Tables 1 to 3)

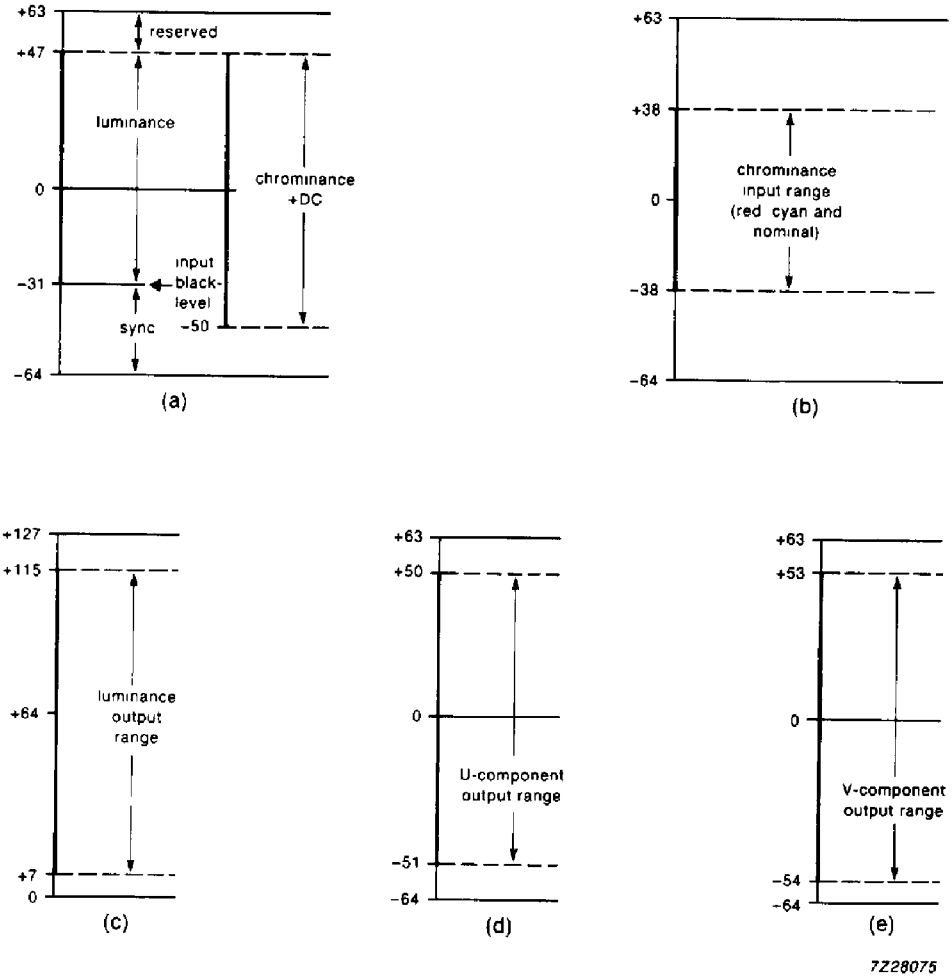
The following control signals are received via the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, YPN)
- video recorder/TV time constant (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)

- increment-delay (IDEL)
- luminance aperture-correction control (BY, PF, BP1, BP2, COR2, COR1, AP2, AP1)
- luminance delay compensation (YDL0, YDL1, YDL2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON, test purposes only (CI)
- vertical noise limiter (VNL) active/bypassed
- luminance and sync output enable (OEY)
- chrominance output enable (OEC)
- switch signals (source select signals SS0, SS1, SS2, SS3)
- additional output for circuit control (AFCC)
- chrominance source select CVBS/chrominance input/output (CT/YC).
- SECAM chrominance delay compensation (SCDC0, SCDC1, SCDC2, SCDC3, SCDC4, SCDC5, SCDC6).
- horizontal sync (HSY) and clamp (HC) pulse disable (SYC).

Signals transmitted from the S-DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- power-on-reset of S-DMSD (PONRES).



(a) CVBS1 to CVBS7 input range
(b) IO1 to IO7 input range
(c) Y output range
(d) U output range (B–Y)
(e) V output range (R–Y)

Fig.4 Diagram showing input/output range of the S-DMSD; all levels in EBU colour bar, values in binary, 100% luminance and 75% chrominance amplitude.

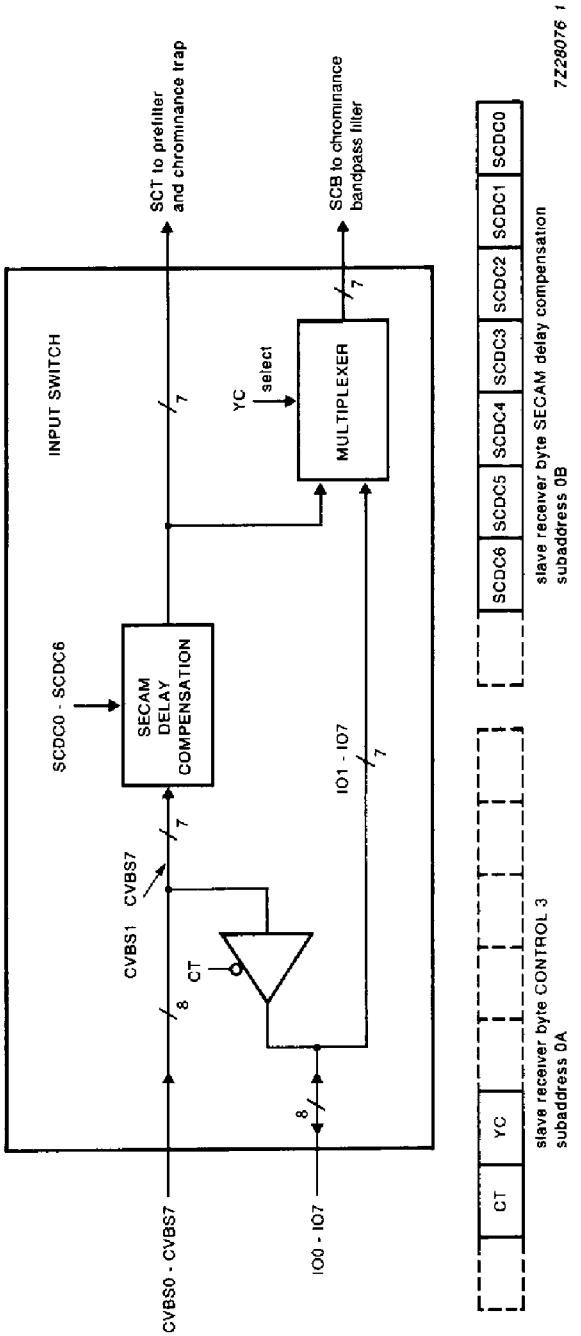


Fig.5 Schematic diagram of the input switch.

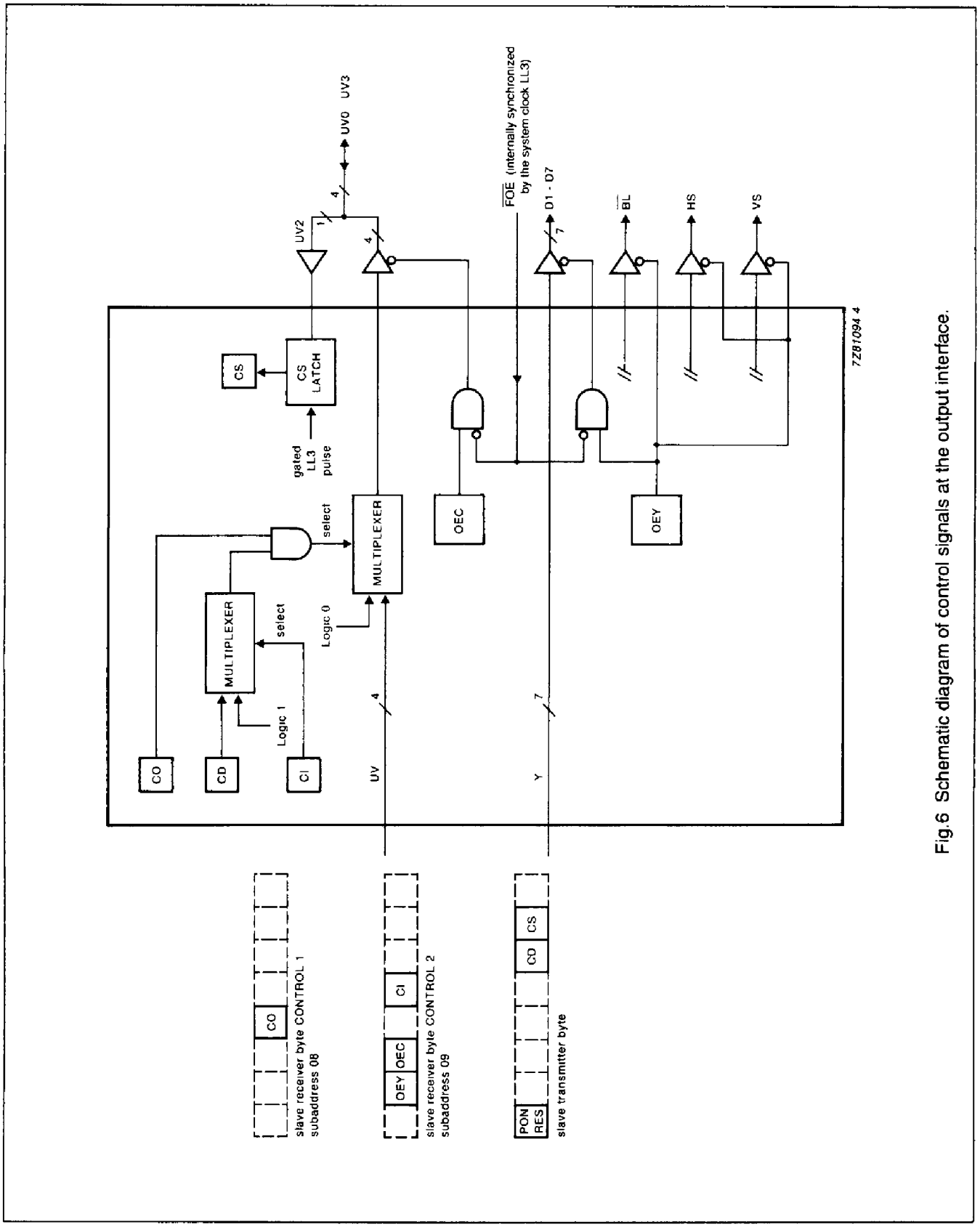


Fig.6 Schematic diagram of control signals at the output interface.

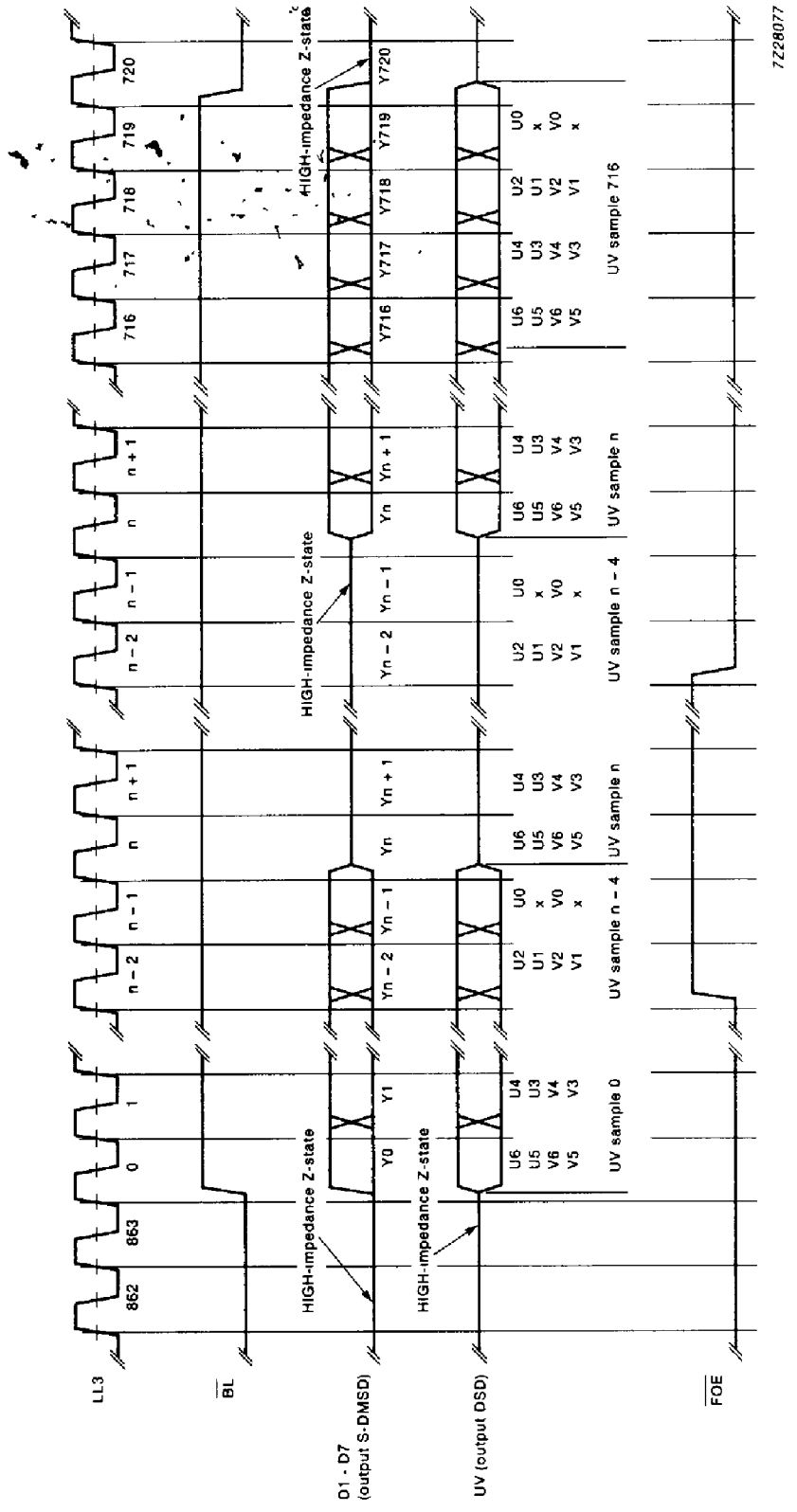


Fig.7 Timing waveform of the output data and $\overline{FOE}$ signals.

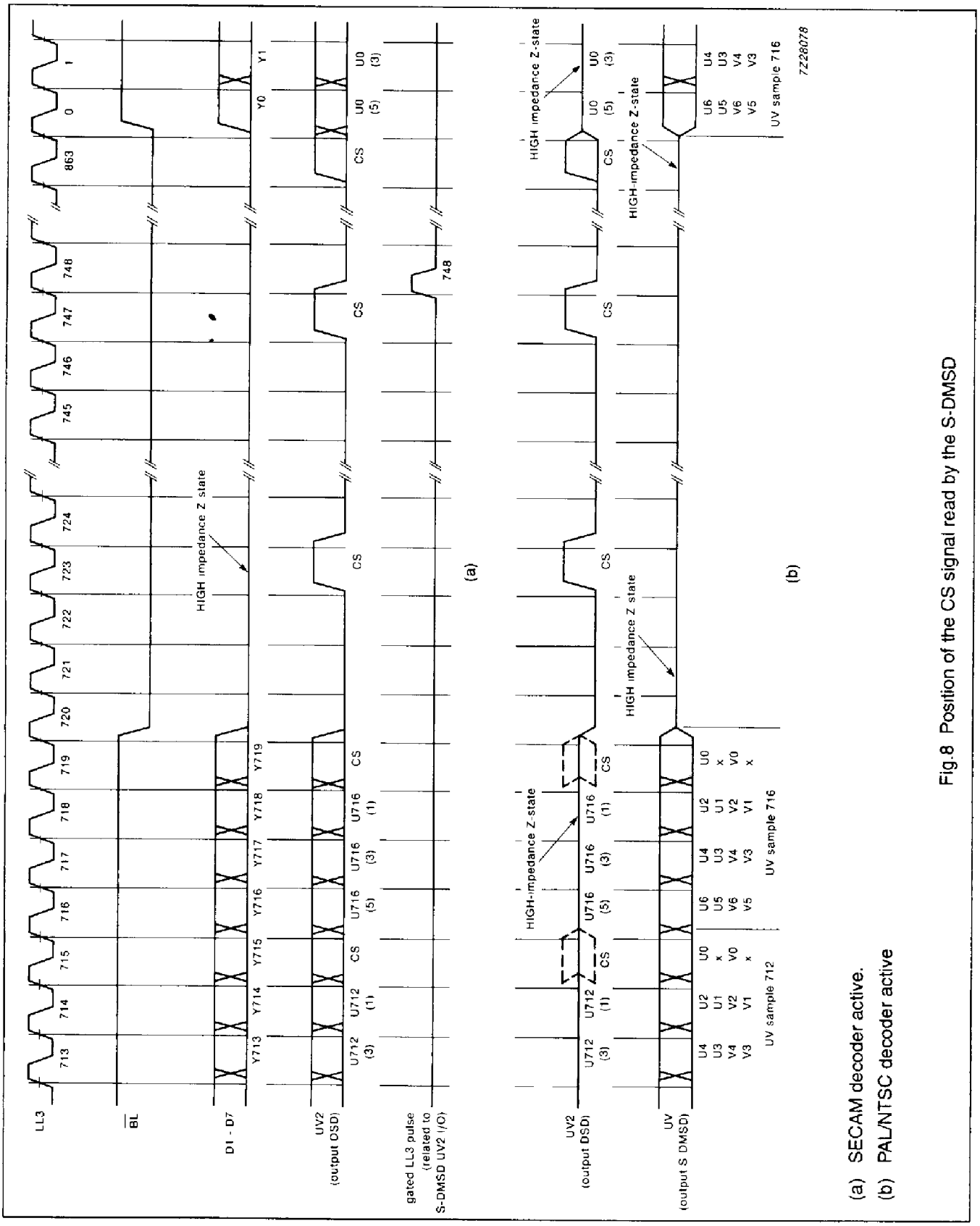


Fig.8 Position of the CS signal read by the S-DMSD

(a) SECAM decoder active.

(b) PAL/NTSC decoder active

Table 4 Slave addresses

SLAVE RECEIVER ADDRESS									REMARKS
SA	A6	A5	A4	A3	A2	A1	A0	*	
0	1	0	0	0	1	0	1	0	binary value (8A hex)
1	1	0	0	0	1	1	1	0	binary value (8E hex)

Where:

* = logic 0, receiver mode
* = logic 1, transmitter mode.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

There are two slave addresses, programmable via input SA, which determine the operating mode of the S-DMSD, see Table 4.

Table 5 Subaddress byte and data byte formats

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
HS start time (after PHI1)	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	BY	PF	BP2	BP1	COR2	COR1	AP2	AP1
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	VNL	OEY	OEC	X	CI	AFCC	SS1	SS0
Control 3	0A	SYC	CT	YC	SS3	SS2	YDL2	YDL1	YDL0
SECAM delay compensation	0B	X	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
Reserved	0C - 0F	X	X	X	X	X	X	X	X

Where:

X = don't care.

Notes to Table 5

1. The subaddress is automatically incremented. This enables quick initialization, within one transmission, by the I²C-bus controller.
2. The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9056) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
3. After power-on-reset the control registers 1 to 3 (subaddresses 08, 09 and 0A) are, with the exception of bits YDL0 - YDL2 of counter 3, set to logic 0. All other registers are undefined.
4. Prior to a reset of the IC all outputs are undefined.
5. The least significant bit of an analog control or alignment register is defined as AX0.

SUBADDRESS 00

Table 6 Increment delay control IDEL (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS*							
		A07	A06	A05	A04	A03	A02	A01	A00
−1 to −110	−148 ns (min. value)	1	1	1	1	1	1	1	1
	−16.3 µs (outside available range)	1	0	0	1	0	0	1	0
−111 to −214	−16.44 µs	1	0	0	1	0	0	0	1
	−31.7 µs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
−215	−31.85 µs (outside central counter range if FS = logic 1)**	0	0	1	0	1	0	0	1
−216	−32 µs (max. value if FS = logic 0)**	0	0	1	0	1	0	0	0
−217 to −256	−32.148 µs (outside central counter if FS = logic 0)**	0	0	1	0	0	1	1	1
	−37.9 µs (outside central counter)**	0	0	0	0	0	0	0	0

Where:

* A sign bit, designated A08 and internally set to HIGH, indicate values are always negative.

** The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within ± 7.1% of the nominal frequency.

SUBADDRESS 01

Table 7 Horizontal synchronization HSY start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A17	A16	A15	A14	A13	A12	A11	A10
+191 to +1	−14.2 µs (max. negative value) to −0.074 µs	1 to 0	0 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −64	+0.074 µs to +4.7 µs (max. positive value)	1 to 1	1 to 1	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0

SUBADDRESS 02

Table 8 Horizontal synchronization HSY stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A27	A26	A25	A24	A23	A22	A21	A20
+191 to +1	−14.2 µs (max. negative value) to −0.074 µs	1 to 0	0 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −64	+0.074 µs to +4.7 µs (max. positive value)	1 to 1	1 to 1	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0

SUBADDRESS 03

Table 9 Horizontal clamp HC start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A37	A36	A35	A34	A33	A32	A31	A30
+127 to +1	−9.4 µs (max. negative value) to −0.074 µs	0 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 0	1 to 1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 µs to +9.5 µs (max. positive value)	1 to 1	0 to 0	0 to 0	0 to 0	0 to 0	0 to 0	0 to 0	0 to 0

SUBADDRESS 04

Table 10 Horizontal clamp HC stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A47	A46	A45	A44	A43	A42	A41	A40
+127 to	−9.4 µs (max. negative value)	0	1	1	1	1	1	1	1
+1	−0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to	+0.074 µs	1	1	1	1	1	1	1	1
−128	+9.5 µs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 05

Table 11 Horizontal synchronization HS start time after PHI1 (application dependent); 50 Hz; 625 lines (FS = 0)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+127 to	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
+109	forbidden; outside available central counter range	0	1	1	0	1	1	0	1
+108 to	−32 µs (max. negative value)	0	1	1	0	1	1	0	0
+1	−0.296 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to	+0.296 µs	1	1	1	1	1	1	1	1
−107	+31.7 µs (max. positive value)	1	0	0	1	0	1	0	1
−108 to	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
−128	forbidden; outside available central counter range	1	0	0	0	0	0	0	0

Table 12 Horizontal synchronization start time after PHI1 (application dependent); 60 Hz; 525 lines (FS = 1)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+127 to	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
+107	forbidden; outside available central counter range	0	1	1	0	1	0	1	1
+106 to	−31.8 µs (max. negative value)	0	1	1	0	1	0	1	0
+1	−0.294 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to	+0.294 µs	1	1	1	1	1	1	1	1
−107	+31.5 µs (max. positive value)	1	0	0	1	0	1	0	1
−108 to	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
−128	forbidden; outside available central counter range	1	0	0	0	0	0	0	0

Programming IDEL, HSY, HC and HS

The variables IDEL, HSY, HC and HS are programmed using data words via the I²C-bus. In the following examples a decrease in value corresponds to an increase in time.

IDEL (SEE FIG.9)

The IDEL data word compensates for the time delays in data processing between loop filter 2, quadrature demodulator and internal/external (system) signal paths. The internal delay (t_{REF}) is the period required for INC1 to pass from loop filter 2, through the divider and DTO1. This delay corrects the relationship between the subcarrier frequency and the line frequency. The external path is a result of the following time delays (time delay is given in term of LL3 clock cycles):

- t_{IDEL}; programmable delay time
- t_a; processing time of DTO2 and the DAC
- t_b; chrominance bandpass and gain control stage delay times
- t_{CGC}; clock generator circuit delay time
- t_{ADC}; analog-to-digital converter delay time
- t_{INP}; input switch delay time.

As delay t_a and t_b are known constants, t_{IDEL} is programmed in the range of −115 to −214/216 LL3 clock cycles, as follows:

- $t_{IDEL} = -115 - 0.5 (* - t_{CGC} - t_{ADC} - t_{INP})$.

* Value to be fixed.

HSY

Referring to Fig.10 point (1) and periods a and b:

- HSY start time = $t_{(1)}$ − a (LL3 clock cycles)
- HSY stop time = $t_{(1)}$ − b (LL3 clock cycles)

Programming range of HSY start/stop time: +191 to −64 (LL3 clock cycles).

HC

Referring to Fig.10 point (1) and periods c and d:

- HC start time = $t_{(1)}$ − c (LL3 clock cycles)
- HC stop time = $t_{(1)}$ − d (LL3 clock cycles)

Programming range of HC start/stop time: +127 to −128 (LL3 clock cycles).

HS

The HS reference positions in PAL and NTSC modes are shown in Fig.10 at points (3) and (4) respectively. To move the HS pulse to the centre of blanking pulse $\overline{BL}$ the following equation is used:

- HS (NTSC):

  position of HS relative to the zero point (LL3 clock cycles) 4 LL3 clock cycles
- HS (PAL):

  position of HS relative to the zero point (LL3 clock cycles) 4 LL3 clock cycles

The length of HS is 64 LL3 clock cycles.

Programming of the luminance path of the S-DMSD

The VBS (without chrominance) or CVBS input signal enters the prefilter (a high-pass transfer function with maximum gain of 9.5 dB). The control bit PF switches the filter into the bypass mode. The next stage is the chrominance trap which can be programmed (zero point) to 4.43 MHz (PAL) or 3.58 MHz (NTSC) by the control bit YPN. Bit BY activates the bypass function for the Y/G mode of the S-DMSD. The chrominance trap output signal is then divided into three Channels as described in section 'Luminance path'.

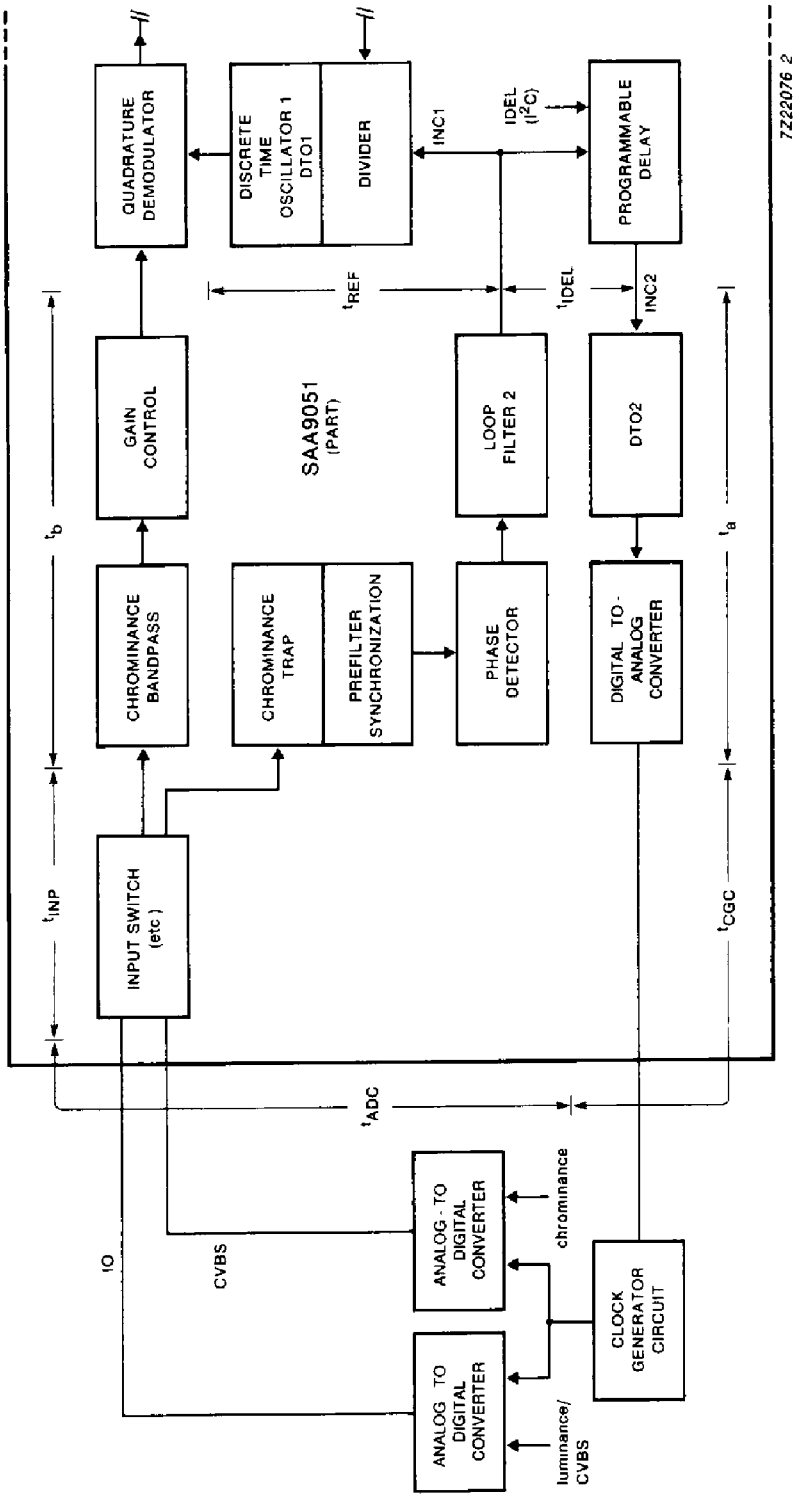
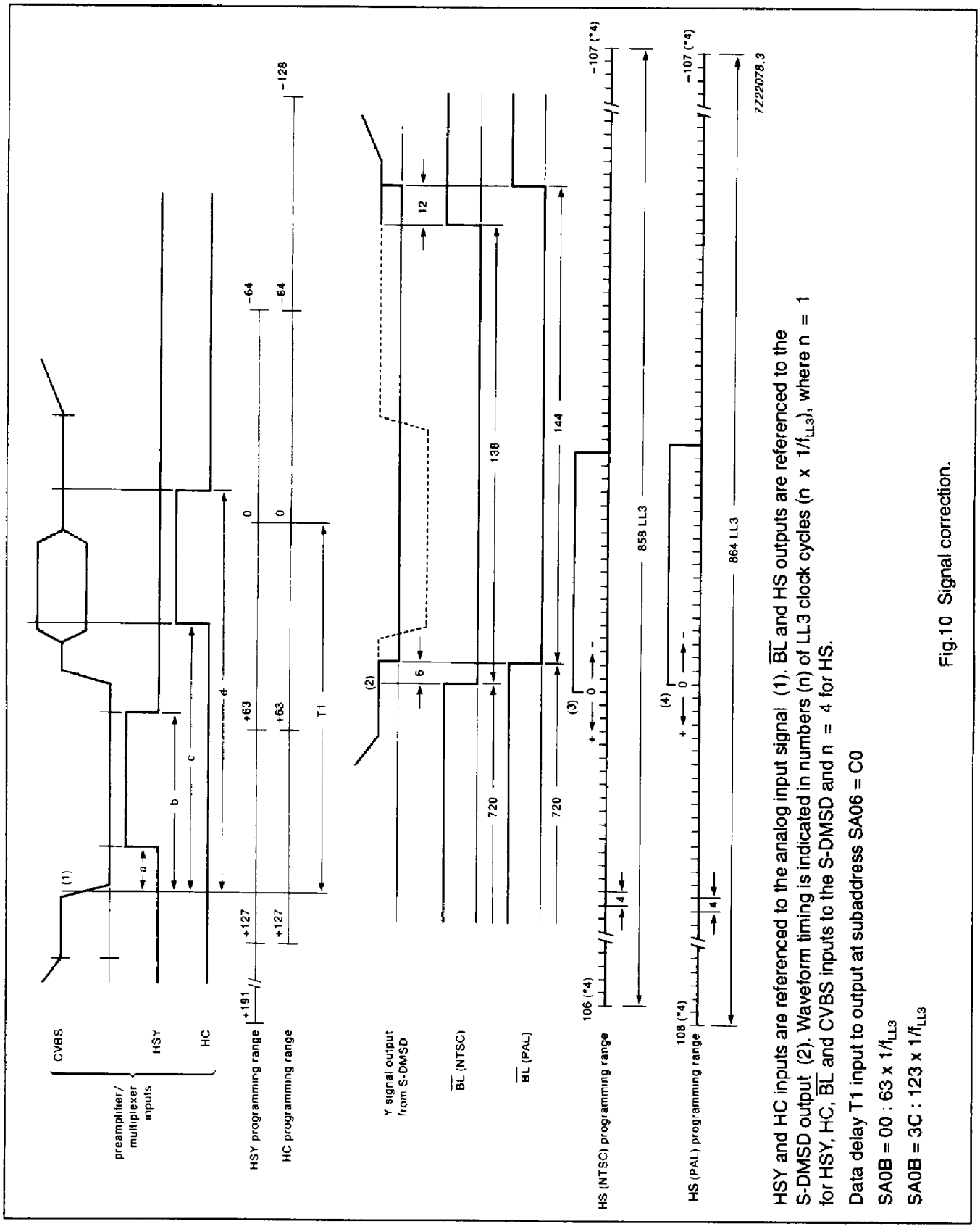


Fig.9 Compensation of delay times by incrementing delay control IDEL.



HSY and HC inputs are referenced to the analog input signal (1). $\overline{BL}$ and HS outputs are referenced to the S-DMSD output (2). Waveform timing is indicated in numbers (n) of LL3 clock cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, $\overline{BL}$ and CVBS inputs to the S-DMSD and n = 4 for HS.

Data delay T1 input to output at subaddress SA06 = C0

SA0B = 00 : 63 x $1/f_{LL3}$

SA0B = 3C : 123 x $1/f_{LL3}$

Fig.10 Signal correction.

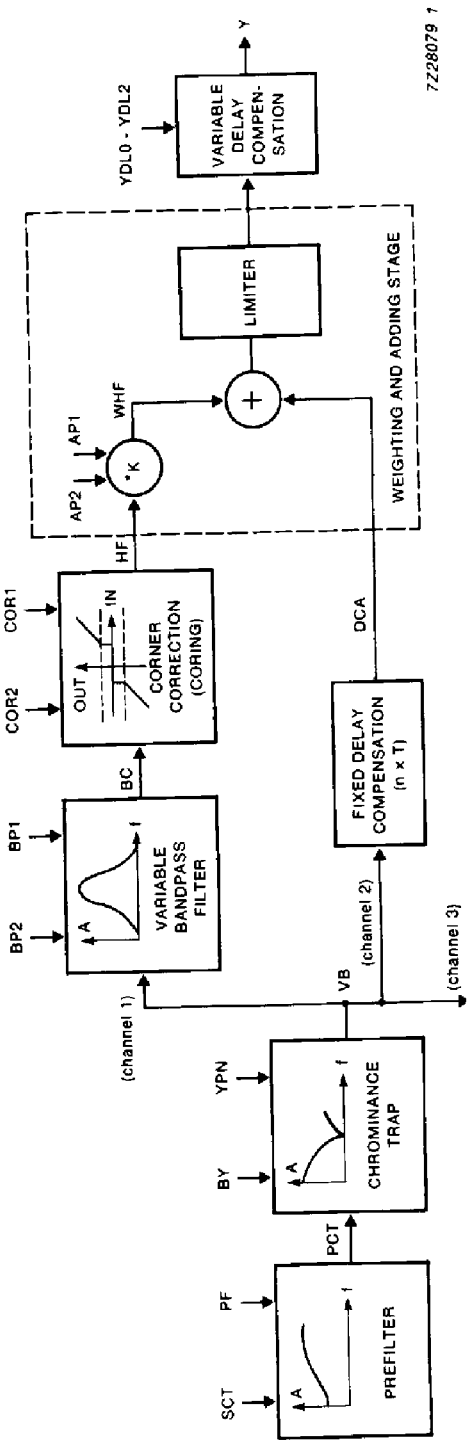


Fig.11 Luminance path of the S-DMSD.

SUBADDRESS 06

Table 13 Chrominance trap select (BY switches the chrominance trap to the bypass mode; YPN selects the notch-frequency)

CHROMINANCE TRAP	CONTROL BITS	
	BY (SA06, D7)	YPN (SA08, D2)
PAL (4 43 MHz)	0	0
NTSC (3.58 MHz)	0	1
bypass	1	X

Table 14 Disconnecting the luminance prefilter (user dependent)

PREFILTER	CONTROL BIT PF (SA06, D6)
ON	0
OFF	1

Table 15 Bandpass control (BP1 and BP2 control the centre frequency of the bandpass filter, see Figs 13 to 16)

BANDPASS TYPE (CENTRE FREQUENCY)	CONTROL BITS	
	BP2 (SA06, D5)	BP1 (SA06, D4)
type 1 (4 1 MHz)	0	0
type 2 (3.8 MHz)	0	1
type 3 (2.6 MHz)	1	0
type 4 (2.9 MHz)	1	1

Table 16 Coring threshold level (COR1 and COR2 control the suppression of low amplitude and high frequency signal components, see Fig.12)

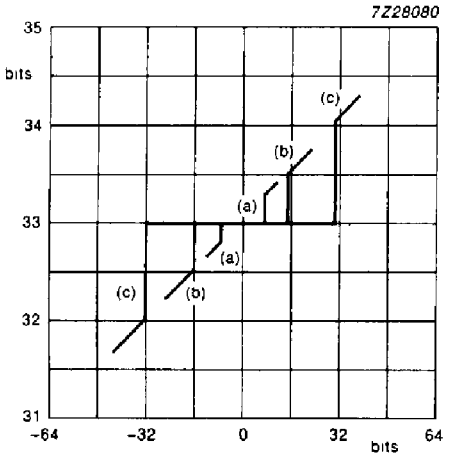
THRESHOLD	Fig.12	CONTROL BITS	
		COR2 (SA06, D3)	COR1 (SA06, D2)
coring off		0	0
coring on (4 bits of 12 bits)	a	0	1
coring on (5 bits of 12 bits)	b	1	0
coring on (6 bits of 12 bits)	c	1	1

Note

The thresholds are related the word width of the bandpass filter (12 bits).

Table 17 Aperture correction factor (AP1 and AP2 select the weighting factor K of the high frequency (HF) luminance components, see Fig.11)

WEIGHTING FACTOR K	CONTROL BITS	
	AP2 (SA06, D1)	AP1 (SA06, D0)
0	0	0
0.25	0	1
0.5	1	0
1	1	1



(a) for COR2 = 0 and COR1 = 1
(b) for COR2 = 1 and COR1 = 0
(c) for COR2 = 1 and COR1 = 1

Fig.12 Coring stage response.

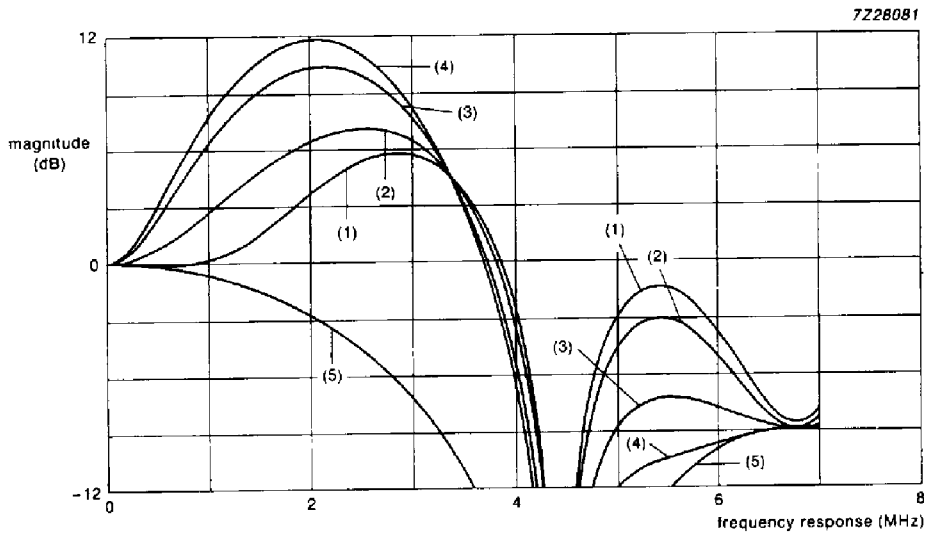


Fig.13 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); PAL mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

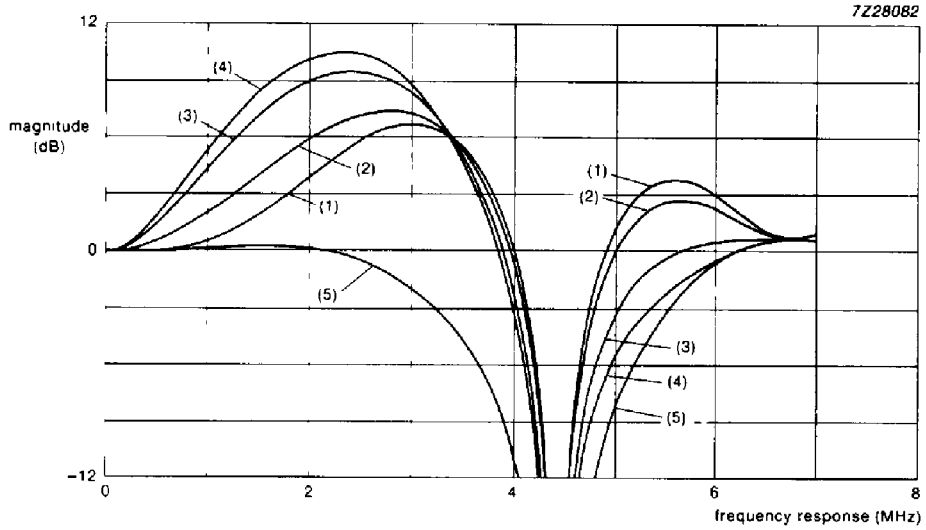


Fig.14 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); PAL mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

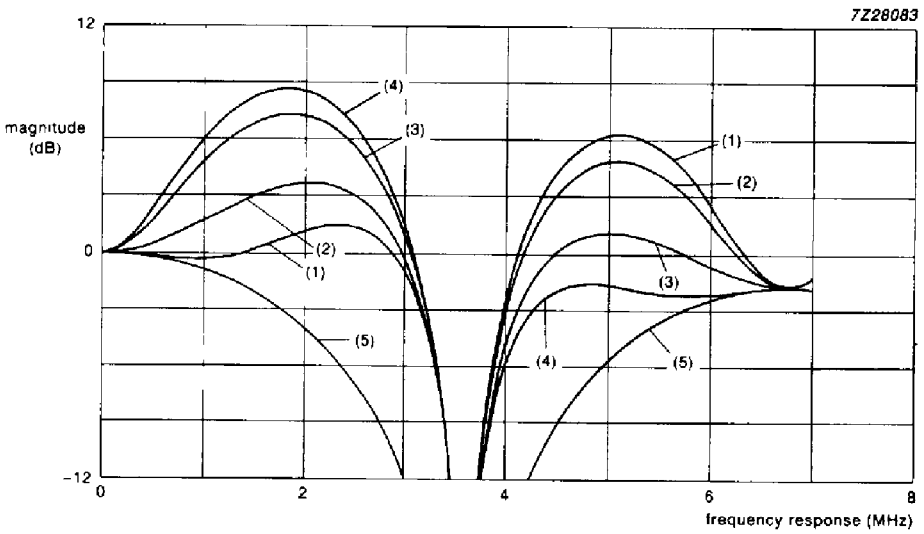


Fig.15 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); NTSC mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

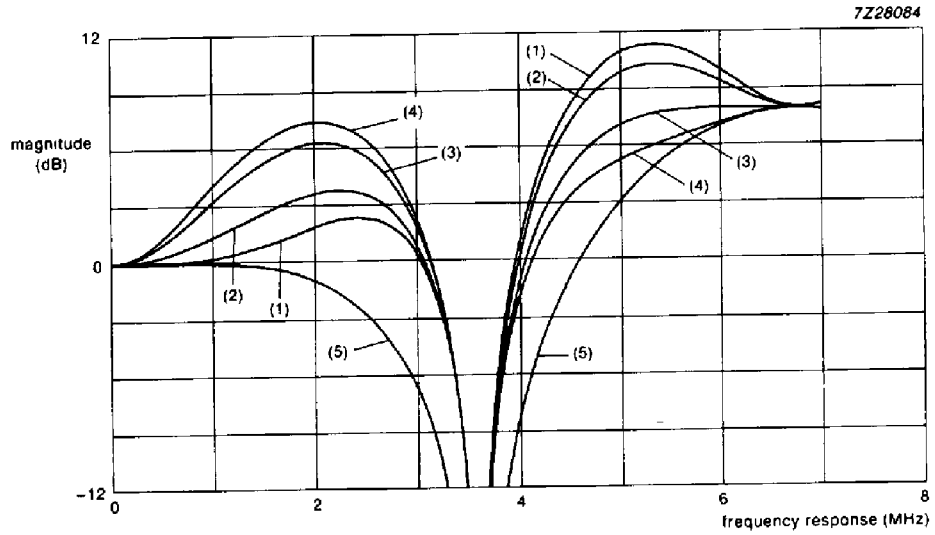


Fig.16 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); NTSC mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

SUBADDRESS 07

Table 18 Hue phase (user dependent, see notes 1 to 3)

HUE PHASE (deg)	CONTROL BITS							
	A77	A76	A75	A74	A73	A72	A71	A70
+178.6 to 0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0
0 to −180	0	0	0	0	0	0	0	0

Notes to Table 18

1. Step size per least significant bit (A70) = 1.4 degree.
2. Reference point for positive colour difference signals = 0 degree.
3. The hue phase may be shifted ±180 degrees from the reference point using bit A77, the colour difference signals are then switched from normally positive to negative polarity.

SUBADDRESS 08

Table 19 Horizontal clock PLL (application dependent)

FUNCTION	HPLL CONTROL BIT (SA08, D7)
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Table 20 Field frequency select (system mode dependent)

FUNCTION	CONTROL BIT FS (SA08, D6)
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

Table 21 VTR/TV mode select (system mode dependent)

FUNCTION	CONTROL BIT VTR (SA08, D5)
VTR mode	1
TV mode	0

Table 22 Colour on control (system mode dependent)

FUNCTION	CONTROL BIT CO (SA08, D4)
colour ON	1
colour OFF (all colour output samples zero)	0

Table 23 Alternate/non–alternate mode (system mode dependent)

FUNCTION	CONTROL BIT ALT (SA08, D3)
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Table 24 Chrominance trap select and amplitude matching (system mode dependent)

CHROMINANCE TRAP	CONTROL BIT YPN (SA08, D2)
3.58 MHz	1
4 43 MHz	0

Table 25 Colour carrier frequency control (system mode dependent)

COLOUR CARRIER FREQUENCY	CONTROL BITS	
	CCFR1 (SA08, D1)	CCFR0 (SA08, D0)
4 433 618 75 Hz (PAL-B, G, H, 1; NTSC 4.43)	0	0
3 575 611.49 Hz (PAL-M)	0	1
3 582 056.25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

SUBADDRESS 09

Table 26 Vertical noise limiter.

FUNCTION	CONTROL BIT VNL (SA09, D7)
VNL active	1
VNL bypassed	0

Table 27 Y-output enable (system mode dependent)

FUNCTION	CONTROL BIT OEY (SA09, D6)
outputs D1 - D7 and $\overline{BL}$ active	1
outputs D1 - D7 and $\overline{BL}$ HIGH-impedance Z-state	0

Table 28 Chrominance output enable (system mode dependent)

FUNCTION	CONTROL BIT OEC (SA09, D5)
outputs UV0 - UV3 active; if CD = logic 1, chrominance signal output; if CD = logic 0, zero signal	1
outputs UV0 - UV3 HIGH-impedance Z-state	0

Table 29 Internal colour forced ON/OFF (test purposes only)

FUNCTION	CONTROL BIT CI (SA09, D3)
colour forced ON, if CO = logic 1 (CD = X) or colour OFF, if CO = logic 0 (CD = X)	1
colour OFF, if CO = logic 0 (CD = X) or colour controlled by CD, if CO = logic 1	0

Where:

X = don't care.

Table 30 Additional output for circuit control

FUNCTION	CONTROL BIT AFCC
output AFCC = HIGH	1
output AFCC = LOW	0

Table 31 Source-select (system mode dependent)

FUNCTION	CONTROL BIT SS0 - SS3
output SS0 - SS3 = HIGH	1
output SS0 - SS3 = LOW	0

Table 32 Source select (pin and subaddress)

CONTROL BIT	PIN	SUBADDRESS
AFCC	68	09, D2
SS3	25	0A, D4
SS2	24	0A, D3
SS1	66	09, D1
SS0	65	09, D0

SUBADDRESS 0A

Table 33 Disabling of HSY and HC pulses (system mode dependent)

FUNCTION	CONTROL BIT SYC (SA0A, D7)
HSY and HC output pulses disabled	1
HSY and HC output pulses enabled	0

Table 34 Chrominance input/output 3-state control

FUNCTION	CONTROL BIT CT (SA0A, D6)
CVBS output active	1
output HIGH-impedance Z-state	0

Table 35 Chrominance source select

FUNCTION	CONTROL BIT YC (SA0A, D5)
Y/C separate inputs	1
CVBS input	0

Table 36 Variable delay compensation of the luminance path (YDL0 - YDL2 control the luminance delay in order to compensate different chrominance delays throughout the system)

DELAY (N =)	CONTROL BITS (SA0A, D2 .. D0)		
	YDL2	YDL1	YDL0
0	0	0	0
+1	0	0	1
+2	0	1	0
+3	0	1	1
–4	1	0	0
–3	1	0	1
–2	1	1	0
–1	1	1	1

Notes to Table 36

1. The delay is given in terms of clock cycles:
2. 13.5 MHz = N x 74 ns.

SUBADDRESS 0B

Table 37 SECAM chrominance delay compensation (system mode dependent)

PROGRAMMABLE DELAY*	CONTROL BITS						
	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
8	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.
16	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.
32	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.
63	0	1	1	1	1	1	1
64	1	1	1	0	0	0	0
65	1	1	1	0	0	0	1
.	.	.	.	.	.	.	.
79	1	1	1	1	1	1	1
Maximum delay selected by single control bit							
	16	32	16	8	4	2	1

Notes to Table 37

1. * = Delay in number of LL3 clock cycles.
2. SA0B, D7 don't care.

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

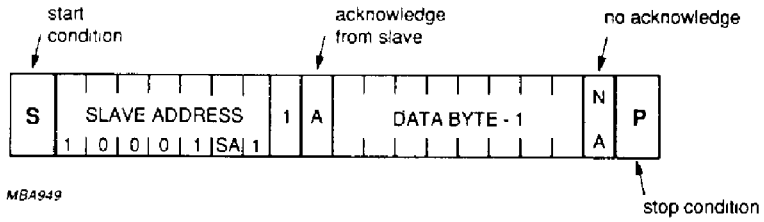


Fig.17 Slave transmitter format (a general call address is not acknowledged).

The format of data byte 1 is:

Table 38

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	HLOCK	1	FD	0	CD	CS	0

Data bits D0, D3 and D5 are fixed in slave transmitter byte.

Table 39 Description of data byte 1

BIT	DESCRIPTION
PONRES	Status bit for power-on-reset ($\overline{RES}$) and after a power failure. logic 1 after the first power-on-reset and after a power failure Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9051). PONRES sets all data bits of control registers 1 and 2 to zero. logic 0 after a successful read of the PAL/NTSC decoder status byte
HLOCK	Status bit for horizontal frequency lock (transmitter identification, stop or mute bit): logic 1 if horizontal frequency is not locked (no transmitter available); logic 0 if horizontal frequency is locked (transmitter received)
FD	Detected field frequency status bit: logic 1 when received signal has 60 Hz synchronization pulses; logic 0 when received signal has 50 Hz synchronization pulses
CD	PAL/NTSC colour-detected status bit: logic 1 when PAL/NTSC colour signal is detected; logic 0 when no PAL/NTSC colour signal is detected
CS	SECAM colour-detected status bit: logic 1 when SECAM colour signal is detected; logic 0 when no SECAM colour signal is detected.

Default coefficients set for the S-DMSD and SAA9056

The default coefficients are set for operation with the TDA8703 or TDA8708, these devices are analog-to-digital converters. The 3-state outputs of the chrominance ADC are controlled by the SS3 switch in this example (all numbers are hex values).

The slave addresses are as follows:

- S-DMSD; 8A or 8E
- SAA9056; 8A or 8E

Table 40 Slave address (SAA9051 part)

SUBADDRESS	FUNCTION	SHORT DELAY	LONG DELAY
00	inc. delay	5E	7E
01	HSY start	37	73
02	HSY stop	07	43
03	HC start	F6	32
04	HC stop	C7	03
05	HS start	FF	FF
06	H-peaking	02 (62 NTSC)	02 (62 NTSC)
07	HUE control	00	00
08	control 1	38 (77 NTSC)	38 (77 NTSC)
09	control 2	E3	E3 (D3 SECAM)
0A	control 3	58 (28 Y/C mode)	58 (28 Y/C mode)
0B	SECAM delay	00	3C

Notes to Table 40

1. Subaddress 05; application dependent.
2. Subaddress 08; HPLL is in the VTR mode. Hex value for TV mode is 18 (57 for NTSC).

Table 41 Slave address (SAA9056 part)

SUBADDRESS	FUNCTION	VALUE
10	luminance delay	C0 - FF
11	$\overline{BL}$ delay	00
12	burst gate start	42
13	burst gate stop	56
14	sensitivity	20
15	filter	24
16	control	04 (02 active)

Table 42 Operating modes of the S-DMSD

INPUT	CT	YC	SS3	CE	SCDC	IDEL	YPN	BY	FS	ALT	CCFR1	CCFR0	REMARKS
PAL B, G, H, I													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	0	0	
Y/C	0	1	0	0	A	A	0 (1)	1	0	1	0	0	
PAL M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	1	0	1	
Y/C	0	1	0	0	A	A	1 (0)	1	1	1	0	1	
PAL N													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	1	0	
Y/C	0	1	0	0	A	A	0 (1)	1	0	1	1	0	
SECAM													
CVBS	1	0 (1)	1	1	B	B	0	0	0	0 (1)	0 (1)	0 (1)	
Y/C	0	1 (0)	0	1	B	B	0 (1)	1	0	0 (1)	0 (1)	0 (1)	
NTSC 4.43 MHz													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	0	0	0	use FS = 1 for 60 Hz vertical frequency
Y/C	0	1	0	0	A	A	0 (1)	1	1	0	0	0	use FS = 1 for 60 Hz vertical frequency
NTSC M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	0	1	1	
Y/C	0	1	0	0	A	A	1 (0)	1	1	0	1	1	

Notes to Table 42

1. SS3 is assumed to control the 3-state output of the chrominance ADC (active LOW).
2. To avoid data collision care must be taken with the programming of CT and SS3 (in this equal they are always equal).

Where:

A = short time delay
B = long time delay.

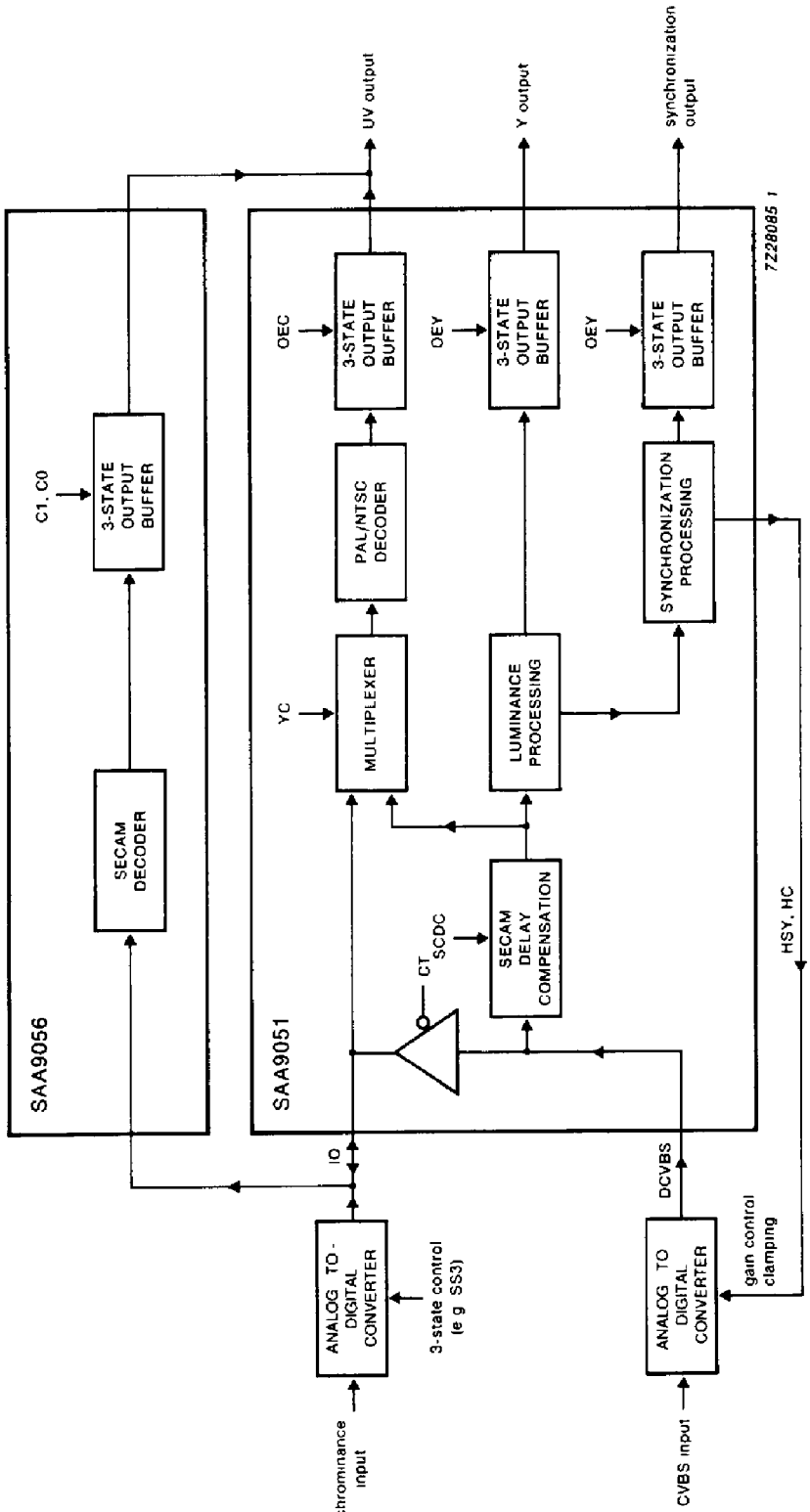


Fig.18 SAA9051 signal flow when used in conjunction with SAA9056.

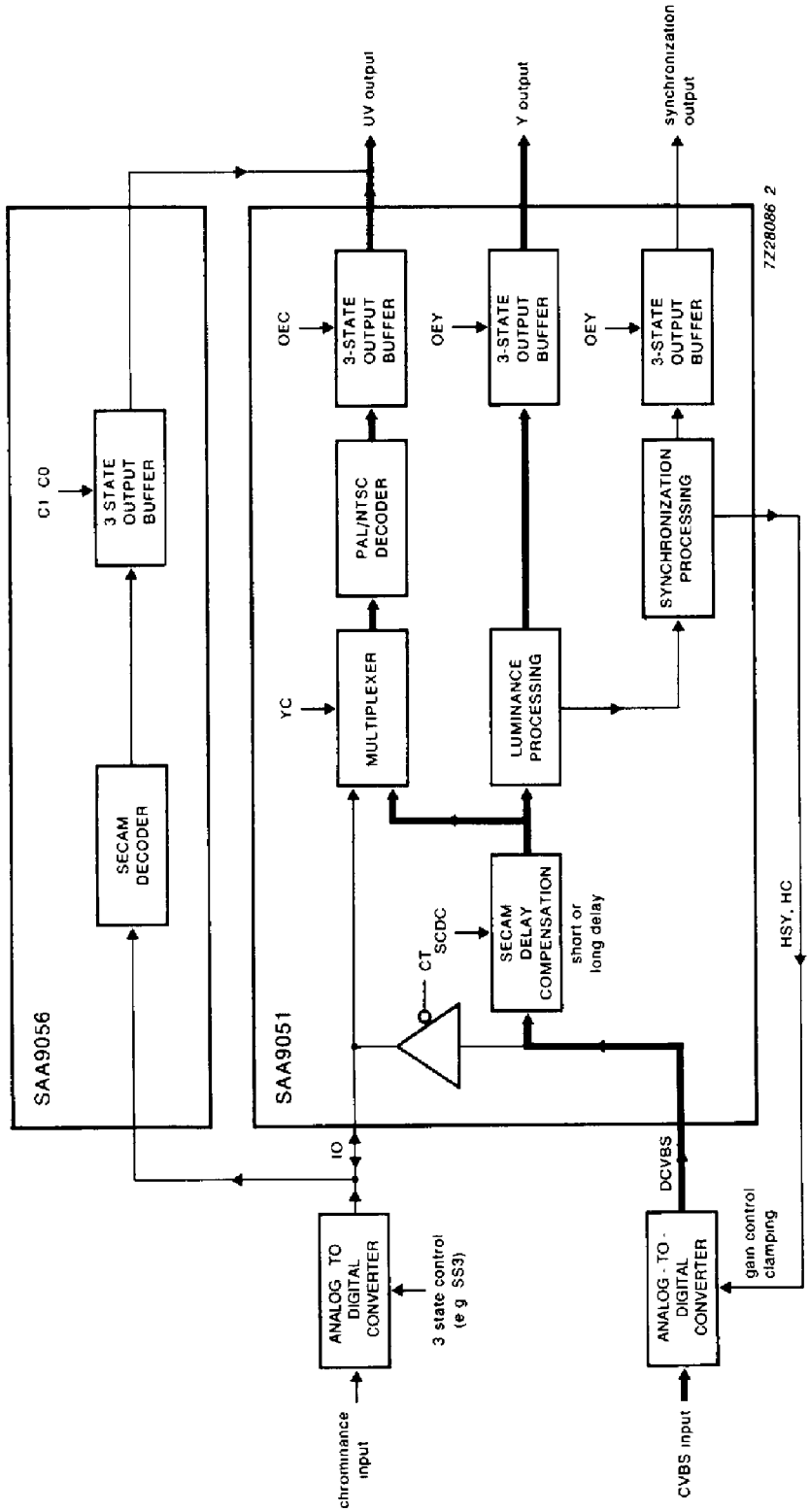


Fig.19 Signal flow - PAL or NTSC with CVBS input signal.

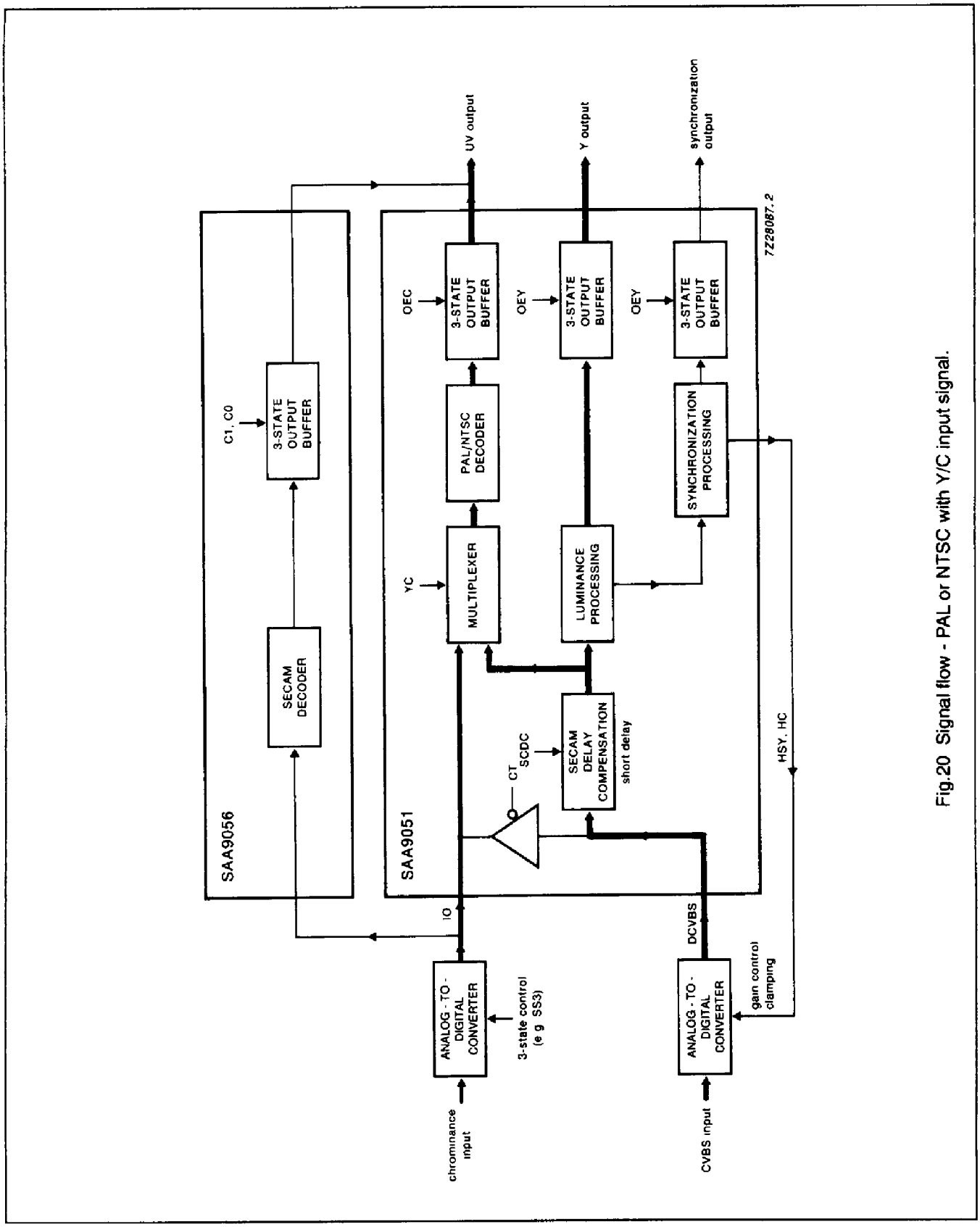


Fig.20 Signal flow - PAL or NTSC with Y/C input signal.

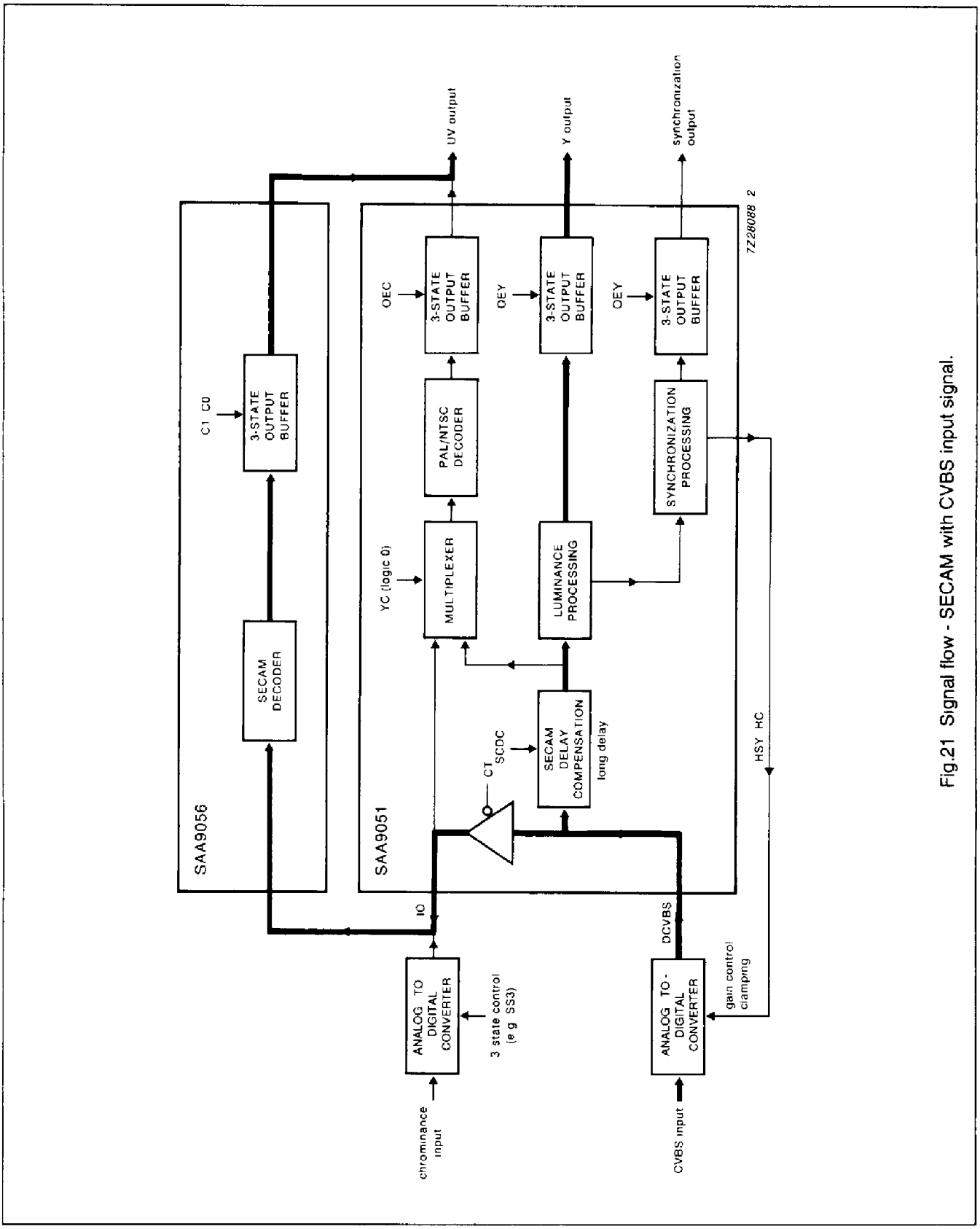


Fig.21 Signal flow - SECAM with CVBS input signal.

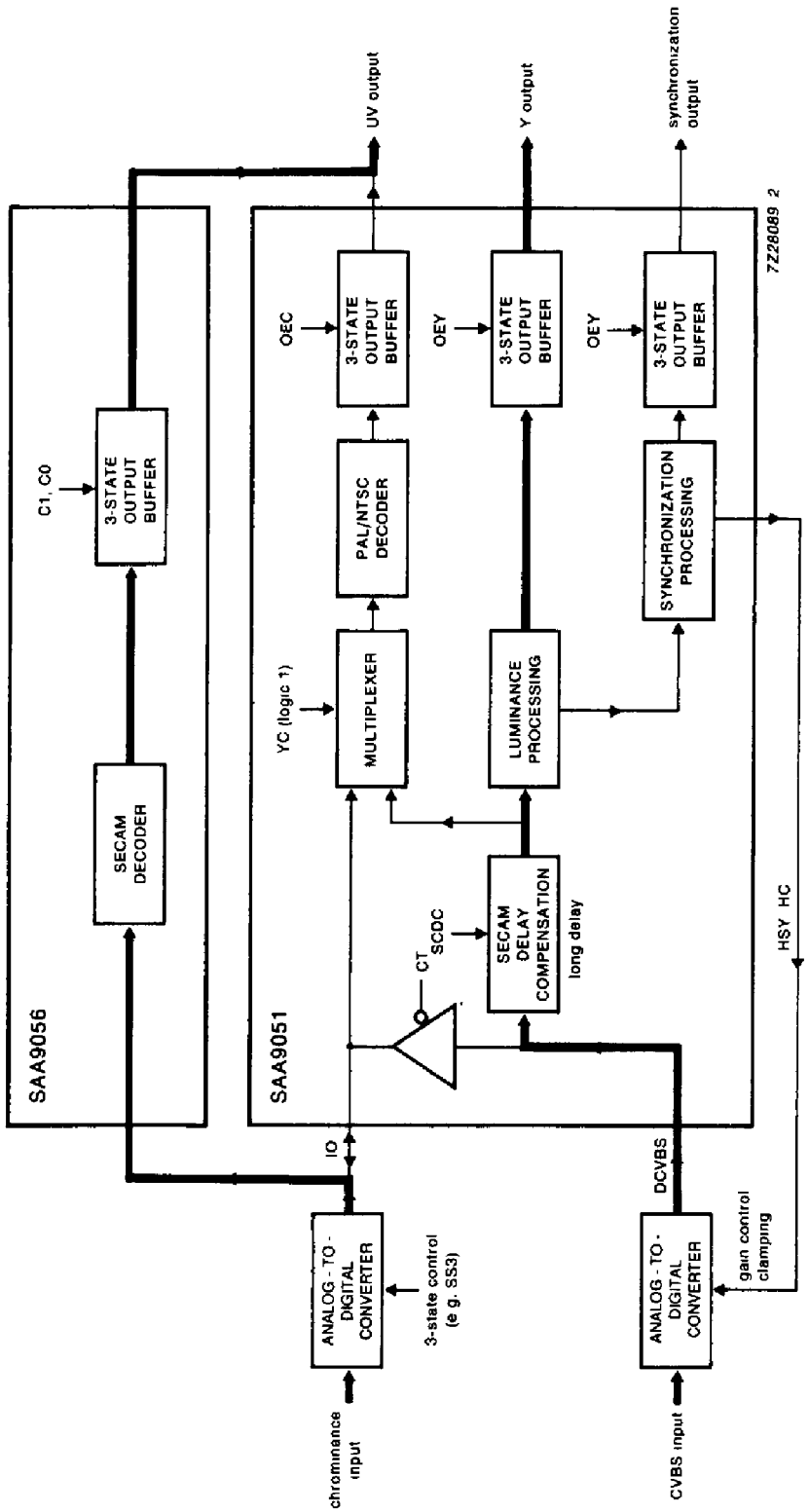


Fig.22 Signal flow - SECAM with Y/C input signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		−0.5	+7	V
V_I	input voltage range		−0.5	+7	V
V_O	output voltage range	I_{Omax} = 20 mA	−0.5	+7	V
P_{tot}	maximum power dissipation per package		-	2750	mW
T_{amb}	operating ambient temperature range		0	+70	°C
T_{stg}	storage temperature range		−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices')

CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5	5.5	V
I_{DD}	supply current	note 1	-	370	500	mA
Inputs						
INPUT VOLTAGE LOW						
V_{IL}	pins 2 - 4, 6 - 17, 20 - 23, 33, 43, 56 and 64		−0.5	-	+0.8	V
V_{IL}	pins 40 and 41		−0.5	-	+1.5	V
INPUT VOLTAGE HIGH						
V_{IH}	pins 2 - 4, 6 - 17, 20 - 23, 43, 56 and 64		2	-	V_{DD}	V
V_{IH}	pins 33, 40 and 41		3	-	V_{DD}	V
INPUT LEAKAGE CURRENT						
I_I	pins 2 - 4, 6 - 17, 20 - 23, 40 - 41, 43 and 64		-	-	10	µA
INPUT CAPACITANCE						
C_I	pin 4		2	-	10	pF
C_I	pins 2 - 3, 14 - 17, 20 - 23, 43 and 64		2	-	7.5	pF
C_I	pins 6 - 13	HIGH-impedance Z-state	2	-	7.5	pF
Outputs						
OUTPUT VOLTAGE LOW						
V_{OL}	pins 6 - 13, 24 - 26, 29 - 32, 42, 45 –50, 53, 55 - 58, 65 - 66 and 68	I_{OL} = 2.0 mA	0	-	0.6	V
V_{OL}	pins 40 and 41	I_{OL} = 5.0 mA	0	-	0.45	V
OUTPUT VOLTAGE HIGH						
V_{OH}	pins 6 - 13, 24 - 26, 29 - 32, 42, 45 - 50, 53, 55 - 58, 65 - 66 and 68	I_{OH} = −0.5 mA	2.2	-	V_{DD}	V
OUTPUT CAPACITANCE						
C_O	pins 45 - 50, 53 and 55 - 58		-	-	7.5	pF
LFCO OUTPUT (NOTE 2)						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	$R_L \geq 10$ kΩ; C_L < 15 pF	1.0	-	-	V
$V_{o(p-p)}$	output voltage (peak-to-peak value)	$R_L \geq 1$ kΩ; C_L < 15 pF	0.5	-	-	V
Timing (see Fig.23)						
t_{C3}	LL3 cycle time		69	-	80	ns
t_{C3H}/t_{C3}	LL3 duty factor		43	-	57	%
t_r, t_f	LL3 rise and fall times	note 3	-	-	6	ns
$t_{SU\ DAT}$	input data set-up time		12	-	-	ns

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Timing (see Fig.23)						
$t_{HD\ DAT}$	input data hold time		5	-	-	ns
t_{HD}	output data hold time		5	-	-	ns
t_D	output data delay time	except HSY and HC; C_L = 25 pF, I_{OL} = 2.0 mA; V_{OH} = 2 2 V	-	-	50	ns
t_D	HSY and HC output delay time	C_L = 25 pF; I_{OL} = 2 0 mA, V_{OH} = 2.6 V	-	-	80	ns
C_L	output data load capacitance		7.5	-	25	pF
Crystal oscillator (see Fig.20)						
f_n	nominal frequency	third harmonic	-	24 576	-	MHz
$\Delta f/f_n$	permissible deviation of f_n		-	$\pm 50 \times 10^{-6}$	-	
$\Delta T/f_n$	temperature deviation from f_n		-	$\pm 20 \times 10^{-6}$	-	
T_{XTAL}	temperature range		0	-	+70	°C
C_{LXTAL}	load capacitance		8	-	-	pF
R_r	maximum resonance resistance		-	40	80	Ω
C_1	motional capacitance		-	1 5 ±20%	-	fF
C_0	parallel capacitance		-	3.5 ±20%	-	pF

Notes to the characteristics

1. Inputs LOW and outputs not connected, V_{DD} = 5 V.
2. 4-bit triangular waveform clocked at 24 576 MHz, AC coupled at pin 36.
3. Rising and falling edges of the clock signal are assumed to be smooth e.g due to roll-off low-pass filtering.

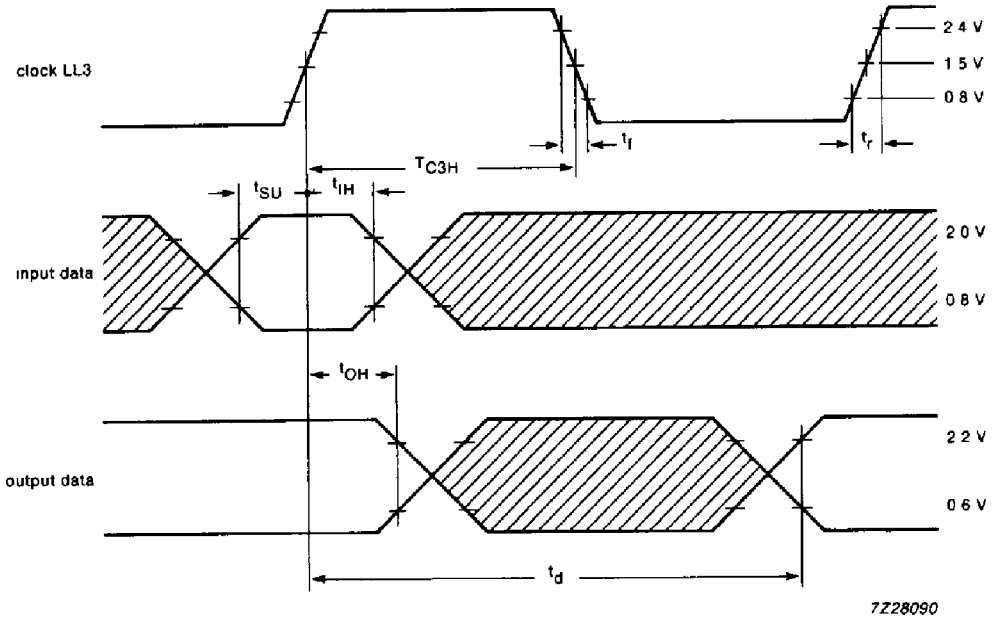


Fig.23 Timing diagram.

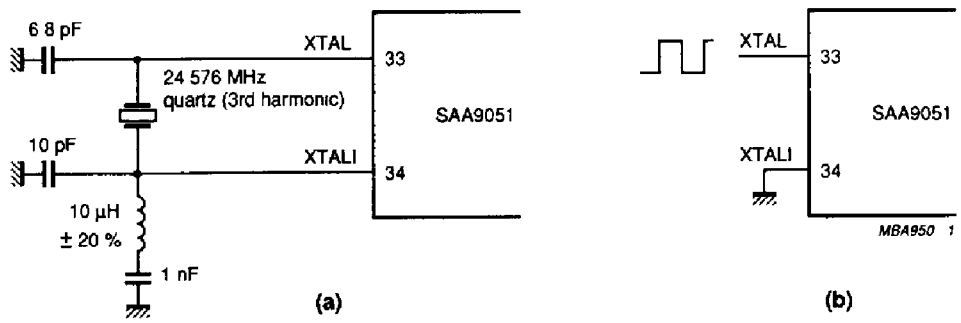


Fig.24 Oscillator circuit requirements; (a) with quartz crystal; (b) with external clock.