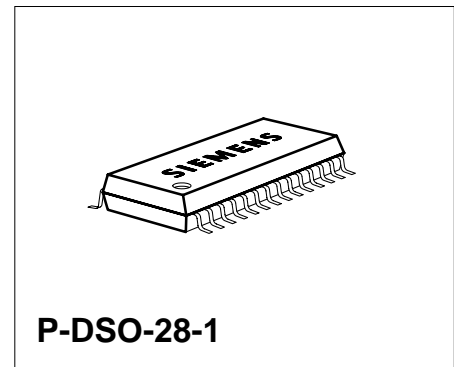
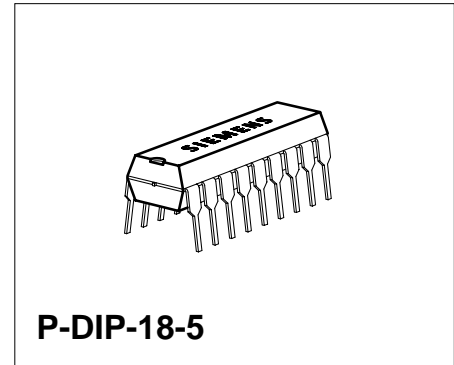


1 Overview

1.1 Features

- Fast I²C Bus controlled (max. 400 kHz)
- Cascadable (2 bus addresses)
- 7 CVBS inputs, 5 outputs
 - 3 inputs with clamp disable by bus
- 1 input selectable as Y-input (S-VHS)
- 1 additional C-input (S-VHS)
- Y+C operation for S-VHS
 - selected by bus
- Fully ESD protected
- – 60 dB max. crosstalk at 5 MHz (P-DSO-28-1 only)
- Low operating voltage of 7.5 V
- 5 V operation is possible with reduced output signals of max. 2 V_{pp}
- 15 MHz minimum bandwidth
- Noise insensitive clamping inputs
- Low impedance off condition
 - separate for each output



Type	Ordering Code	Package
TDA 6920	Q67000-A5200	P-DIP-18-5
TDA 6920X	Q67007-A5225 GEG	P-DSO-28-1

1.2 General Description

The TDA 6920 switches 7 video input sources to 5 outputs. Each output can be switched to only one input, but one input can be switched to all outputs. The C-input may be combined with one CVBS input as Y for Y+C (S-VHS) operation. Y+C operation is selected by bus.

1.3 Application

- Television sets
- Satellite receivers
- Video mixing desks

1.4 Pin Configuration
(top view)

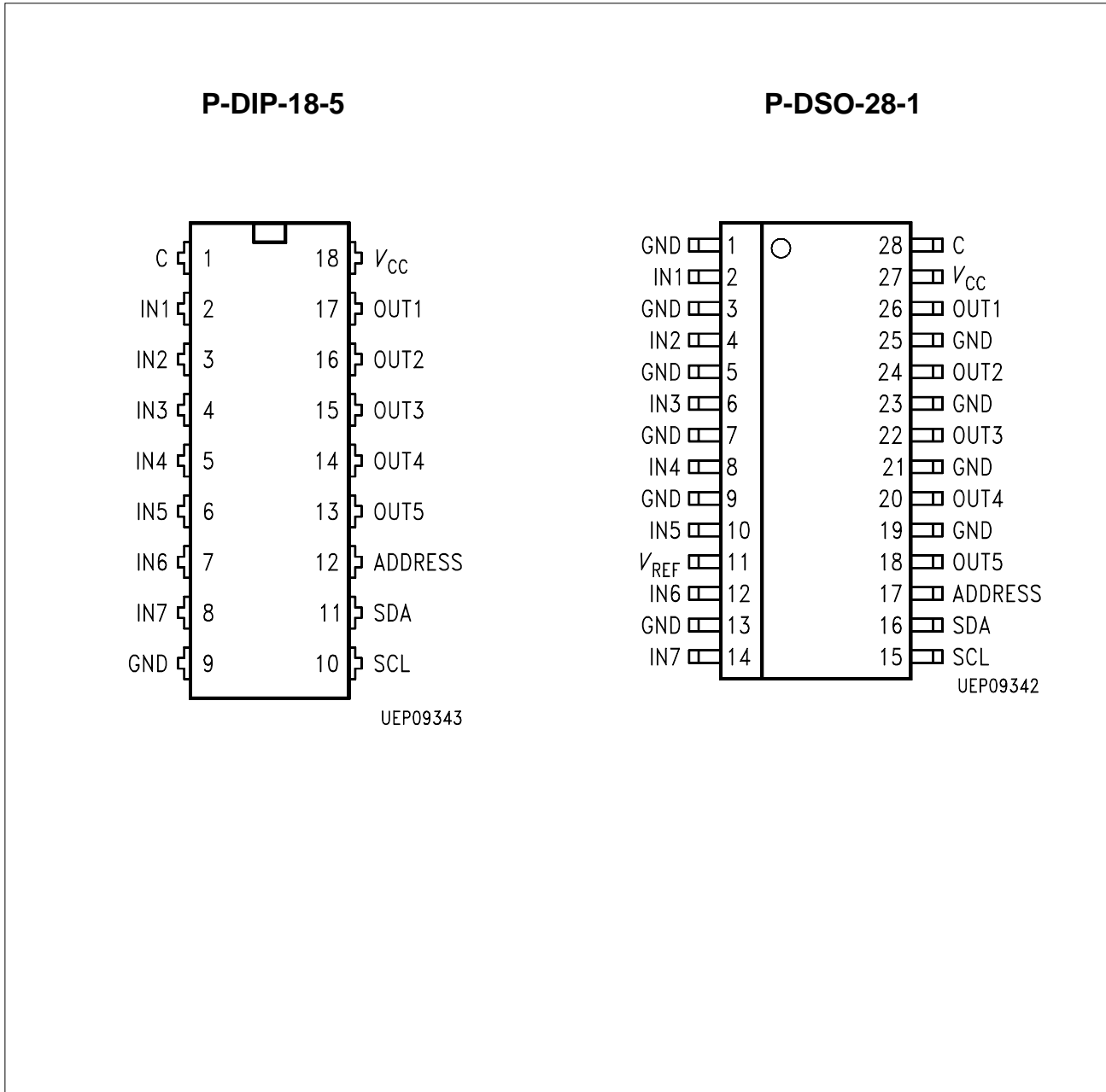


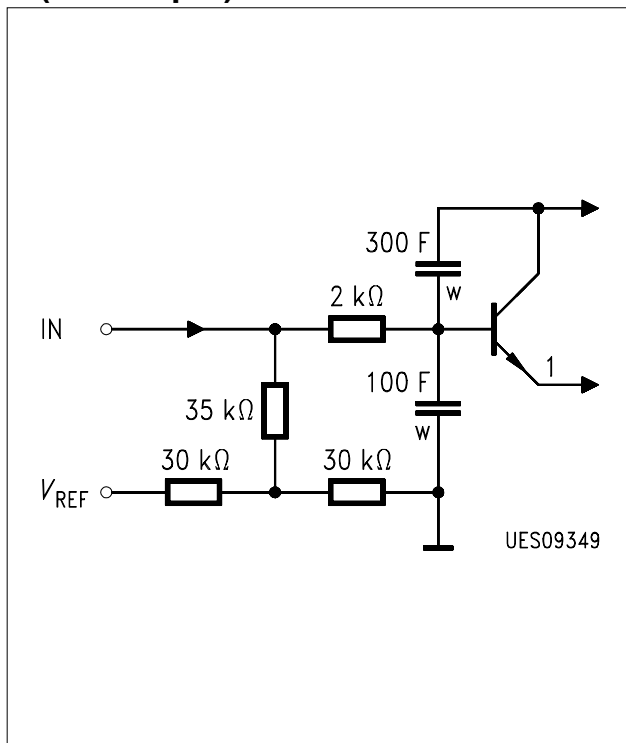
Figure 1

1.5 Pin Definitions and Functions

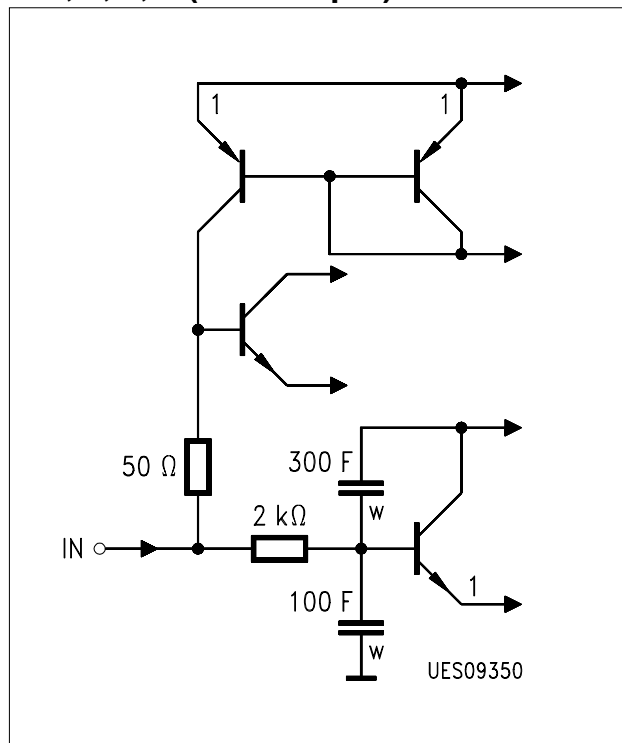
Pin No.		Symbol	Function
P-DIP-18-5	P-DSO-28-1		
–	1	GND	Signal and power supply ground
2	2	IN1	CVBS input 1
–	3	GND	Signal and power supply ground
3	4	IN2	CVBS input 2
–	5	GND	Signal and power supply ground
4	6	IN3	CVBS input 3
–	7	GND	Signal and power supply ground
5	8	IN4	CVBS input 4
–	9	GND	Signal and power supply ground
6	10	IN5	CVBS input 5
–	11	V_{REF}	Reference Voltage for external use
7	12	IN6	CVBS input 6
9	13	GND	Power supply ground
8	14	IN7	CVBS input 7
10	15	SCL	I ² C-Bus clock
11	16	SDA	I ² C-Bus data
12	17	ADDRESS	Address selection
13	18	OUT5	CVBS output 5
–	19	GND	Signal and power supply ground
14	20	OUT4	CVBS output 4
–	21	GND	Signal and power supply ground
15	22	OUT3	CVBS output 3
–	23	GND	Signal and power supply ground
16	24	OUT2	CVBS output 2
–	25	GND	Signal and power supply ground
17	26	OUT1	CVBS output 1
18	27	V_{CC}	Positive power supply voltage
1	28	C	Separate color adding input for input 1

1.6 Pin Description

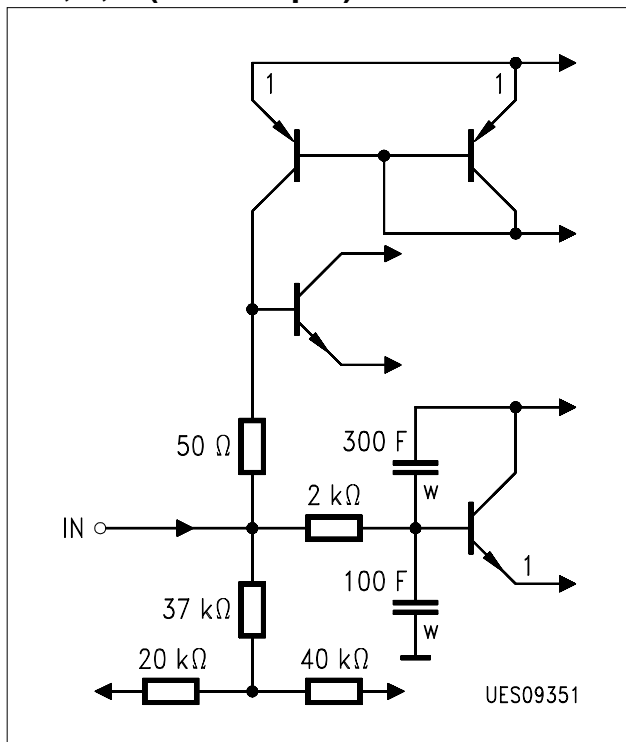
C (color input)



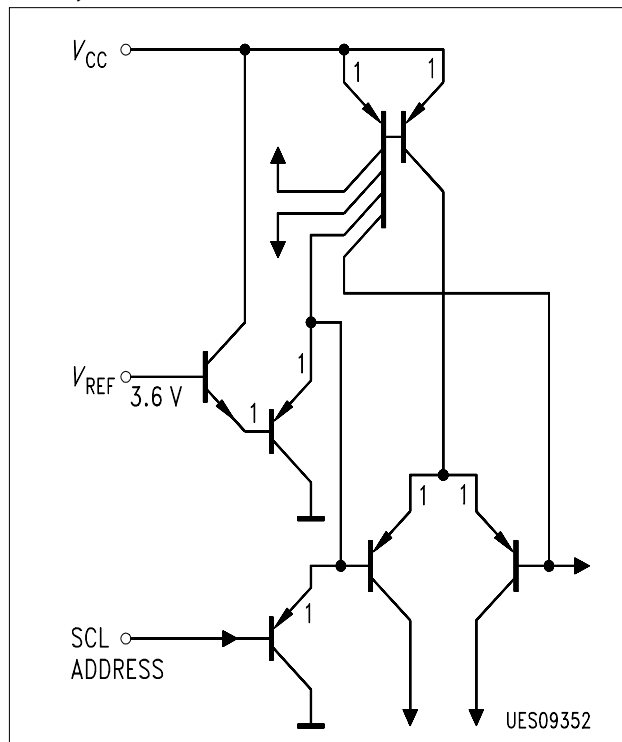
In 2, 5, 6, 7 (CVBS input)



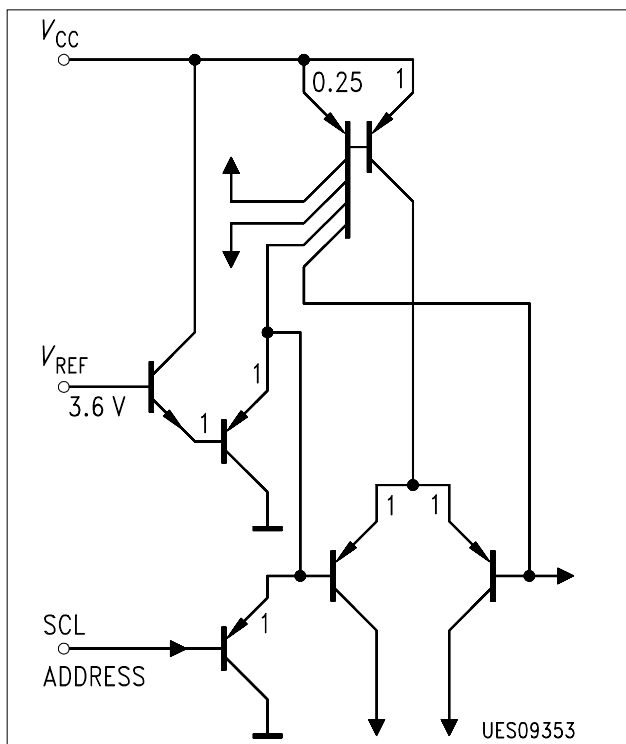
In 2, 3, 4 (CVBS input)



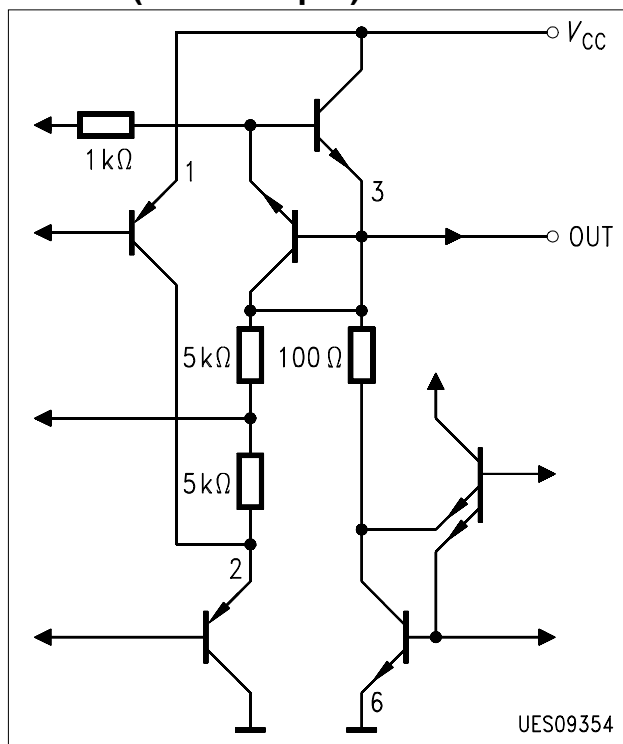
SCL, Address



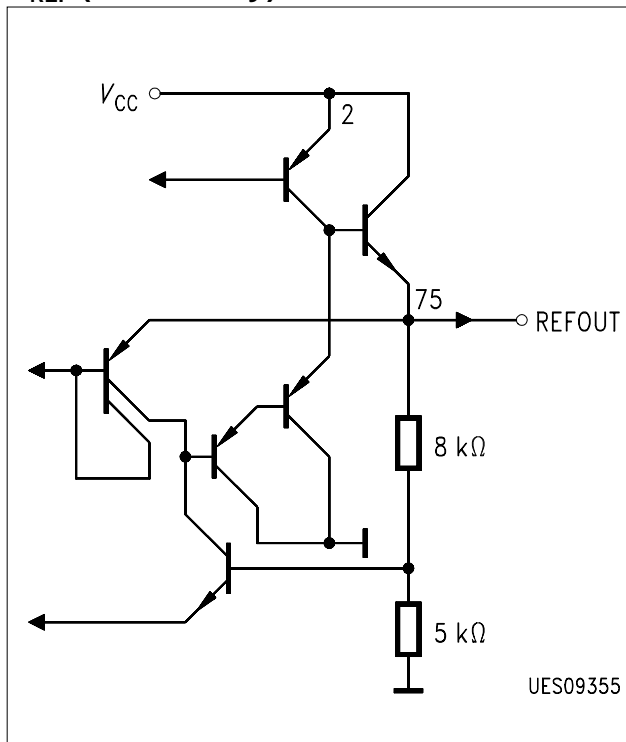
SDA



Out 1-5 (CVBS output)



V_{REF} (SO-28 only)



1.7 Functional Block Diagram

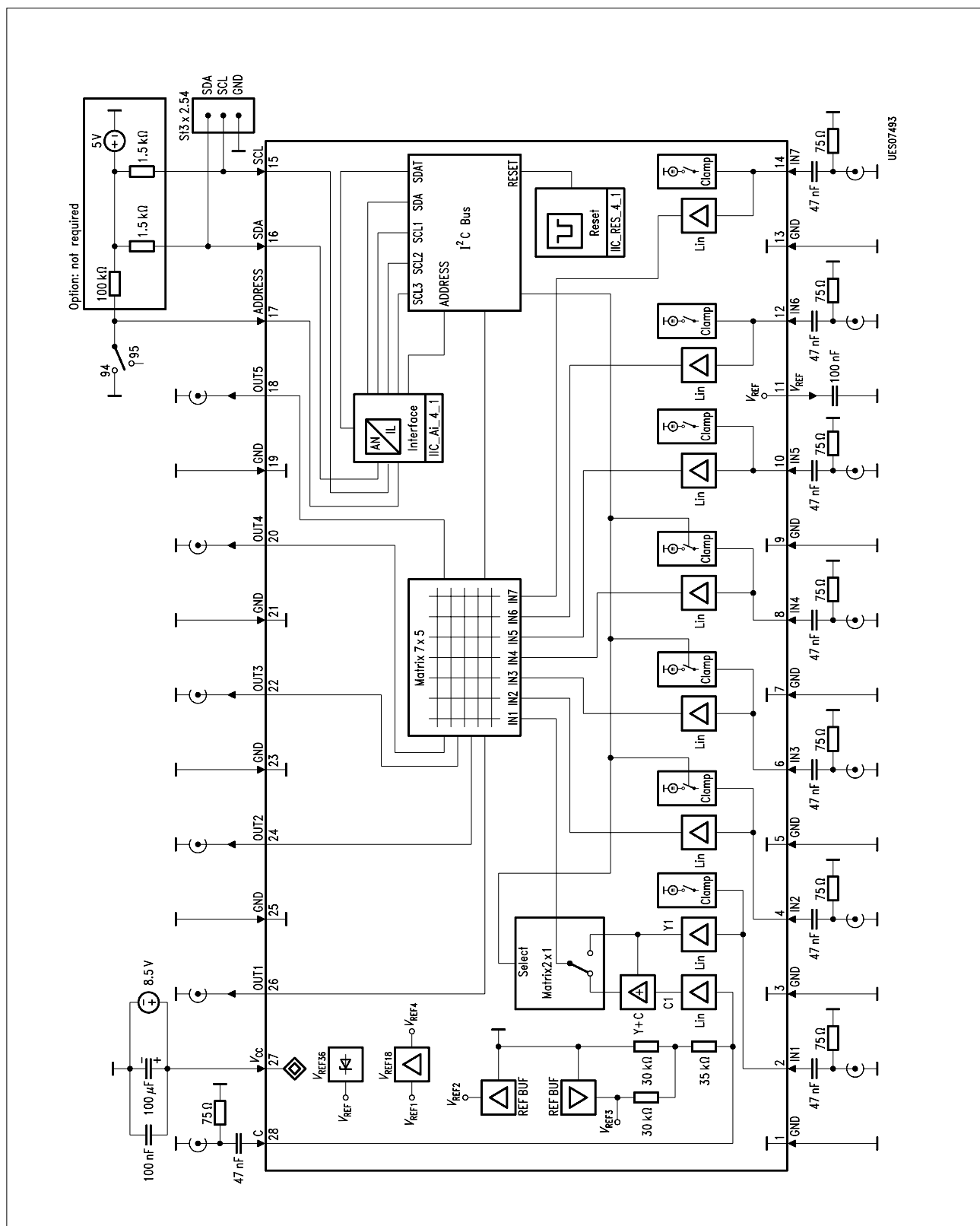


Figure 2
Block Diagram (P-DSO-28-1)

2 Functional Description

The main function of the IC is to switch 7 input video sources to 5 outputs.

Each output can be switched to only one input.

It is possible to have the same input connected to several outputs.

3 of the inputs can be used as non-clamping-input, switching is controlled by bus.

The clamping function of the other 4 inputs can be overridden by external resistor divider.

The other 4 inputs can be switched to non-clamping mode with external R/C network.

All switching possibilities are controlled by the I²C Bus.

All outputs can be switched to low impedance off condition by the I²C Bus.

Driving 75 Ω load requires external transistors for best performance.

The recommended coupling capacitor at each input is 47 nF.

Each clamping input requires a 75 Ω (max. 500 Ω) termination resistor.

Operation without or with a termination resistor greater than 500 Ω causes malfunction of the new high performance clamping circuit.

Unused inputs should be directly grounded.

6 × 8 bits are necessary to determine one complete configuration change.

(1 addressbyte, 5 databytes)

Minimum configuration change for 1 output needs 2 × 8 bit (1 addressbyte, 1 databyte).

Power on reset state: all 5 outputs switched to input 1, all inputs clamped, Y+C off.

● Address Selection (fast I²C Bus)

1st byte of transmission (8 bit)

Hex	Binary		Address Pin
	MSB	LSB	
96	1001	0110	V _{CC} (min. 3 V)
94	1001	0100	GND

● **Data Mode Selections (fast I²C Bus)**

2nd byte of transmission (8 bit)

Output Selection (3 bit, bit 7 must always be 0)

b7 b6¹⁾	b5 b4 b3	b2 b1 b0¹⁾	Selected Output
0X	000	XXX	- not used
0X	001	XXX	OUT1
0X	010	XXX	OUT2
0X	011	XXX	OUT3
0X	100	XXX	OUT4
0X	101	XXX	OUT5
0X	110	XXX	- not used
0X	111	XXX	- not used

¹⁾..X = don't care

Input Selection Clamped (3 bit, bit 7 must always be 0)

b7 b6	b5 b4 b3¹⁾	b2 b1 b0	Selected Input
0X	XXX	000	Output off condition
00	XXX	001	IN1
00	XXX	010	IN2
00	XXX	011	IN3
00	XXX	100	IN4
0X	XXX	101	IN5
0X	XXX	110	IN6
0X	XXX	111	IN7

¹⁾..X = don't care

● **Data Mode Selections** (fast I²C Bus) continued

2nd byte of transmission (8 bit)

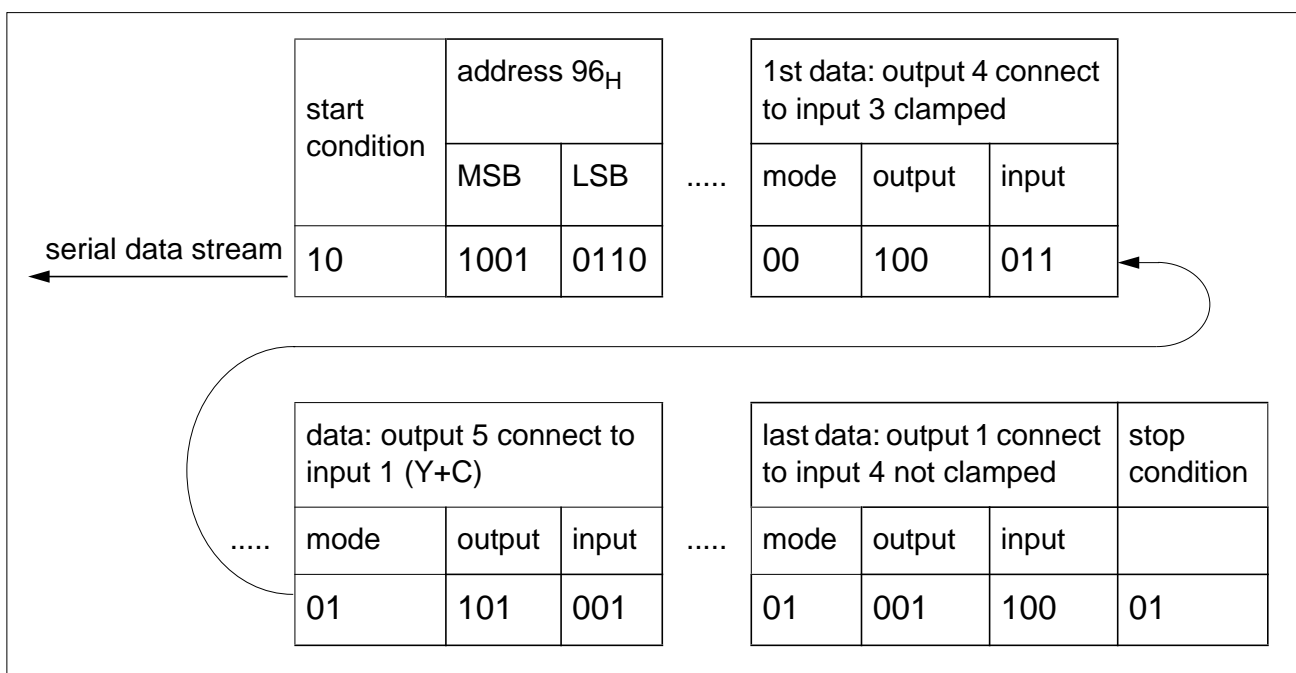
Input Selection Non Clamped / Y+C (Y: always clamped. C: non clamped)
(3 bit, bit 7 must always be 0)

b7 b6	b5 b4 b3 ¹⁾	b2 b1 b0	Selected input
00	XXX	001	in1, (Y+C) off
00	XXX	010	in2, clamp on
00	XXX	011	in3, clamp on
00	XXX	100	in4, clamp on
01	XXX	001	in1, (Y+C) on
01	XXX	010	in2, clamp off
01	XXX	011	in3, clamp off
01	XXX	100	in4, clamp off

¹⁾ X = don't care (if only input operation mode change is requested, b5, b4 b3 should be 0, 0, 0: no output configuration is changed.)

● **Bus Protocol** (fast I²C Bus)

Programming Example: SDA sequence



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage (V_{CC})	V_{CC}	0	14	V	
Reference voltage (P-DSO-28-1 only)	V_{REF}	0	5	V	
Reference current ($R_{Lmin} = 1\text{ k}\Omega$)	I_{REF}		3.5	mA	
Output voltage	$V_{OUT1 - OUT5}$	0	V_{CC}	V	
Output current ($R_{Lmin} = 500\ \Omega$)	$I_{OUT1 - OUT5}$		5	mA	
Input voltage	V_C	0	V_{CC}	V	
Input voltage	$V_{IN1 - IN7}$	0	V_{CC}	V	
SCL, SDA, address input voltage	$V_{SDA, SCL,}$ Address	0	V_{CC}	V	
ESD-voltage all pins HBM ($R = 1.5\text{ k}\Omega, C = 100\text{ pF}$)	V_{ESD}	- 6	6	kV	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	- 40	125	°C	
Thermal resistance (system - air)	$R_{th SA}$		75	K/W	

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_{CC}	7.5	13.2	V	
Absolute minimum supply voltage (only usable with reduced output signals of max. 2 Vpp)	V_{CC}	4.5		V	
Reference voltage (P-DSO-28-1 only)	V_{REF}	3.3	3.9	V	
Video-input frequency range – 3 dB	$f_{IN\ IN1 - IN7, C}$	0	20	MHz	
Video-input AC-voltage (color)	V_C		1.0	Vpp	
Video-input AC-voltage (Y, CVBS)	$V_{IN1 - IN7}$		1.7	Vpp	
Video-output AC-voltage	$V_{OUT1 - OUT5}$		3.4	Vpp	
Input DC-voltage	V_C	1.3	2.3	V	
Input DC-voltage (clamping)	$V_{IN1 - IN7}$	1.8	3.5	V	
Input DC-voltage (non clamping)	$V_{IN2, 3, 4}$	1.5	3.2	V	
Input source-impedance (clamping)	$RI_{IN1 - IN7}$	0	500	Ω	
I ² C-Bus clock	$f_{IN\ SDA, SCL}$	0	500	kHz	
Ambient temperature during operation	T_A	– 10	85	°C	

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 DC Characteristics

$$T_A = 25\text{ °C}, V_{CC} = 8.5\text{ V}$$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Total current consumption	I_{CC}		42	58	mA	$R_L = \infty$
Reference voltage (P-DSO-28-1 only)	V_{REF}	3.4	3.6	3.8	V	$R_L = \infty$
Output DC-voltage (clamping)	$V_{OUT1 - OUT5}$		1.8		V	$V_{C, IN1 - IN7} = 0\text{ Vpp}$
Output DC-voltage (output off)	$V_{OUT1 - OUT5}$		0.8		V	$V_{C, IN1 - IN7} = 0\text{ Vpp}$
Output current	$I_{OUT1 - OUT5}$	0.5	1.0	2.0	mA	$V_{OUT} = 2\text{ V},$ $I_n = 0\text{ Vpp}$
Input DC-voltage	V_C		1.8		V	$V_C = 0\text{ Vpp}$
Input DC-voltage (clamping)	$V_{IN1 - IN7}$		1.8		V	$V_{IN1 - IN7} = 0\text{ Vpp}$
Input current (clamping)	$I_{IN1 - IN7}$		0.33	1	μA	$I_{IN1 - IN7} = 0\text{ Vpp}$
Input DC-voltage (for ext. clamping override)	$V_{IN1 - IN7}$		2.4		V	$V_{IN1 - IN7} = 0\text{ Vpp}$
Input DC-voltage (non-clamping, Bus controlled)	$V_{IN2, 3, 4}$		2.4		V	$V_{IN2, 3, 4} = 0\text{ Vpp}$
Input current (SCL, SDA, address)	$I_{SDA, SCL}$ $I_{Address}$		0.1	0.4	μA	$V_{SDA, SCL} = 0\text{ V}$ $V_{Address} = 0\text{ V}$
Output current (SDA)	I_{SDA}	6			mA	$V_{SDA} = 0.6\text{ V}$
Output voltage low (SDA)	V_{SDA}	0	0.2	0.4	V	$I_{SDA} = 3\text{ mA sink}$
	V_{SDA}	0	0.3	0.6	V	$I_{SDA} = 3\text{ mA sink}$
SCL, SDA, address (96 hex) : high	$V_{SDA, SCL}$ $V_{Address}$	3.0		V_{CC}	V	
SCL, SDA, address (94 hex) : low	$V_{SDA, SCL}$ $V_{Address}$	0		1.5	V	
SCL, SDA, address (hysteresis)	$V_{SDA, SCL}$ $V_{Address}$	0.2		1	V	dependant on input frequency

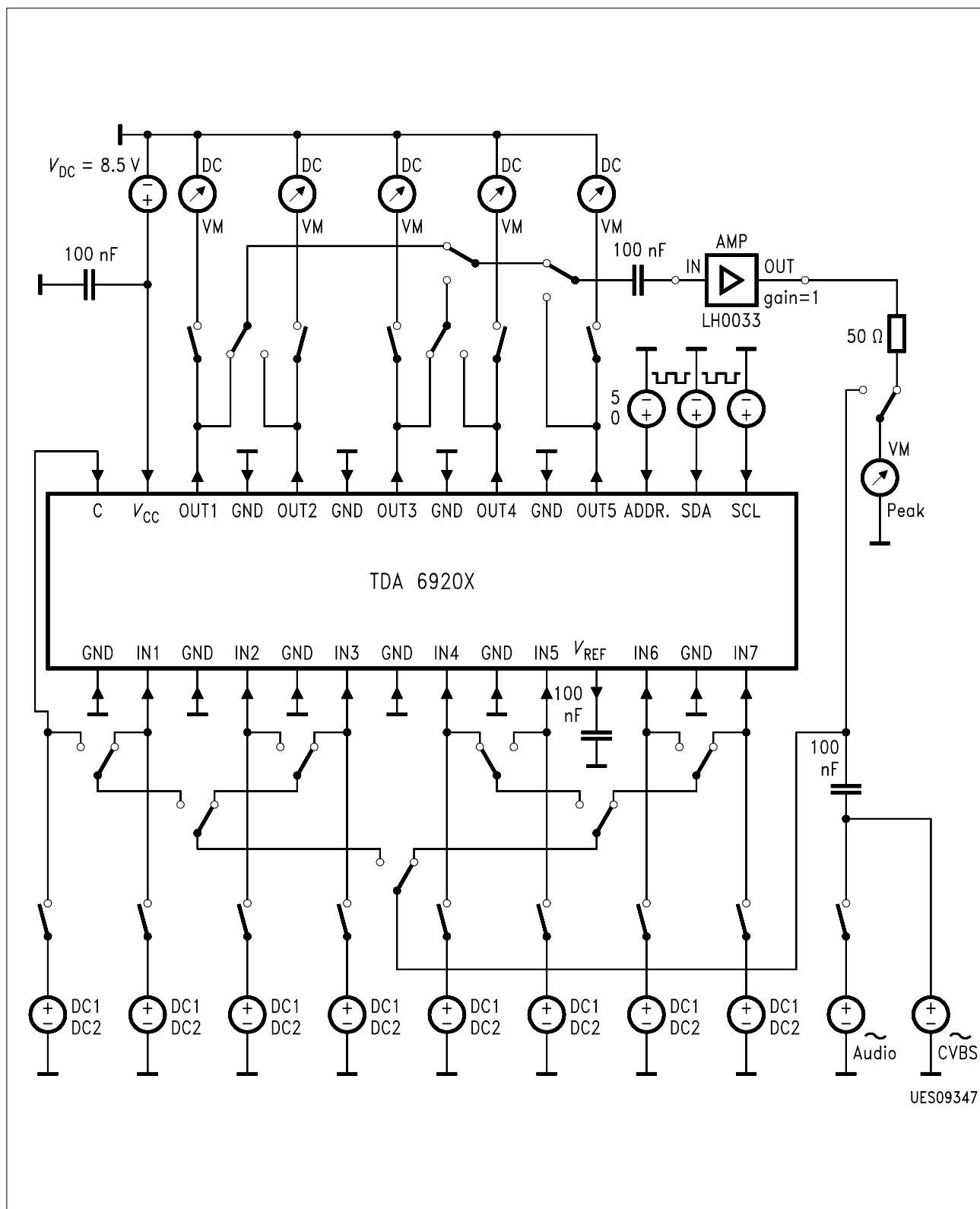
3.4 AC Characteristics

$$T_A = 25\text{ °C}, V_{CC} = 8.5\text{ V}$$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Video bandwidth	$P_{OUT/IN}$	15	20		MHz	– 3 dB point
Video gain	$V_{OUT/IN}$	1.9	2.0	2.1		
Crosstalk (0 - 5 MHz) P-DSO-28-1	A		– 65	– 60	dB	inputs 75 Ω to GND
Crosstalk (0 - 5 MHz) P-DSO-28-1	A		– 55	– 50	dB	inputs 500 Ω to GND
Crosstalk (0 - 5 MHz) P-DIP-18-5	A		– 62	– 60	dB	inputs 75 Ω to GND
Crosstalk (0 - 5 MHz) P-DIP-18-5	A		– 45	– 50	dB	inputs 500 Ω to GND
Input AC-voltage	V_C		0.75	1	Vpp	sinus
Input AC-voltage	$V_{IN1 - IN7}$		1	1.5	Vpp	clamped
Input AC-voltage (sinus)	$V_{IN2, 3, 4}$		1	1.5	Vpp	non clamped
Output AC-voltage	$V_{OUT1 - OUT5}$		2	3	Vpp	
I ² C-Bus clock	$f_{IN\ SDA, SCL}$		400	500	kHz	
Output linearity	$DG_{OUT1 - OUT5}$		0.2	1	%	$R_L = \infty$
Input resistance (non-clamping)	$R_{C, IN2, 3, 4}$	40	50		k Ω	
Input source-impedance (clamping)	$R_{IN1 - IN7}$	0	75	500	Ω	
Input coupling-capacitor (clamping)	$C_{IN1 - IN7}$		47 10		nF μ F	CVBS-signal > 20 Hz Audiosignal
Output dyn. impedance	$R_{OUT1 - OUT5}$		50	75	Ω	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\text{ °C}$ and the given supply voltage.

4 Test Circuits



UES09347

Figure 3
Test Circuit (P-DSO-28-1)

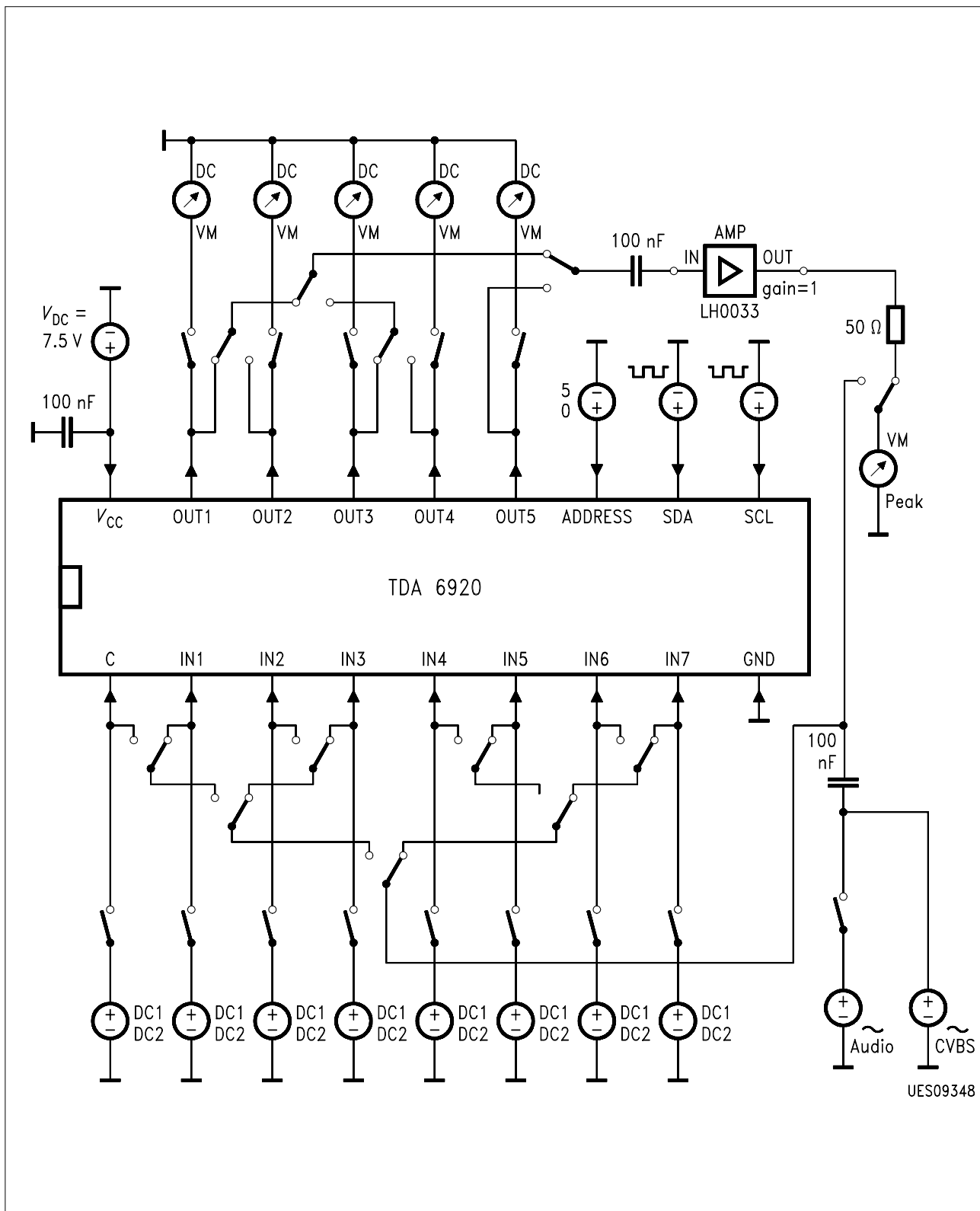


Figure 4
Test Circuit (P-DIP-18-5)

5 Application Circuits

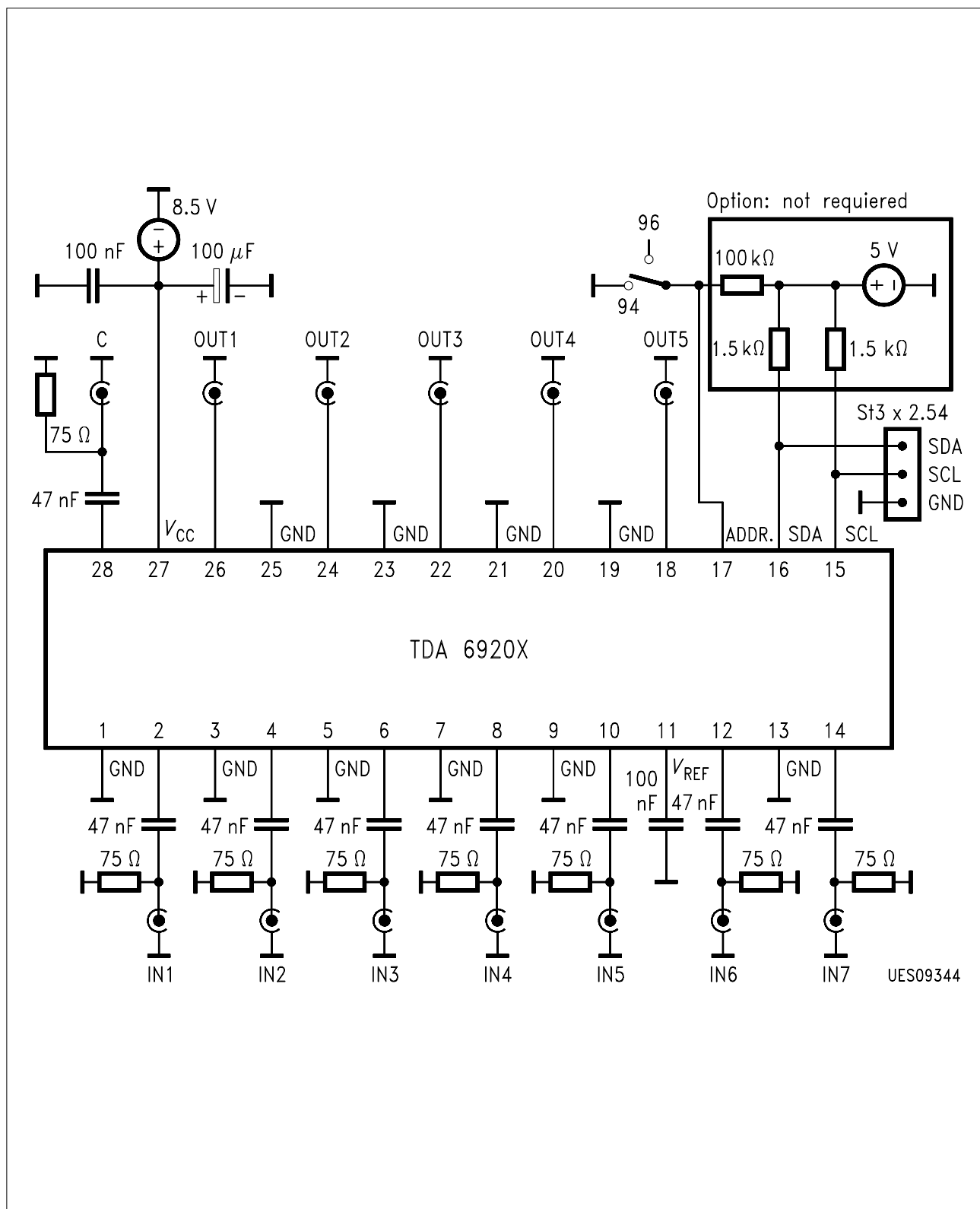


Figure 5 Application Circuit P-DSO-28-1 (clamping inputs)

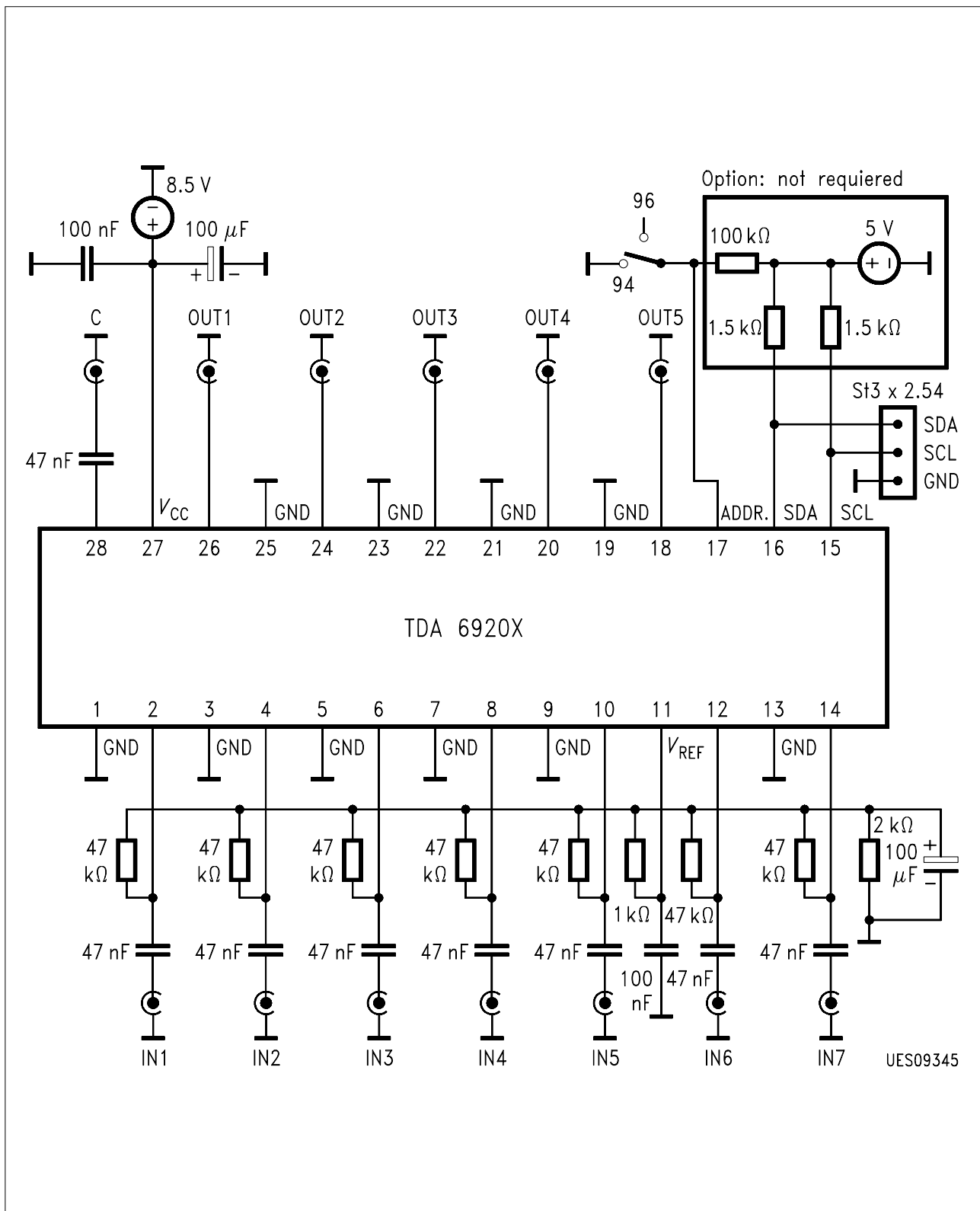
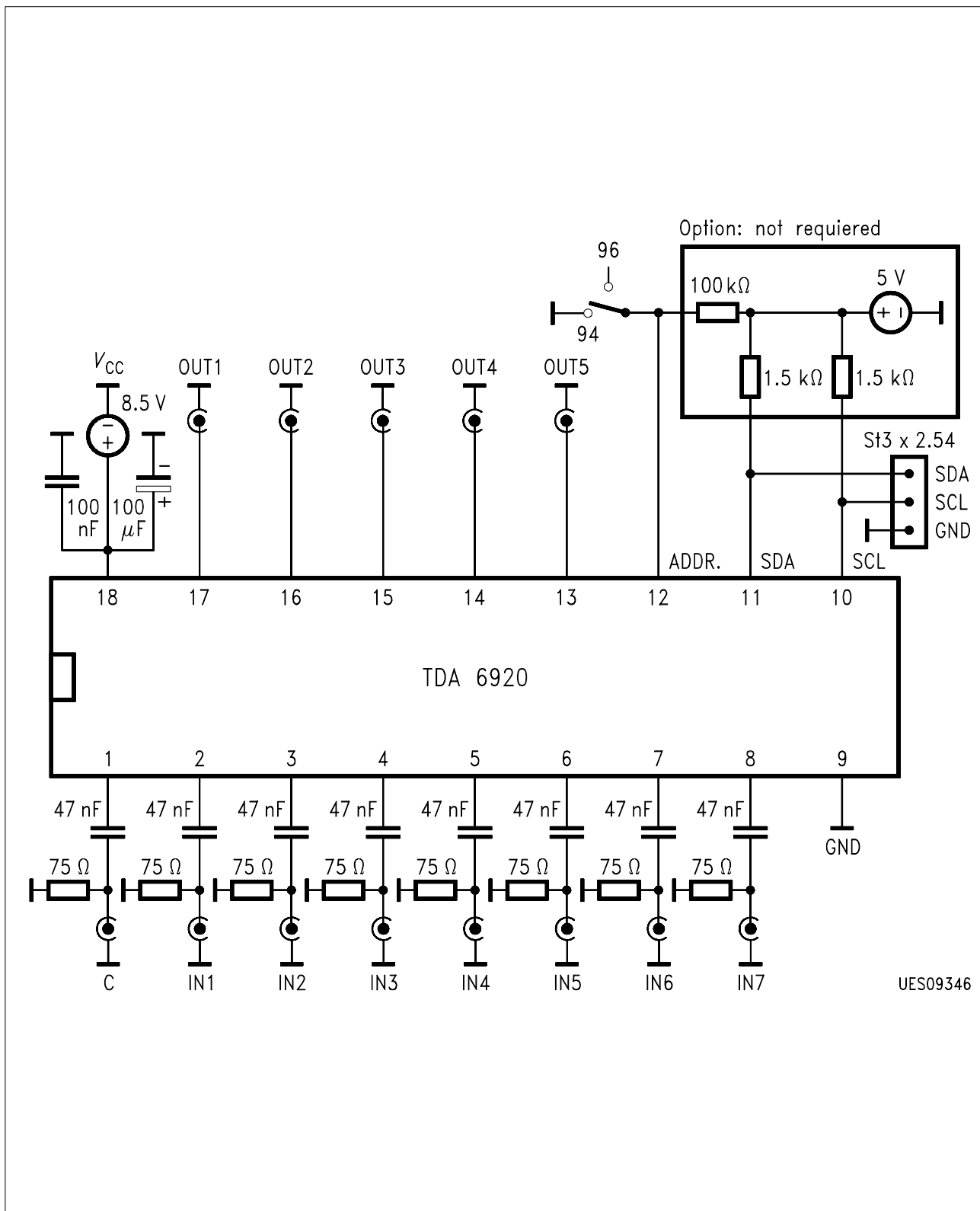


Figure 6
Application Circuit P-DSO-28-1 (no clamping inputs with clamping override)

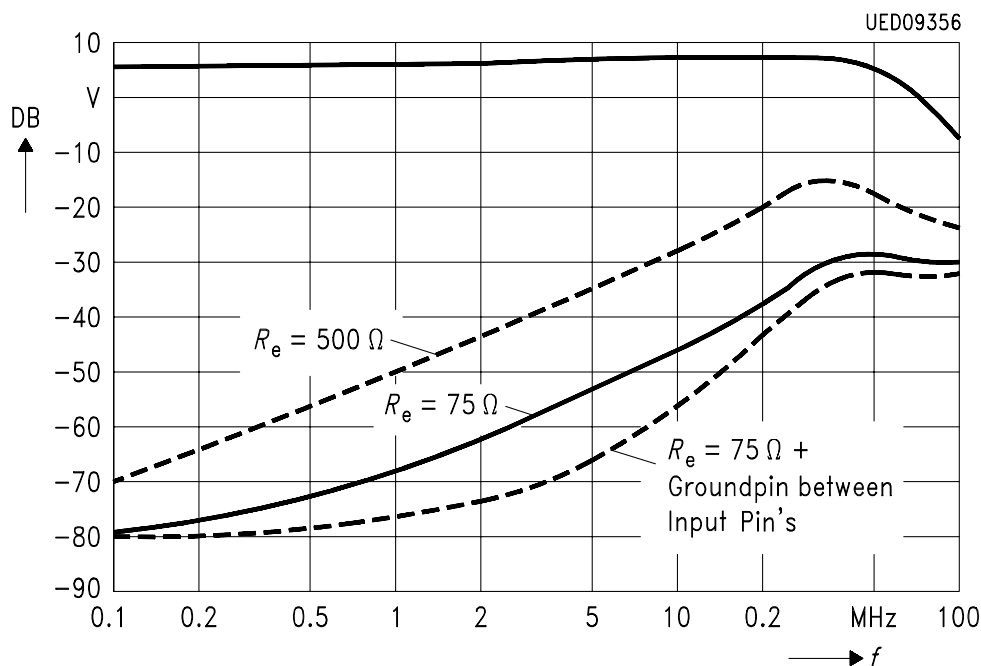


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Figure 7
Application Circuit (P-DIP-18-5)

6 Electrical Diagrams

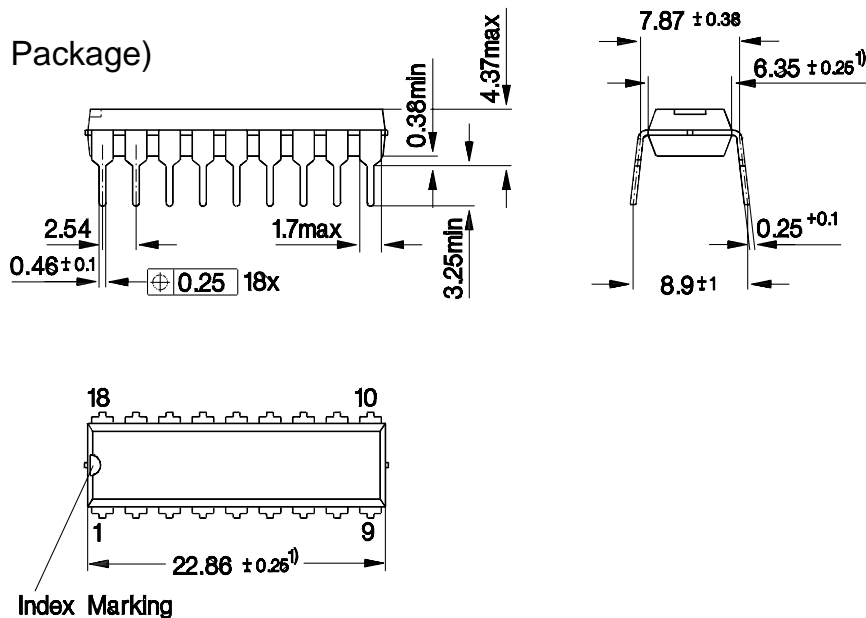
Typical frequency response and crosstalk (simulated) for P-DSO-28-1 package



Conditions: $V_{CC} = 8.5 \text{ V}$, all outputs selected to one different input;
 response: the measured output has max. signal on the selected input;
 crosstalk: the measured output has no signal on the selected input, another input has max. signal

7 Package Outlines

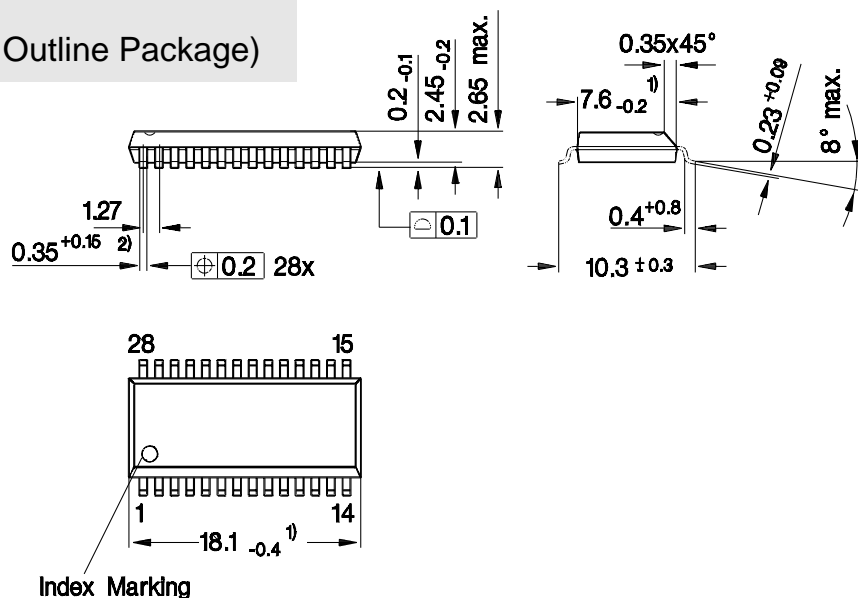
P-DIP-18-5
(Plastic Dual in-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05586

P-DSO-28-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05123

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm