MAX5309EUE
Rev. A

RELIABILITY REPORT

FOR

MAX5309EUE

PLASTIC ENCAPSULATED DEVICES

March 30, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX5309 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX5309 is a10-bit, eight channel, low-power, voltage-output, digital-to-analog converters (DAC) in a space-saving 16-pin TSSOP package. The wide +2.7V to +5.5V supply voltage range and less than 215µA (max) supply current per DAC is excellent for low-power and low-voltage applications. The low 2nV-s glitch energy of the MAX5309 makes it ideal for digital control of fast-response, closed-loop systems.

The MAX5309 has a hardware reset input (CLR-bar) which clears all registers and DACs to zero. The MAX5309 has a software shutdown feature that reduces the supply current to 1µA. The MAX5308 features a load DAC (LDAC-bar) function that updates the output of all eight DACs simultaneously.

The 3-wire SPI™, QSPI™, MICROWIRE™ and DSP-compatible serial interface allows the input and DAC registers to be updated independently or simultaneously with a single software command. This device uses a double-buffered design to minimize the digital-noise feedthrough from the digital inputs to the outputs. The MAX5309 operating temperature range is from -40°C to +85°C

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
All Other Pins to GND	-0.3V to (VDD + 0.3V)
Maximum Current Into Any Pin	±50mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin TSSOP	775mW
Derates above +70°C	
16-Pin TSSOP	9.4mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Power, Low-Glitch, Octal 10-Bit Voltage-Output DACs with Serial Interface
B. Process:	S6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	19,000
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	**16-Pin TSSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3901-0002
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1

IV. Die Information

A. Dimensions:	102 x 141 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 79 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.75 \times 10^{-9}$

$\lambda = 13.75$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5814) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DB06 die type has been found to have all pins able to withstand a transient pulse of ±1500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX5309EUE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		79	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

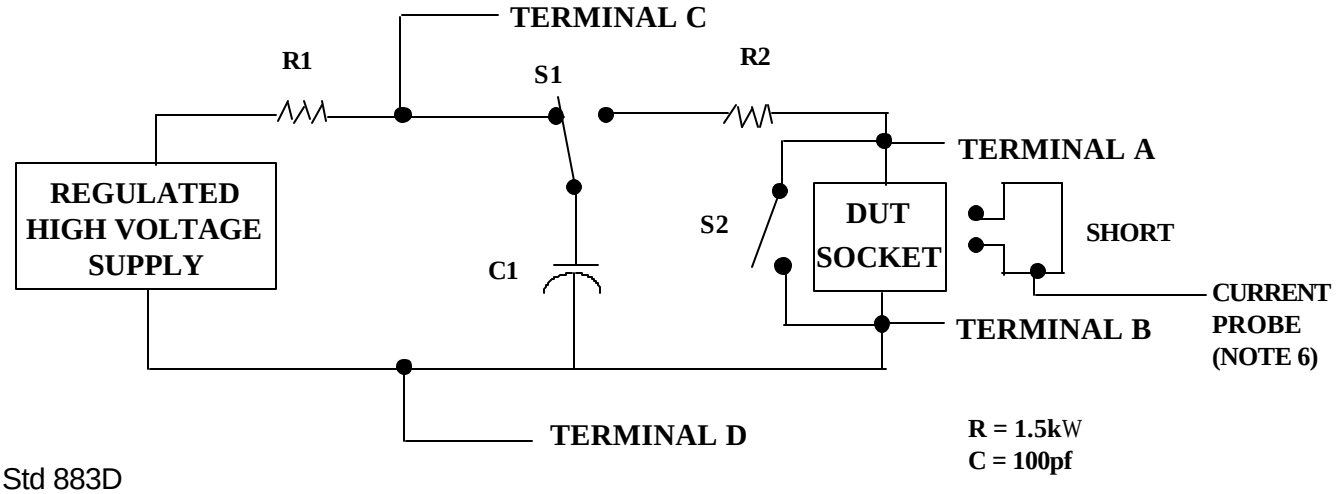
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

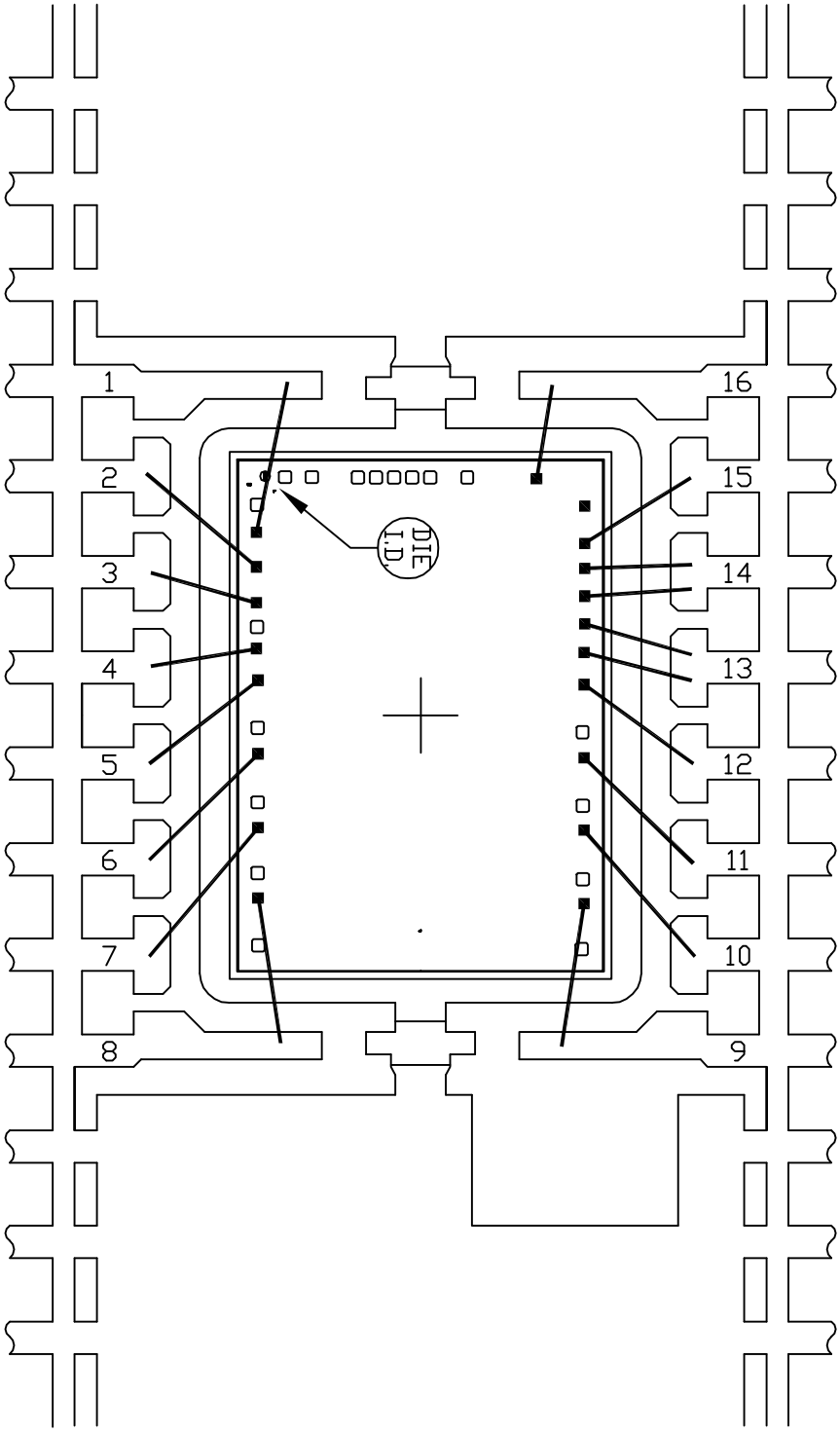
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

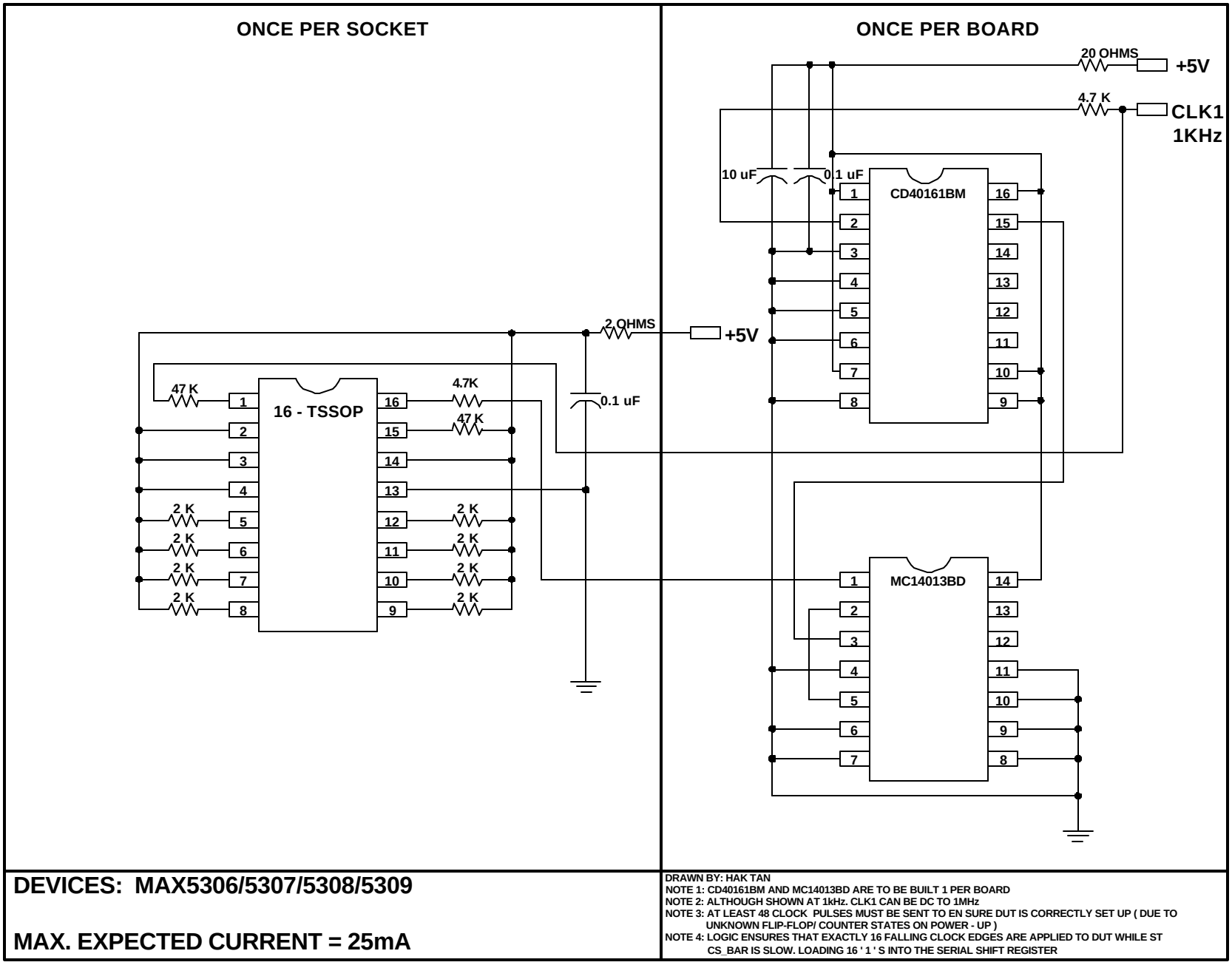
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: U16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118X154	PKG.			BOND DIAGRAM #: 05-3901-0002	REV: A
	DESIGN				


ONCE PER SOCKET
ONCE PER BOARD
20 OHMS
+5V
4.7 K
CLK1
1KHz
10 uF
0.1 uF
CD40161BM
2 OHMS
+5V
47 K
16 - TSSOP
4.7K
47 K
0.1 uF
2 K
2 K
2 K
2 K
2 K
2 K
2 K
2 K
MC14013BD
DEVICES: MAX5306/5307/5308/5309
MAX. EXPECTED CURRENT = 25mA
DRAWN BY: HAK TAN
NOTE 1: CD40161BM AND MC14013BD ARE TO BE BUILT 1 PER BOARD
NOTE 2: ALTHOUGH SHOWN AT 1kHz. CLK1 CAN BE DC TO 1MHz
NOTE 3: AT LEAST 48 CLOCK PULSES MUST BE SENT TO EN SURE DUT IS CORRECTLY SET UP (DUE TO UNKNOWN FLIP-FLOP/ COUNTER STATES ON POWER - UP)
NOTE 4: LOGIC ENSURES THAT EXACTLY 16 FALLING CLOCK EDGES ARE APPLIED TO DUT WHILE ST CS_BAR IS SLOW. LOADING 16 ' 1 ' S INTO THE SERIAL SHIFT REGISTER