

LH521028

CMOS 64K × 18 Static RAM

FEATURES

- Fast Access Times: 17/20/25/35 ns
- Wide Word (18-Bits) for:
 - Improved Performance
 - Reduced Component Count
 - Nine-bit Byte for Parity
- Transparent Address Latch
- Reduced Loading on Address Bus
- Low-Power Stand-by Mode when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- 2 V Data Retention
- JEDEC Standard Pinout
- Package: 52-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH521028 is a high-speed 1,179,648-bit CMOS SRAM organized as 64K × 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The LH521028 is available in a compact 52-Pin PLCC, which along with the six pairs of supply terminals, provide for reliable operation.

The control signals include Write Enable (\overline{W}), Chip Enable (\overline{E}), High and Low Byte Select (\overline{S}_L and \overline{S}_H), Output Enable (\overline{G}) and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte-parity with no additional RAM required.

This RAM is fully static in operation. The Chip Enable (\overline{E}) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). The Byte-select controls, \overline{S}_H and \overline{S}_L , are also used to enable or disable Read and Write

operations on the high and the low bytes. The Address Latches are transparent when ALE is HIGH (for applications not requiring a latch), and are latched when ALE is LOW. The Address Latches and the wide word help to eliminate the need for external Addressbusbuffers and/or latches.

Write cycles occur when Chip Enable (\overline{E}), \overline{S}_H and/or \overline{S}_L , and Write Enable (\overline{W}) are LOW. The Byte-select signals can be used for Byte-write operations by disabling the other byte during the Write operation. Data is transferred from the DQ pins to the memory location specified by the 16 address lines. The proper use of the Output Enable control (\overline{G}) can prevent bus contention.

When \overline{E} and either \overline{S}_H or \overline{S}_L are LOW and \overline{W} is HIGH, a static Read will occur at the memory location specified by the address lines. \overline{G} must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address with ALE HIGH.

PIN CONNECTIONS

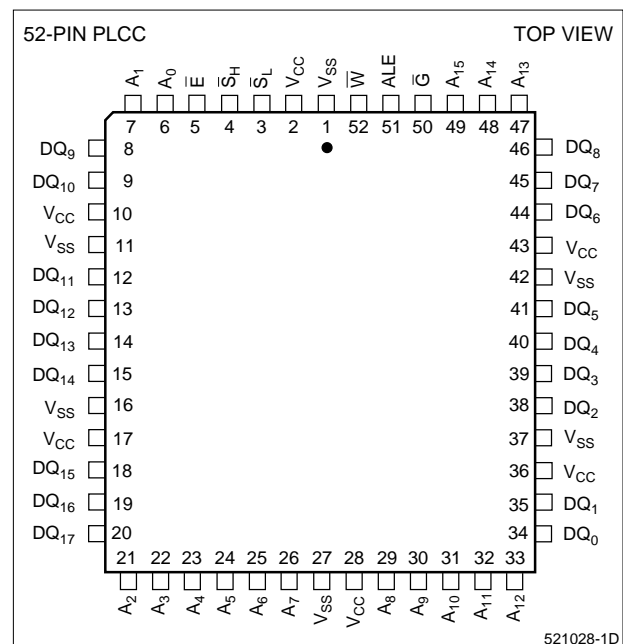
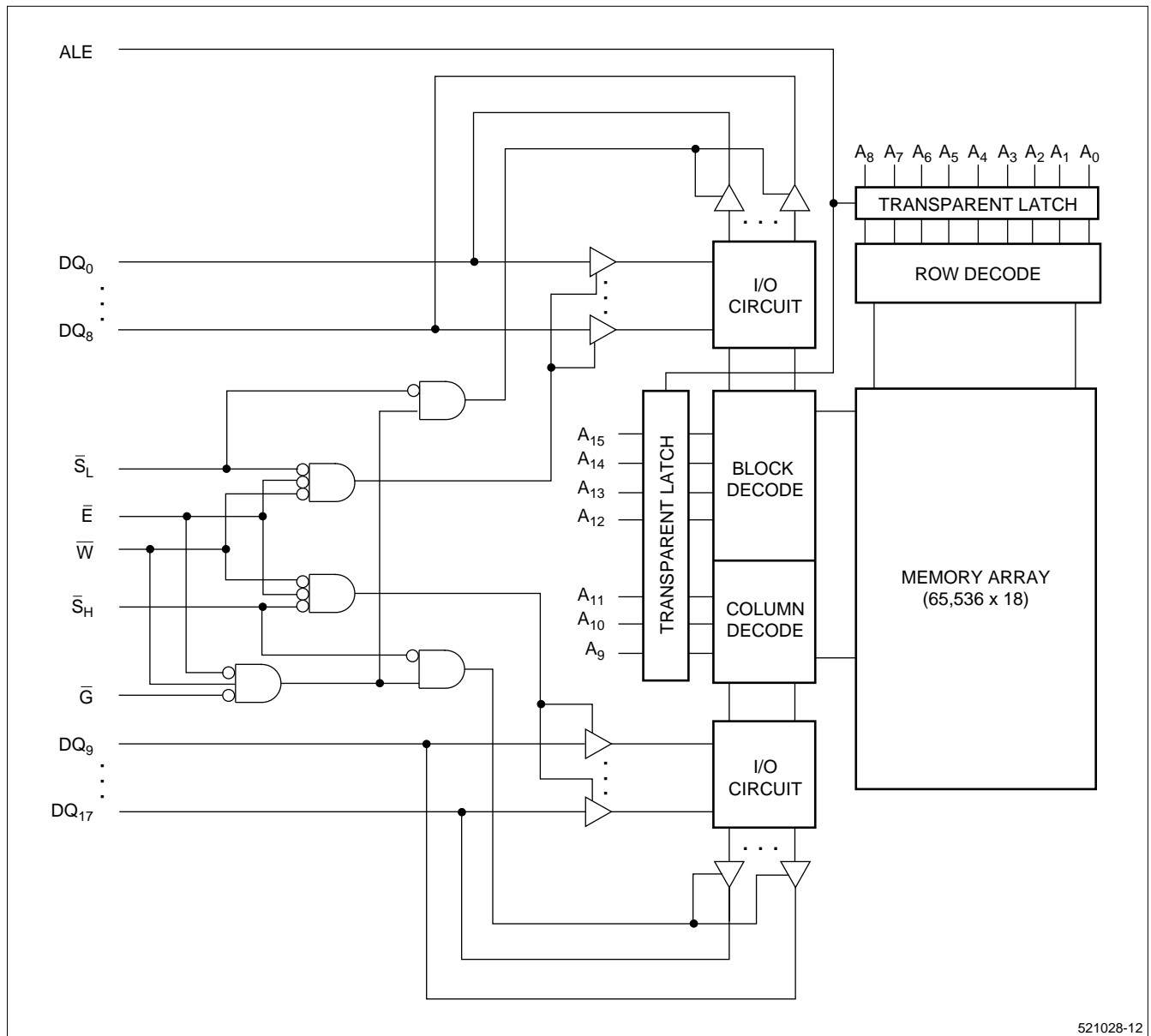


Figure 1. Pin Connections for PLCC Package



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Figure 2. LH521028 Block Diagram

TRUTH TABLE

| ADDRESS | \bar{E} | \bar{S}_H | \bar{S}_L | ALE | \bar{G} | \bar{W} | DQ ₀ -DQ ₈ | DQ ₉ -DQ ₁₇ | MODE | I _{CC} |
|------------|-----------|-------------|-------------|-----|-----------|-----------|----------------------------------|-----------------------------------|-------------------|------------------|
| Don't Care | H | X | X | H | X | X | High-Z | High-Z | Standby | I _{SB} |
| Valid | L | L | H | H | L | H | Active | High-Z | Read | I _{CC1} |
| Valid | L | H | L | H | L | H | High-Z | Active | Read | I _{CC1} |
| Valid | L | L | L | H | L | H | Active | Active | Read | I _{CC1} |
| Valid | L | L | L | H | H | H | High-Z | High-Z | Read | I _{CC1} |
| Don't Care | L | L | L | L | L | H | Data Out | Data Out | Read | I _{CC1} |
| Valid | L | L | H | H | X | L | Data In | Don't Care | Write, low byte | I _{CC1} |
| Valid | L | H | L | H | X | L | Don't Care | Data In | Write, high byte | I _{CC1} |
| Valid | L | L | L | H | X | L | Data In | Data In | Write, both bytes | I _{CC1} |
| Valid | L | H | H | H | X | L | Don't Care | Don't Care | Write, inhibited | I _{CC1} |
| Don't Care | L | L | L | L | X | L | Data In | Data In | Write, both bytes | I _{CC1} |

NOTE:

X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

| PIN | SIGNAL |
|-----|------------------|
| 1 | V _{SS} |
| 2 | V _{CC} |
| 3 | \bar{S}_L |
| 4 | \bar{S}_H |
| 5 | \bar{E} |
| 6 | A ₀ |
| 7 | A ₁ |
| 8 | DQ ₉ |
| 9 | DQ ₁₀ |
| 10 | V _{CC} |
| 11 | V _{SS} |
| 12 | DQ ₁₁ |
| 13 | DQ ₁₂ |

| PIN | SIGNAL |
|-----|------------------|
| 14 | DQ ₁₃ |
| 15 | DQ ₁₄ |
| 16 | V _{SS} |
| 17 | V _{CC} |
| 18 | DQ ₁₅ |
| 19 | DQ ₁₆ |
| 20 | DQ ₁₇ |
| 21 | A ₂ |
| 22 | A ₃ |
| 23 | A ₄ |
| 24 | A ₅ |
| 25 | A ₆ |
| 26 | A ₇ |

| PIN | SIGNAL |
|-----|-----------------|
| 27 | V _{SS} |
| 28 | V _{CC} |
| 29 | A ₈ |
| 30 | A ₉ |
| 31 | A ₁₀ |
| 32 | A ₁₁ |
| 33 | A ₁₂ |
| 34 | DQ ₀ |
| 35 | DQ ₁ |
| 36 | V _{CC} |
| 37 | V _{SS} |
| 38 | DQ ₂ |
| 39 | DQ ₃ |

| PIN | SIGNAL |
|-----|-----------------|
| 40 | DQ ₄ |
| 41 | DQ ₅ |
| 42 | V _{SS} |
| 43 | V _{CC} |
| 44 | DQ ₆ |
| 45 | DQ ₇ |
| 46 | DQ ₈ |
| 47 | A ₁₃ |
| 48 | A ₁₄ |
| 49 | A ₁₅ |
| 50 | \bar{G} |
| 51 | ALE |
| 52 | \bar{W} |

ABSOLUTE MAXIMUM RATINGS¹

| PARAMETER | RATING |
|--|-----------------------------------|
| V _{CC} to V _{SS} Potential | −0.5 V to 7 V |
| Input Voltage Range | −0.5 V to V _{CC} + 0.5 V |
| DC Output Current ² | ± 40 mA |
| Storage Temperature Range | −65°C to 150°C |
| Power Dissipation (Package Limit) | 2 W |

NOTES:

- Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------------|------|-----|-----------------------|------|
| T _A | Temperature, Ambient | 0 | | 70 | °C |
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{SS} | Supply Voltage | 0 | 0 | 0 | V |
| V _{IL} | Logic '0' Input Voltage ¹ | −0.5 | | 0.8 | V |
| V _{IH} | Logic '1' Input Voltage | 2.2 | | V _{CC} + 0.5 | V |

NOTE:

- Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------------------------|---|-----|-----|-----|------|
| I _{CC1} | Operating Current ¹ | t _{CYCLE} = minimum | | | 300 | mA |
| I _{SB1} | Standby Current | $\bar{E} \geq V_{CC} - 0.2 V$ $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$ f = 0 | | | 4 | mA |
| I _{SB2} | Standby Current | $\bar{E} \geq V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL} | | | 50 | mA |
| I _{LI} | Input Leakage Current | V _{IN} = 0 V to V _{CC} | −2 | | 2 | μA |
| I _{LO} | I/O Leakage Current | V _{IN} = 0 V to V _{CC} | −2 | | 2 | μA |
| V _{OH} | Output High Voltage | I _{OH} = −4.0 mA | 2.4 | | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 8.0 mA | | | 0.4 | V |

NOTE:

- I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

| PARAMETER | RATING |
|-------------------------------------|------------------------|
| Input Pulse Levels | V _{SS} to 3 V |
| Input Rise and Fall Times | 5 ns |
| Input and Output Timing Ref. Levels | 1.5 V |
| Output Load, Timing Tests | Figure 3 |

CAPACITANCE^{1,2}

| PARAMETER | RATING |
|-------------------------------------|--------|
| C _{IN} (Input Capacitance) | 5 pF |
| C _{DQ} (I/O Capacitance) | 7 pF |

NOTES:

- Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
- Guaranteed but not tested.

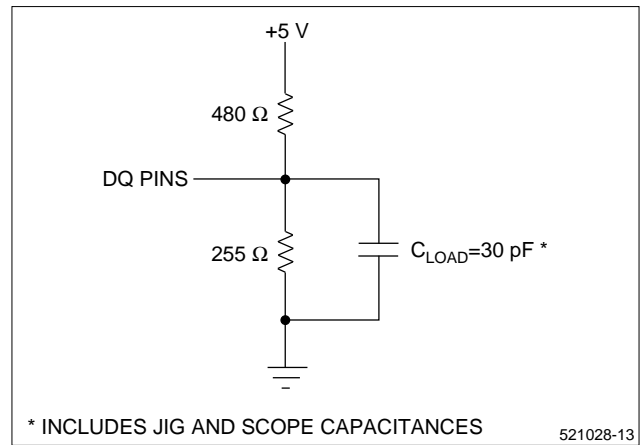


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS¹ (Over Operating Range)

| SYMBOL | DESCRIPTION | -17 | | -20 | | -25 | | -35 | | UNITS |
|--------------------|--|-----|-----|-----|-----|-----|-----|-----|-----|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| READ CYCLE | | | | | | | | | | |
| t _{RC} | Read Cycle Timing | 17 | | 20 | | 25 | | 35 | | ns |
| t _{AA} | Address Access Time | | 17 | | 20 | | 25 | | 35 | ns |
| t _{ASL} | Address Setup to Latch Enable | 3 | | 3 | | 3 | | 3 | | ns |
| t _{AHL} | Address Hold from Latch Enable | 4 | | 5 | | 6 | | 6 | | ns |
| t _{LEA} | Latch Enable to Data Valid | | 19 | | 22 | | 27 | | 37 | ns |
| t _{LHM} | Latch Enable High Pulse Width | 5 | | 5 | | 6 | | 6 | | ns |
| t _{OH} | Output Hold from Address Change | 3 | | 5 | | 5 | | 5 | | ns |
| t _{LH} | Output Hold from Latch High | 4 | | 7 | | 7 | | 7 | | ns |
| t _{EA} | \bar{E} Low to Valid Data | | 17 | | 20 | | 25 | | 35 | ns |
| t _{ELZ} | \bar{E} Low to Output Active ^{2,3} | 3 | | 3 | | 3 | | 3 | | ns |
| t _{EHZ} | \bar{E} High to Output High-Z ^{2,3} | | 10 | | 10 | | 12 | | 20 | ns |
| t _{SA} | \bar{S} Low to Valid Data | | 9 | | 10 | | 12 | | 20 | ns |
| t _{SLZ} | \bar{S} Low to Output Active ^{2,3} | 2 | | 2 | | 3 | | 3 | | ns |
| t _{SHZ} | \bar{S} High to Output High-Z ^{2,3} | | 10 | | 10 | | 12 | | 20 | ns |
| t _{GA} | \bar{G} Low to Valid Data | | 8 | | 9 | | 12 | | 20 | ns |
| t _{GLZ} | \bar{G} Low to Output Active ^{2,3} | 0 | | 0 | | 0 | | 0 | | ns |
| t _{GHZ} | \bar{G} High to Output High-Z ^{2,3} | | 8 | | 8 | | 10 | | 20 | ns |
| t _{RCS} | Read Setup from \bar{W} High | 0 | | 0 | | 0 | | 0 | | ns |
| t _{RCH} | Read Hold from \bar{W} Low | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PU} | \bar{E} LOW to Power Up Time ³ | 0 | | 0 | | 0 | | 0 | | ns |
| t _{PD} | \bar{E} HIGH to Power Down Time ³ | | 17 | | 20 | | 25 | | 35 | ns |
| t _{WA} | Access Time From Write Enable HIGH | | 20 | | 25 | | 28 | | 35 | ns |
| WRITE CYCLE | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 17 | | 20 | | 25 | | 35 | | ns |
| t _{EW} | \bar{E} Low to End of Write | 13 | | 15 | | 20 | | 30 | | ns |
| t _{SW} | \bar{S} LOW to End of Write | 13 | | 15 | | 20 | | 30 | | ns |
| t _{AW} | Address Valid to End of Write | 13 | | 15 | | 20 | | 30 | | ns |
| t _{AS} | Address Setup to Start of Write | 0 | | 0 | | 0 | | 0 | | ns |
| t _{AH} | Address Hold from End of Write | 0 | | 0 | | 0 | | 0 | | ns |
| t _{ASL} | Address Setup to Latch Enable | 3 | | 3 | | 3 | | 3 | | ns |
| t _{AHL} | Address Hold from Latch Enable | 4 | | 5 | | 6 | | 6 | | ns |
| t _{LHW} | Latch Hold from \bar{W} High | 0 | | 0 | | 0 | | 0 | | ns |
| t _{LHM} | Latch Enable HIGH Pulse Width | 5 | | 5 | | 6 | | 6 | | ns |
| t _{WP} | \bar{W} Pulse Width | 13 | | 15 | | 20 | | 30 | | ns |
| t _{DW} | Input Data Setup Time | 9 | | 12 | | 13 | | 15 | | ns |
| t _{DH} | Input Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| t _{WHZ} | \bar{W} Low to Output High-Z ^{2,3} | | 8 | | 8 | | 10 | | 14 | ns |
| t _{WLZ} | \bar{W} High to Output Active ^{2,3} | 3 | | 3 | | 3 | | 3 | | ns |

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ± 500 mV transition from steady state levels into the test load.
C_{Load} = 5 pF.
3. Guaranteed but not tested.

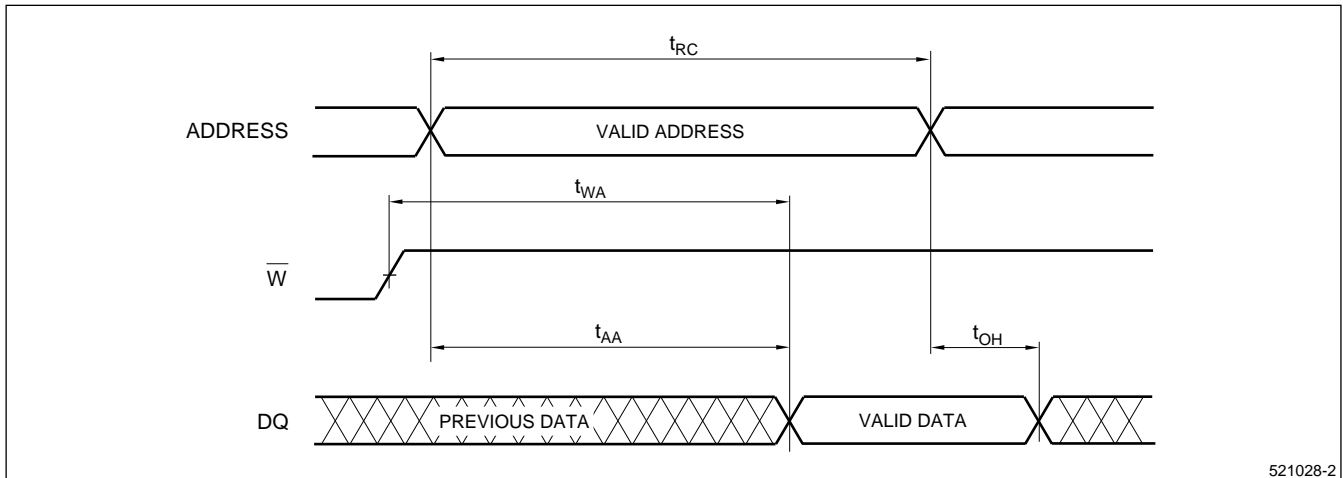
TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1 (Unlatched Address Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode), \bar{E} and \bar{G} are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following a \bar{W} -controlled Write cycle, t_{WA} and t_{AA} must both be satisfied to ensure valid data. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA} .

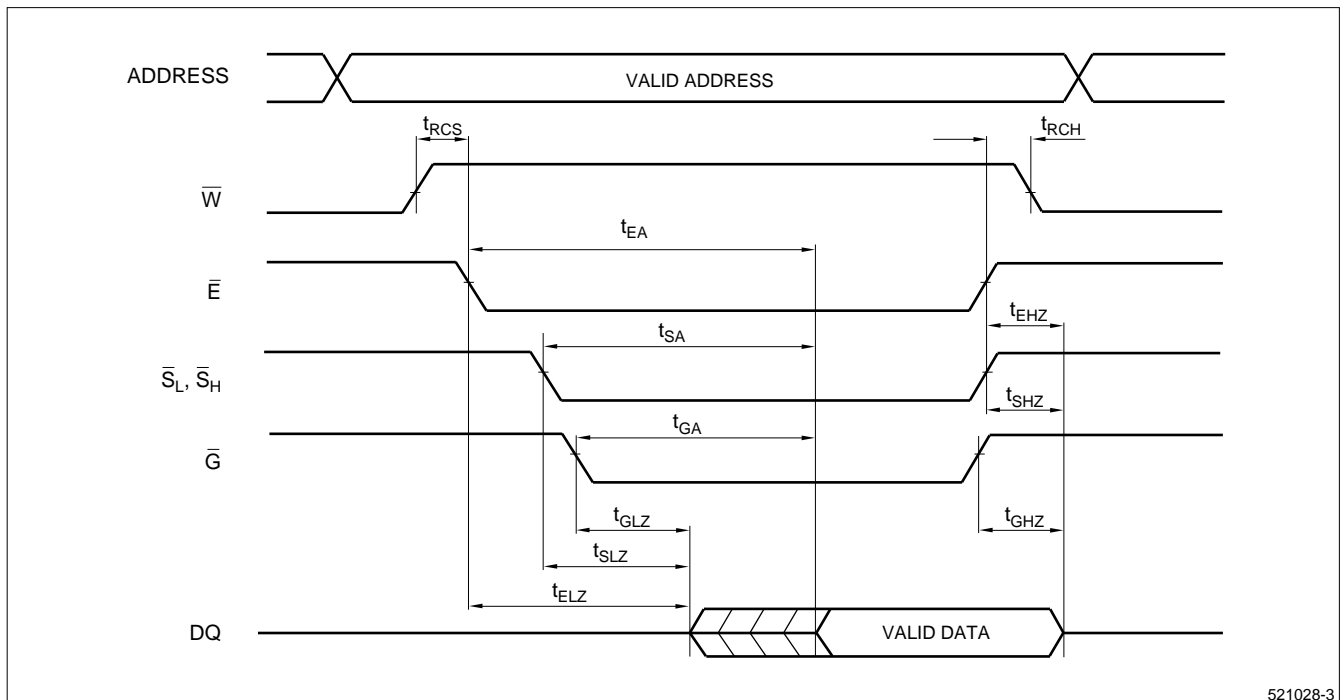
Read Cycle No. 2 (Unlatched Chip Enable Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode). Read cycle timing is referenced from when \bar{E} , \bar{S} , and \bar{G} are stable until the first address transition. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.



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Figure 4. Read Cycle No. 1



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Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 3 (Latched Address Controlled Read)

Chip is in Read Mode: \overline{W} is HIGH, \overline{E} , \overline{S}_H , \overline{S}_L and \overline{G} are LOW. Both t_{AA} and t_{LEA} must be met before valid data is available. If the address is valid prior to the rising edge of

ALE, then the access time is t_{LEA} . If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is t_{AA} . Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA} .

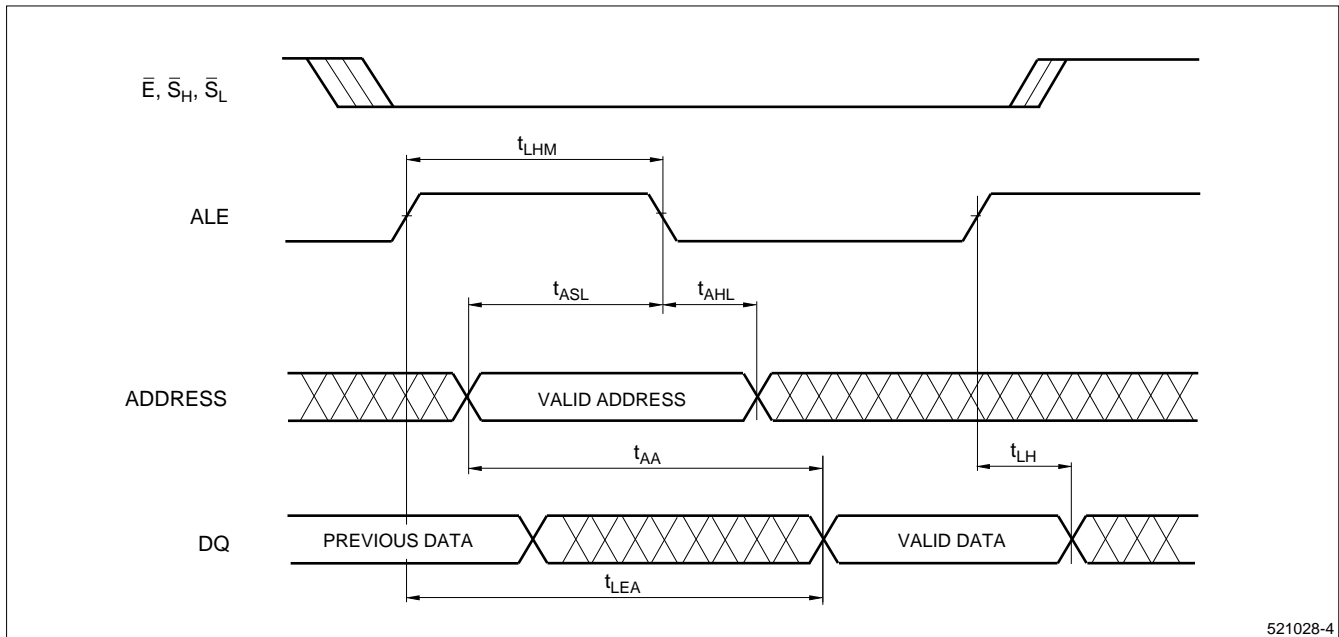


Figure 6. Read Cycle No. 3

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 4

Chip is in Read Mode: Timing illustrated for the case when addresses are valid before \bar{E} goes LOW. Data Out is not specified to be valid until t_{EA} , t_{SA} and t_{GA} , but may become active as early as t_{ELZ} , t_{SLZ} or t_{GLZ} .

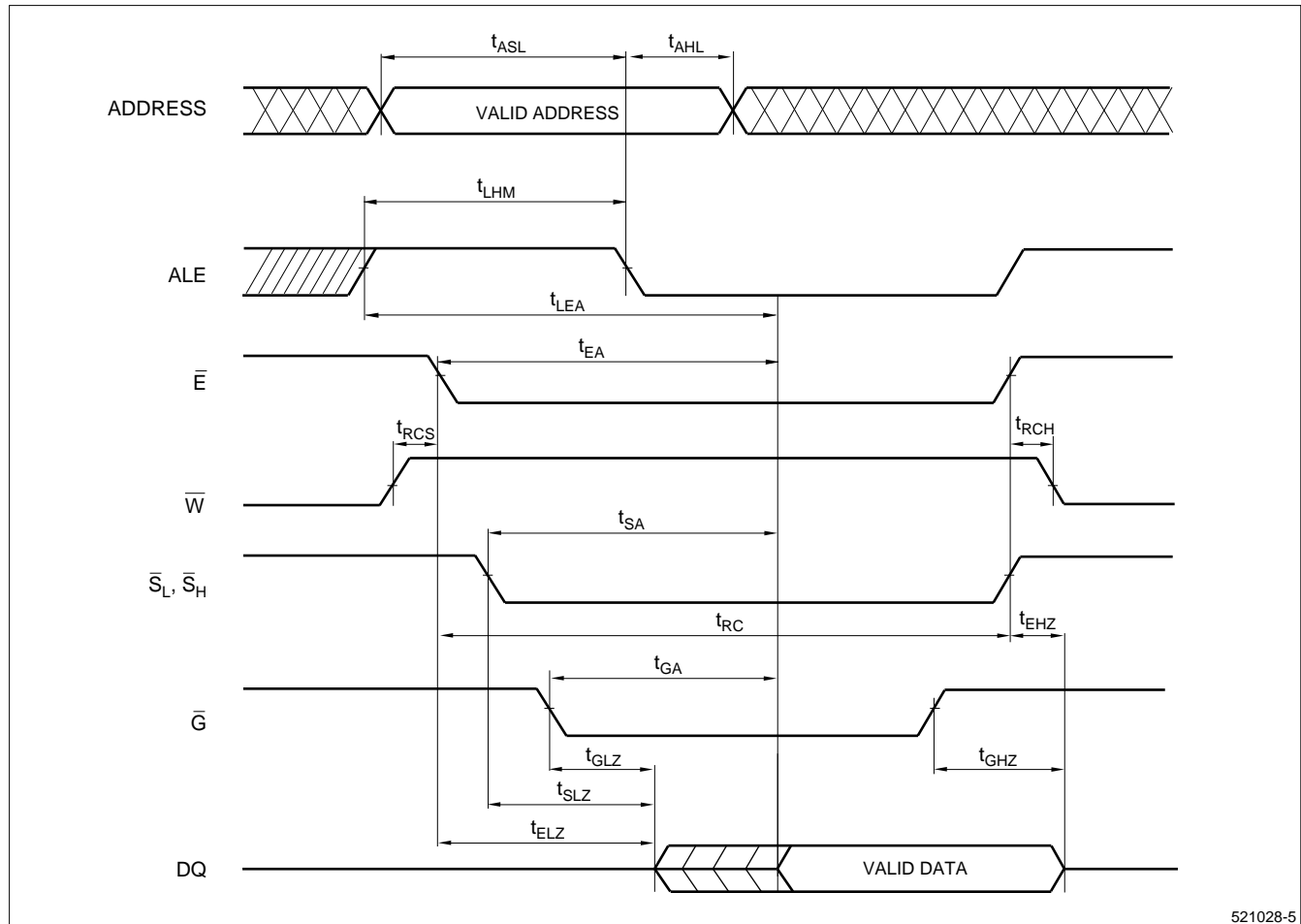


Figure 7. Read Cycle No. 4

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if \overline{W} is LOW when \overline{E} and $\overline{S}_H / \overline{S}_L$ go LOW. If \overline{G} is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with \overline{G} active, it is recommended that \overline{G} be held HIGH for all Write cycles. This will prevent the LH521028's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 (Unlatched \overline{W} Controlled Write)

Chip is selected: \overline{E} , \overline{G} , and $\overline{S}_H / \overline{S}_L$ are LOW, ALE is High. Using only \overline{W} to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 (\overline{E} , \overline{S}_L , \overline{S}_H Controlled Write)

\overline{G} is LOW. DQ lines may transition to Low-Z if the falling edge of \overline{W} occurs after the falling edge of \overline{E} , $\overline{S}_H / \overline{S}_L$ if \overline{G} is LOW.

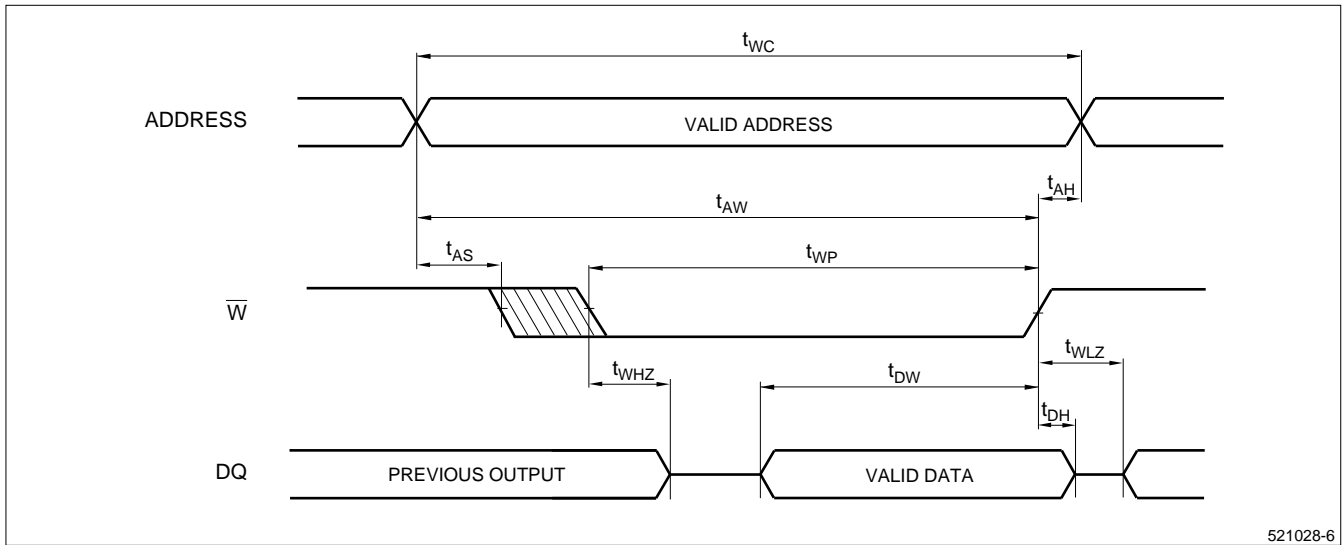


Figure 8. Write Cycle No. 1

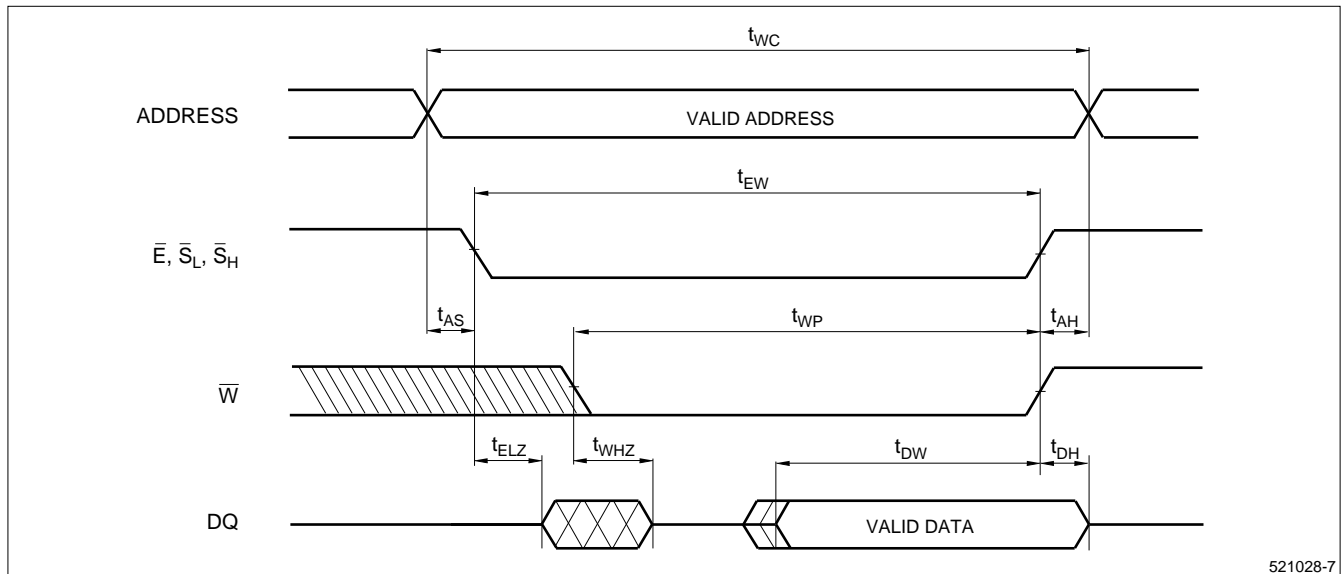


Figure 9. Write Cycle No. 2

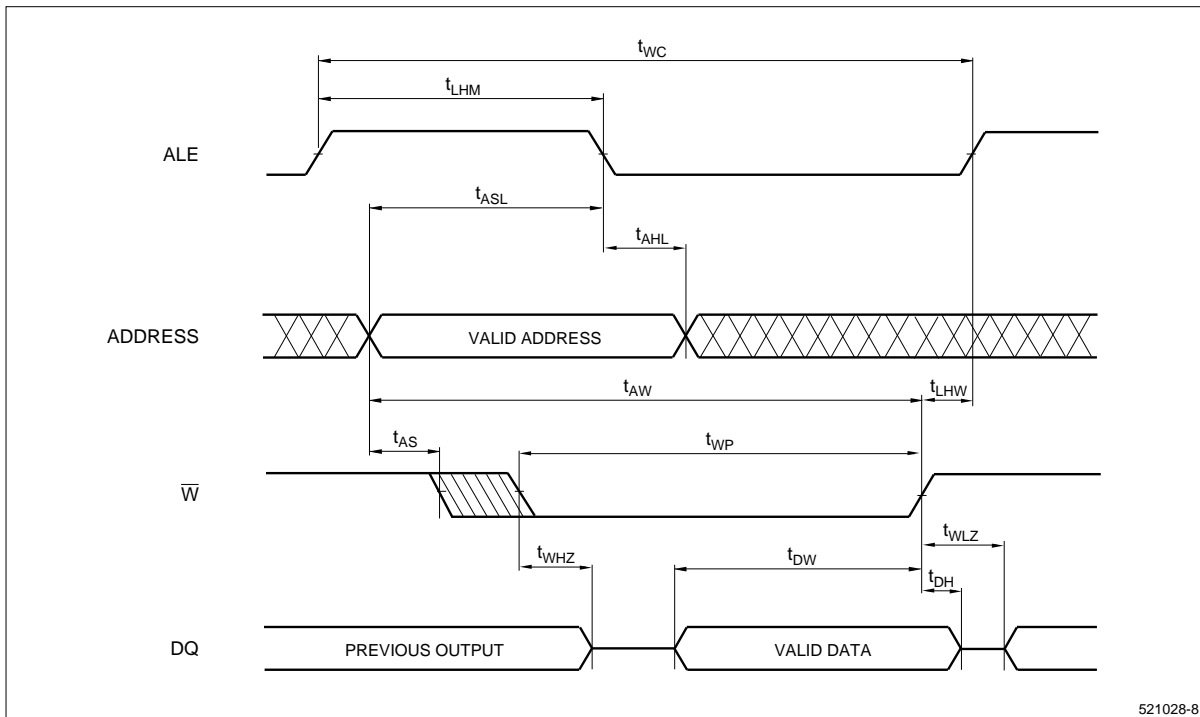
TIMING DIAGRAMS – WRITE CYCLE (cont'd)

Write Cycle No. 3 (Latched \overline{W} Controlled Write)

Chip is selected: \overline{E} , \overline{G} , and $\overline{S}_H / \overline{S}_L$ are LOW.

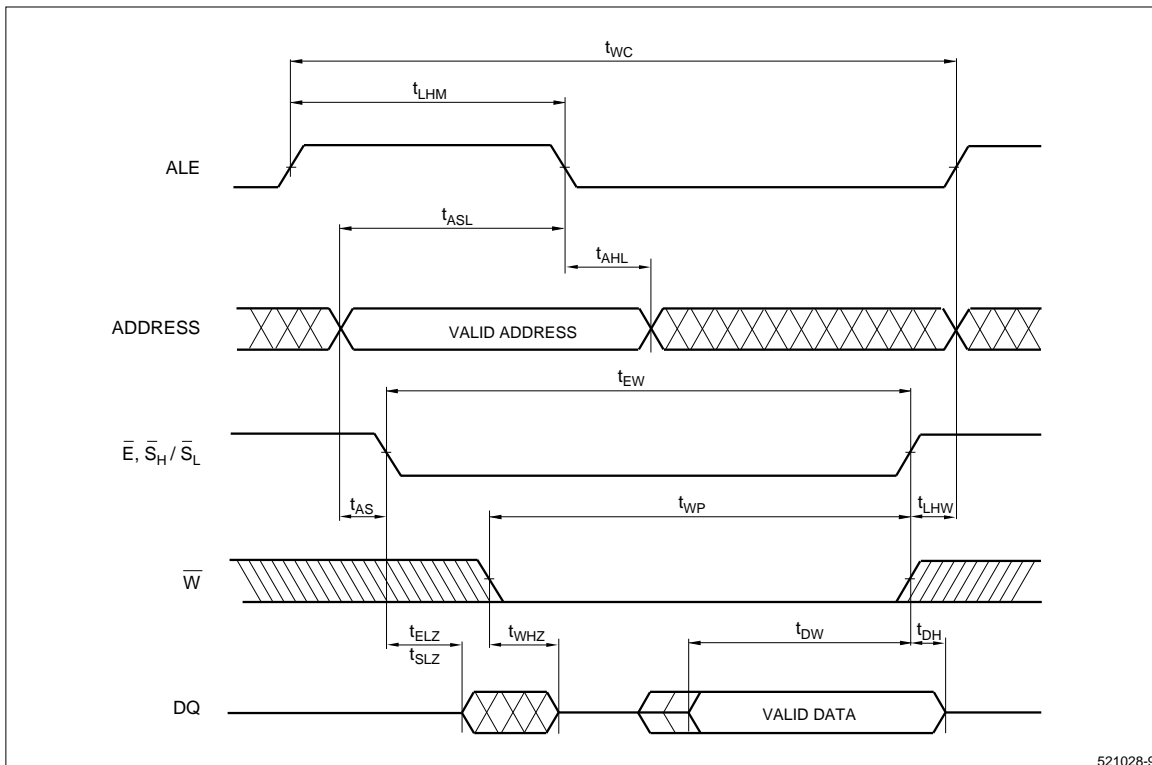
Write Cycle No. 4 (\overline{E} Controlled)

\overline{G} is LOW. DQ lines may transition to Low-Z if the falling edge of \overline{W} occurs after the falling edges of \overline{E} and $\overline{S}_H / \overline{S}_L$.



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Figure 10. Write Cycle No. 3



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Figure 11. Write Cycle No. 4

BYTE OPERATIONS

Byte Read Description (Figure 12)

To read individual bytes, the device must be enabled (\bar{E} is LOW), \bar{W} must be HIGH, the outputs must be enabled (\bar{G} is LOW) and the addresses must be either stable or latched with ALE. Figure 12 is one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(1) At the beginning of the cycle both \bar{S}_L and \bar{S}_H are HIGH.

- (2) \bar{S}_H goes LOW initiating a Read on the upper byte $DQ_{H(9-17)}$. \bar{S}_L remains HIGH keeping the lower byte $DQ_{L(0-8)}$ disabled and in a high-impedance mode.
- (3) \bar{S}_L goes LOW activating $DQ_{L(0-8)}$. Valid data is available in t_{SA} following \bar{S}_L going LOW.
- (4) When \bar{S}_H goes HIGH, $DQ_{H(9-17)}$ remains valid for t_{SHZ} before returning to a high-impedance condition.
- (5) Finally, the Read for the lower byte is terminated by deasserting \bar{S}_L (HIGH). $DQ_{L(0-8)}$ remains active for t_{SHZ} following \bar{S}_L going HIGH.

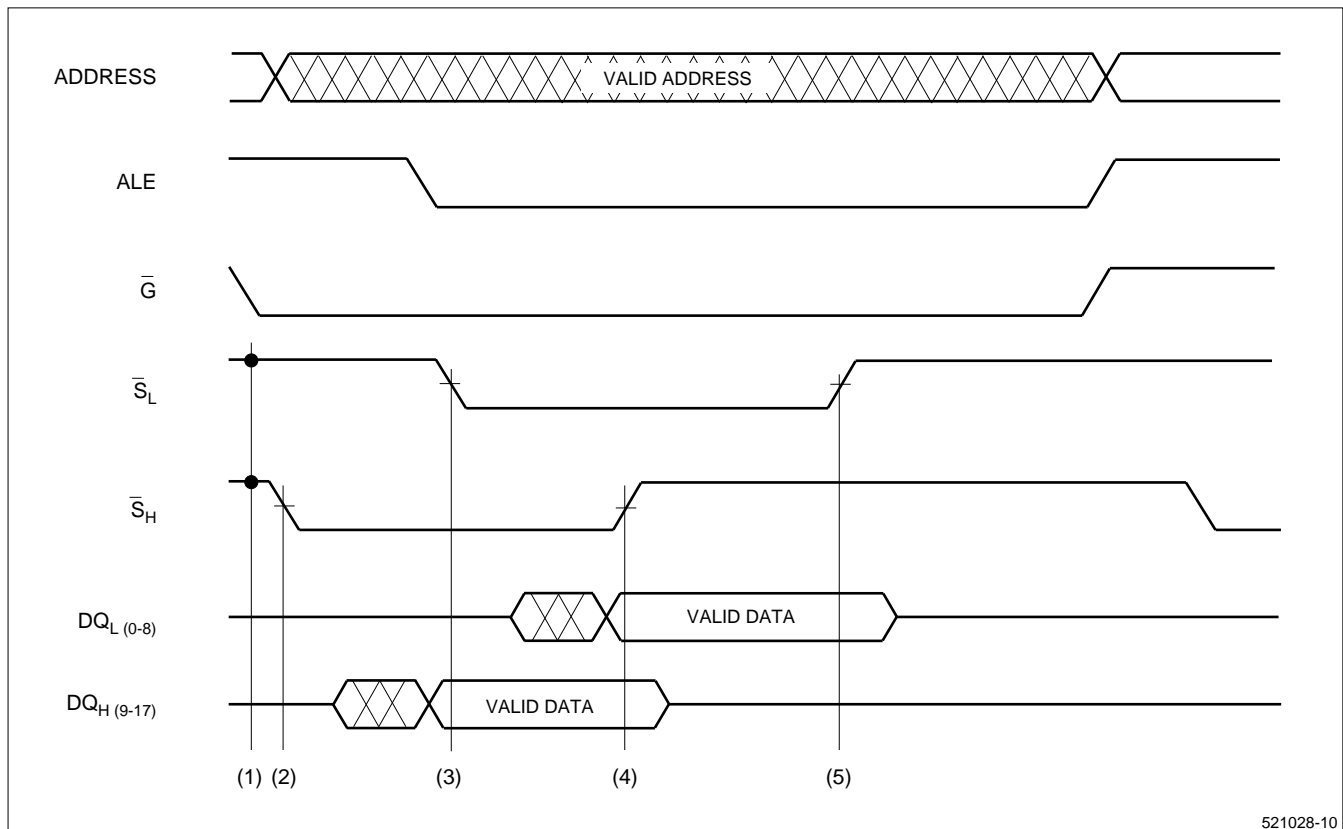


Figure 12. Byte Read (\bar{E} is LOW and \bar{W} is HIGH)

BYTE OPERATIONS (cont'd)

Byte Write Description (Figure 13)

To do individual byte-write operations, the device must be enabled (\bar{E} is LOW, \bar{G} is don't care) and addresses must be either stable or latched. Figure 13 is one example of the byte-write capabilities of this device. The diagram shows two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

- (1) \bar{W} goes LOW while \bar{S}_L and \bar{S}_H remain HIGH.
- (2) \bar{S}_L goes LOW initiating a Write into the lower byte $DQ_{L(0-8)}$ of memory location N. \bar{S}_H remains HIGH preventing a Write into the upper byte $DQ_{L(9-17)}$ of memory location N.
- (3) \bar{S}_L now goes HIGH terminating the Write operation on the lower byte of memory location N.
- (4) Address N is changed to M.
- (5) The Write operation is now initiated on the upper byte $DQ_{H(9-17)}$ by bringing \bar{S}_H LOW. \bar{S}_L remains HIGH preventing a Write operation from occurring in the lower byte $DQ_{L(0-8)}$ of memory location N+ 1.
- (6) \bar{S}_H now goes HIGH terminating the Write operation on the upper byte of address M.
- (7) \bar{W} goes HIGH, ending the Write operation.

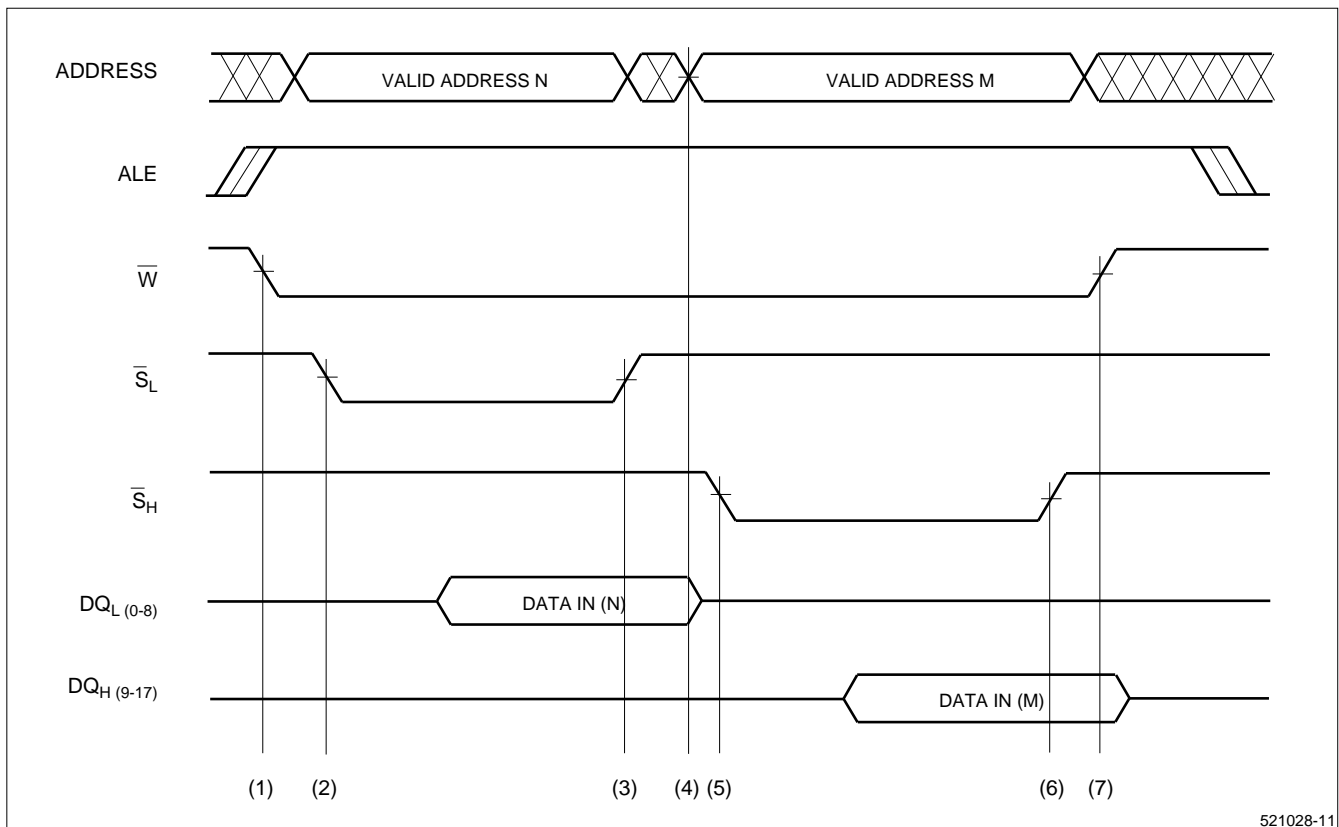
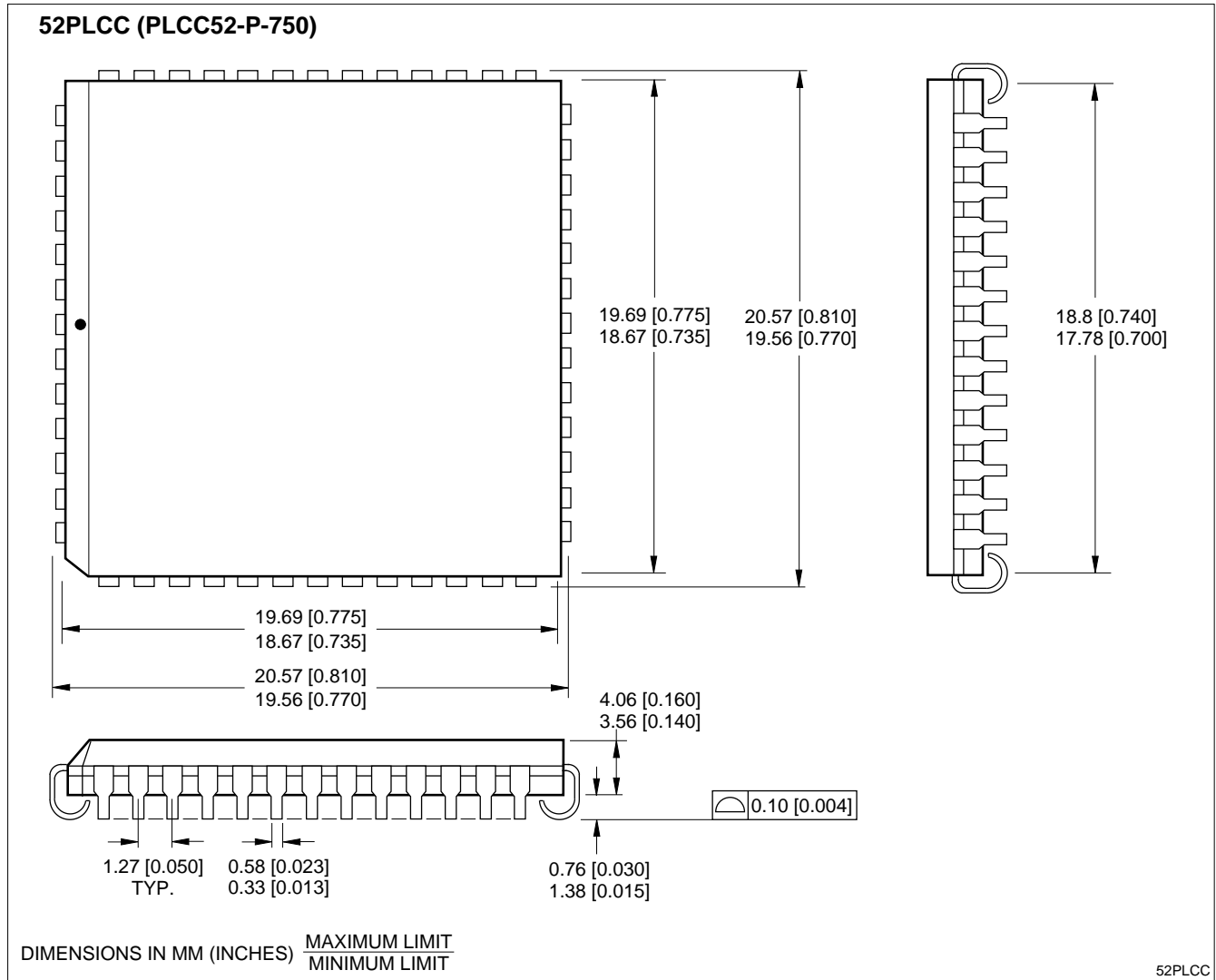


Figure 13. Byte Write (\bar{E} is LOW)

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PACKAGE DIAGRAM



52-pin, 750-mil PLCC

ORDERING INFORMATION

