HMA510/883

16 x 16-Bit CMOS Parallel Multiplier Accumulator

April 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **16 x 16-Bit Parallel Multiplication with Accumulation to a 35-Bit Result**
- **High-Speed (55ns) Multiply Accumulate Time**
- **Low Power CMOS Operation**
  - **I_{CCSB} = 500μA Maximum**
  - **I_{CCOP} = 7.0mA Maximum at 1.0MHz**
- **HMA510/883 is Compatible with the CY7C510 and the IDT7210**
- **Supports Two's Complement or Unsigned Magnitude Operations**
- **Three-State Outputs**

Ordering Information

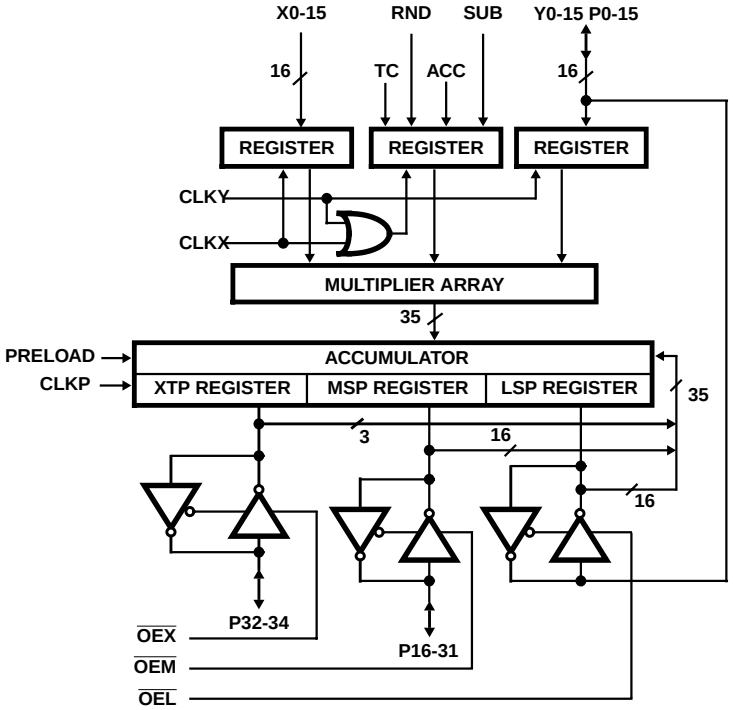
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HMA510GM-55/883	-55 to 125	68 Ld CPGA	G68.B
HMA510GM-65/883	-55 to 125	68 Ld CPGA	G68.B
HMA510GM-75/883	-55 to 125	68 Ld CPGA	G68.B

Description

The HMA510/883 is a high speed, low power CMOS 16 x 16-bit parallel multiplier accumulator capable of operating at 55ns clocked multiply-accumulate cycles. The 16-bit X and Y operands may be specified as either two's complement or unsigned magnitude format. Additional inputs are provided for the accumulator functions which include: loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, and pre-loading the Accumulator Registers from the external inputs.

All inputs and outputs are registered. The registers are all positive edge triggered, and are latched on the rising edge of the associated clock signal. The 35-bit Accumulator Output Register is broken into three parts. The 16-bit least significant product (LSP), the 16-bit most significant product (MSP), and the 3-bit extended product (XTP) Registers. The XTP and MSP Registers have dedicated output ports, while the LSP Register shares the Y-inputs in a multiplexed fashion. The entire 35-bit Accumulator Output Register may be preloaded at any time through the use of the bidirectional output ports and the preloaded control.

Block Diagram



Pinout

68 LEAD CPGA
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X15	RND	ACC	CLKY	TC	PREL	CLKP	P33	
10	X13	X14	$\overline{OEL}$	SUB	CLKX	V_{CC}	$\overline{OEX}$	$\overline{OEM}$	P34	P32	N/C
9	X11	X12								P30	P31
8	X9	X10								P28	P29
7	X7	X8								P26	P27
6	X5	X6				TOP VIEW				P24	P25
5	X3	X4								P22	P23
4	X1	X2								P20	P21
3	Y0/P0	X0								P18	P19
2	N/C	Y1/P1	Y3/P3	Y5/P5	Y7/P7	Y8/P8	Y10/ P10	Y12/ P12	Y14/ P14	P16	P17
1		Y2/P2	Y4/P4	Y6/P6	GND	Y9/P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	

Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}		The +5V power supply pins. 0.1µF capacitors between the V_{CC} and GND pins are recommended.
GND		The device ground.
X0-X15	I	X-Input Data. These 16 data inputs provide the multiplicand which may be in two's complement or unsigned magnitude format.
Y0-Y15/P0-P15	I/O	Y-Input/LSP Output Data. This 16-bit port is used to provide the multiplier which may be in two's complement or unsigned magnitude format. It may also be used for output of the least significant product (P0-P15) or for preloading the LSP Register.
P16-P3	I/O	MSP Output Data. This 16-bit port is used to provide the most significant product output (P16-P31). It may also be used to preload the MSP Register.
P32-P34	I/O	XTP Output Data. This 3-bit port is used to provide the extended product output (P32-P34). It may also be used to preload the XTP Register.
TC	I	Two's Complement Control. Input data is interpreted as two's complement when this control is HIGH. A LOW indicates the data is to be interpreted as unsigned magnitude format. This control is latched on the rising edge of CLKX or CLKY.
ACC	I	Accumulate Control. When this control is HIGH, the Accumulator Output Register contents are added to or subtracted from the current product, and the result is stored back into the Accumulator Output Register. When LOW, the product is loaded into the Accumulator Output Register overwriting the current contents. This control is also latched on the rising edge of CLKX or CLKY.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
SUB	I	Subtract Control. When both SUB and ACC are HIGH, the Accumulator Register contents are subtracted from the current product. When ACC is HIGH and SUB is LOW, the Accumulator Register contents and the current product are summed. The SUB control input is latched on the rising edge of CLKX or CLKY.
RND	I	Round Control. When this control is HIGH, a one is added to the most significant bit of the LSP. When LOW, the product is unchanged.
PREL	I	Preload Control. When this control is HIGH, the three bidirectional ports may be used to preload the Accumulator Registers. The three-state controls ($\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$) must be HIGH, and the data will be preloaded on the rising edge of CLKP. When this control is LOW, the Accumulator Registers function in a normal manner.
$\overline{OEL}$	I	Y-Input/LSP Output Port Three-State Control. When $\overline{OEL}$ is HIGH, the output drivers are in the high impedance state. This state is required for Y-data input or preloading the LSP Register. When $\overline{OEL}$ is LOW, the port is enabled for LSP output.
$\overline{OEM}$	I	MSP Output Port Three-State Control. A LOW on this control line enables the port for output. When $\overline{OEM}$ is HIGH, the output drivers are in the high impedance state. This control must be HIGH for preloading the MSP Register.
$\overline{OEX}$	I	XTP Output Port Three-State Control. A LOW on this control line enables the port for output. When $\overline{OEX}$ is HIGH, the output drivers are in the high impedance state. This control must be HIGH for preloading the XTP Register.
CLKX	I	X-Register Clock. The rising edge of this clock latches the X-Data Input Register along with the TC, ACC, SUB and RND inputs.
CLKY	I	Y-Register Clock. The rising edge of this clock latches the Y-Data Input Register along with the TC, ACC, SUB and RND inputs.
CLKP	I	Product Register Clock. The rising edge of CLKP latches the LSP, MSP and XTP Registers. If the preload control is active, the data on the I/O ports is loaded into these registers. If preload is not active, the accumulated product is loaded into the registers.

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input or Output Voltage Applied . . . . . G ND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +4.5V to +5.5V
Temperature Range . . . . . 55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CPGA Package	43	10

Maximum Package Power Dissipation at 125^oC
CPGA Package 1.17W
Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range . . . . . 65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Gate Count . . . . . 4800 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. HMA5IO/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +4.0mA V_{CC} = 4.5V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open	1, 2, 3	$-55 \le T_A \le 125$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 1.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Note 3)	1, 2, 3	$-55 \le T_A \le 125$	-	7.0	mA
Functional Test	FT	(Note 4)	7, 8	$-55 \le T_A \le 125$	-	-	

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating Supply Current a proportional to frequency, typical rating is 5mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} (clock inputs) = 3.2V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \ge 1.5V$, and $V_{OL} \le 1.5V$.

TABLE 2. HMA510/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 5) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (^oC)	-55		-65		-75		UNITS
					MIN	MAX	MIN	MAX	MIN	MAX	
Multiply Accumulate Time	t_{MA}		9, 10, 11	$-55 \le T_A \le 125$	-	55	-	65	-	75	ns
Input Setup Time	t_S		9, 10, 11	$-55 \le T_A \le 125$	20	-	25	-	25	-	ns

TABLE 2. HMA510/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 5) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (^{O}C)	-55		-65		-75		UNITS
					MIN	MAX	MIN	MAX	MIN	MAX	
Clock HIGH Pulse Width	t_{PWH}		9, 10, 11	$-55 \le T_A \le 125$	20	-	25	-	25	-	ns
Clock LOW Pulse Width	t_{PWL}		9, 10, 11	$-55 \le T_A \le 125$	20	-	25	-	25	-	ns
Output Delay	t_D		9, 10, 11	$-55 \le T_A \le 125$	-	30	-	35	-	35	ns
Three-State Enable Time	t_{ENA}	(Note 5)	9, 10, 11	$-55 \le T_A \le 125$	-	30	-	30	-	35	ns

NOTES:

5. AC Testing as follows: V_{CC} = 4.5V and 5.5V. Input levels 0V and 3.0V (0V and 3.2V tor clock inputs). Timing reference levels = 1.5V, Output load per test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.
6. Transition is measured at 1200mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.

TABLE 3. HMA510/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	NOTE	TEMPERATURE (^{O}C)	-55		-65		-75		UNITS
					MIN	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All measurements are referenced to device GND	1	T_A = 25	-	10	-	10	-	10	pF
Output Capacitance	C_{OUT}		1	T_A = 25	-	10	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$		1	T_A = 25	-	15	-	15	-	15	pF
Input Hold Time	t_H		1	$-55 \le T_A \le 125$	3	-	3	-	3	-	ns
Three-State Disable Time	t_{DIS}		1	$-55 \le T_A \le 125$	-	30	-	30	-	30	ns
Output Rise Time	t_r	From 0.8V to 2.0V	1	$-55 \le T_A \le 125$	-	10	-	10	-	10	ns
Output Fall Time	t_f	From 2.0V to 0.8V	1	$-55 \le T_A \le 125$	-	10	-	10	-	10	ns

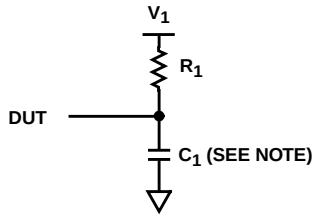
NOTE:

7. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

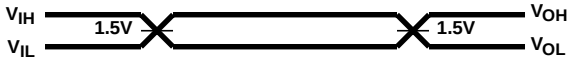
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10,11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

AC Test Circuit



NOTE: Includes Stray and Jig Capacitance

AC Testing Input, Output Waveforms



NOTE: AC Testing: All Parameters tested as per test circuit. Input rise and fall times are driven at 1ns/V.

Timing Diagram

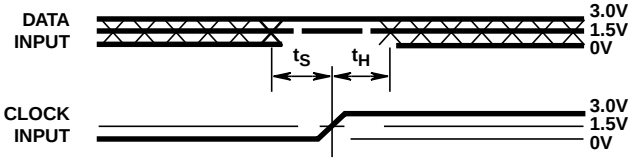


FIGURE 1. SET-UP AND HOLD TIME

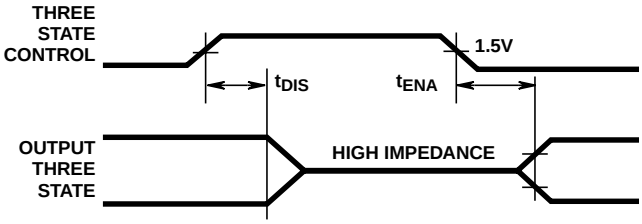


FIGURE 2. THREE-STATE CONTROL

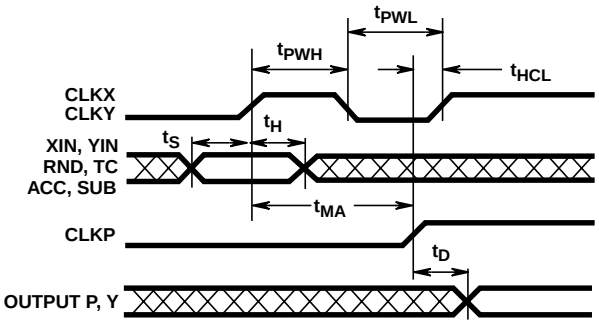


FIGURE 3. HMA510 TIMING DIAGRAM

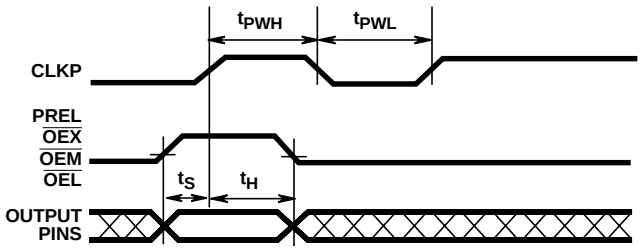


FIGURE 4. PRELOAD TIMING DIAGRAM

Burn-In Circuit

68 LEAD CPGA
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X15	RND	ACC	CLKY	TC	PREL	CLKP	P33	
10	X13	X14	$\overline{OEL}$	SUB	CLKX	V_{CC}	$\overline{OEX}$	$\overline{OEM}$	P34	P32	N/C
9	X11	X12								P30	P31
8	X9	X10								P28	P29
7	X7	X8								P26	P27
6	X5	X6								P24	P25
5	X3	X4								P22	P23
4	X1	X2								P20	P21
3	Y0/P0	X0								P18	P19
2	N/C	Y1/P1	Y3/P3	Y5/P5	Y7/P7	Y8/P8	Y10/P10	Y12/P12	Y14/P14	P16	P17
1		Y2/P2	Y4/P4	Y6/P6	GND	Y9/P9	Y11/P11	Y13/P13	Y15/P15	N/C	

CPGA PIN	PIN NAME	BURN-IN SIGNAL
B6	X6	F1
A6	X5	F2
B5	X4	F3
A5	X3	F4
B4	X2	F5
A4	X1	F6
B3	X0	F7
A3	Y0/P0	F8
B2	Y1/P1	F9
B1	Y2/P2	F10
C2	Y3/P3	F11
C1	Y4/P4	F12
D2	Y5/P5	F13
D1	Y6/P6	F14
E2	Y7/P7	F15
E1	GND	GND
F2	Y8/P8	F1
F1	Y9/P9	F2
G2	Y10/P10	F3

CPGA PIN	PIN NAME	BURN-IN SIGNAL
G1	Y11/P11	F5
H2	Y12/P12	F4
H1	Y13/P13	F4
J2	Y14/P14	F8
J1	Y15/P15	F9
K2	P16	$V_{CC}/2$
L2	P17	$V_{CC}/2$
K3	P18	$V_{CC}/2$
L3	P19	$V_{CC}/2$
K4	P20	$V_{CC}/2$
L4	P21	$V_{CC}/2$
K5	P22	$V_{CC}/2$
L5	P23	$V_{CC}/2$
K6	P24	$V_{CC}/2$
L6	P25	$V_{CC}/2$
K7	P26	$V_{CC}/2$
L7	P27	$V_{CC}/2$
K8	P28	$V_{CC}/2$
L8	P29	$V_{CC}/2$

CPGA PIN	PIN NAME	BURN-IN SIGNAL
K9	P30	$V_{CC}/2$
L9	P31	$V_{CC}/2$
K10	P32	$V_{CC}/2$
K11	P33	$V_{CC}/2$
J10	P34	$V_{CC}/2$
J11	CLKP	F0
H10	$\overline{OEM}$	GND
H11	PREL	F6
G10	$\overline{OEX}$	GND
G11	TC	F5
F10	V_{CC}	V_{CC}
F11	CLKY	F0
E10	CLKY	F0
E11	ACC	F1
D10	SUB	F2
D11	RND	F3
C10	$\overline{OEL}$	V_{CC}
C11	X15	F8
B10	X14	F9
A10	X13	F10
B9	X12	F11
A9	X11	F12
B8	X10	F13
A8	X9	F14
B7	X8	F15
A7	X7	F7
A2	N.C.	N.C.
K1	N.C.	N.C.
L10	N.C.	N.C.
B11	N.C.	N.C.

NOTES:

8. V_{CC} = 5.5V +0.5V/-0.0V with 0.1µF decoupling capacitor to GND.
9. F0 = 100kHz, F1 = F0/2, F2 = F1/2, ... 10%
10. $V_{IH} = V_{CC}$ - 1V ±0.5V (Min), V_{IL} = 0.8V (Max).
11. 47kΩ load resistors used on all pins except V_{CC} and GND (Pin-Grid identifiers F10, G10, G11 and H11).

Die Characteristics

DIE DIMENSIONS:
184 x 176 x 19 ± 1mils

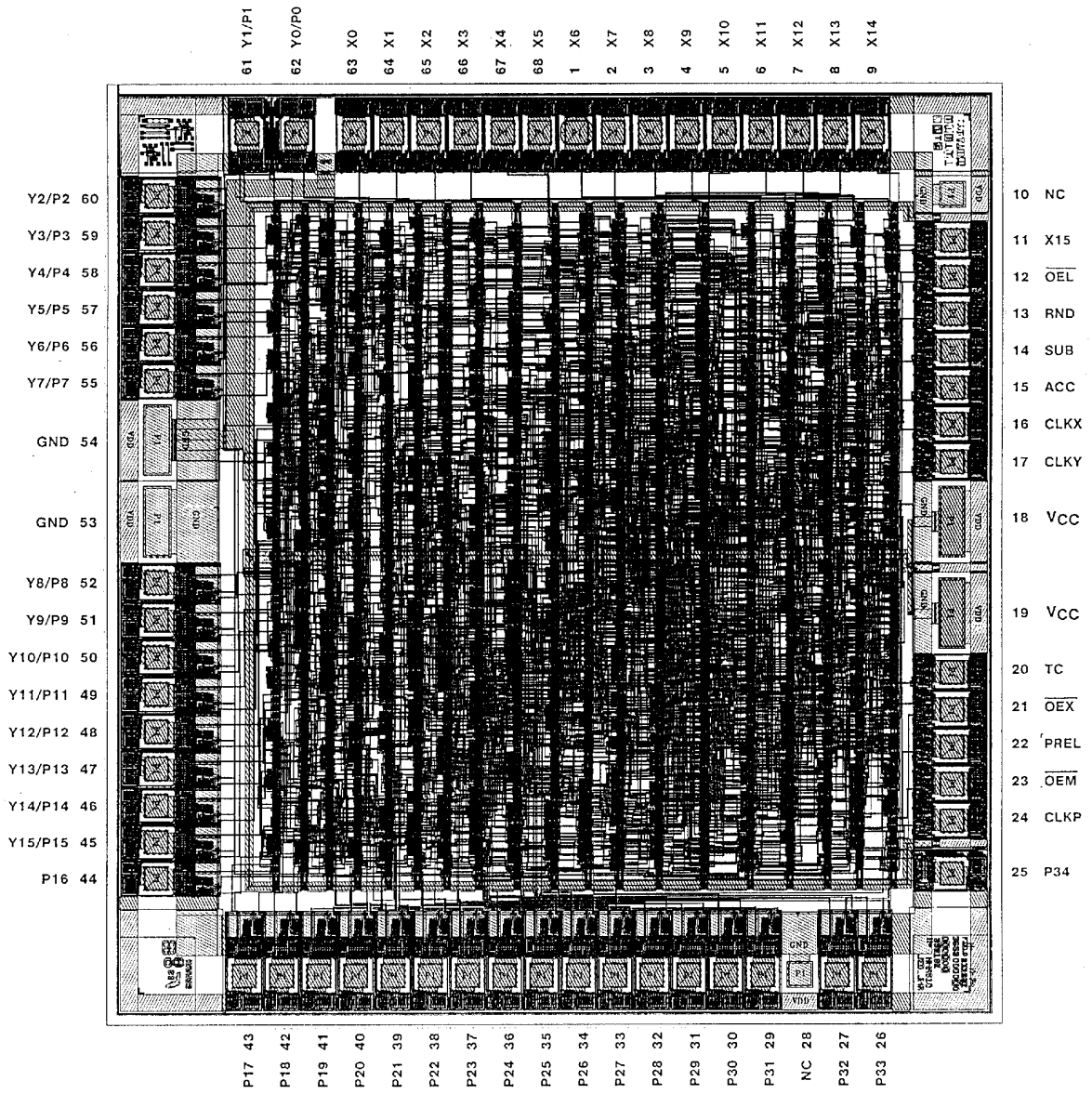
METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $0.9 \times 10^5 A/cm^2$

Metallization Mask Layout

HMA510/883



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