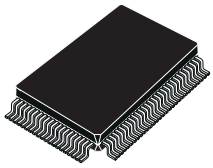
SERCON816

SERCOS INTERFACE CONTROLLER

- Single-chip controller for SERCOS interface
- Real time communication for industrial control systems
- 8/16-bit bus interface, Intel and Motorola control signals
- Dual port RAM with 2048 word *16-bit
- Data communications via optical fiber rings, RS 485 rings and RS 485 busses
- Maximum transmission rate of 16 Mbaud with internal clock recovery
- Internal repeater for ring connections
- Full duplex operation
- Modulation of power of optical transmitter diode
- Automatic transmission of synchronous and data telegrams in the communication cycle
- Flexible RAM configuration, communication data stored in RAM (single or double buffer) or transfer via DMA
- Synchronization by external signal



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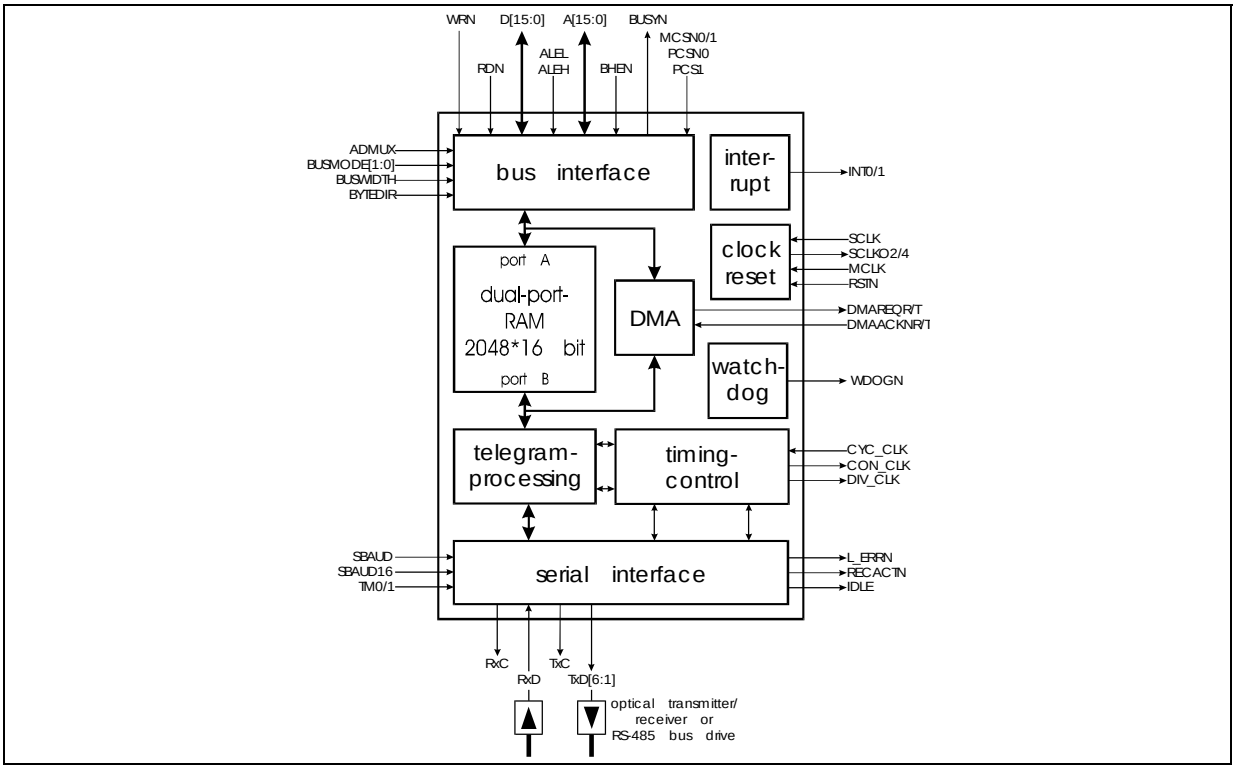
ORDERING NUMBERS: SERC816
SERC816/TR

- Timing control signals
- Automatic service channel transmission
- Watchdog to monitor software and external synchronization signals
- Compatible mode to SERCON410B SERCOS interface controller
- 100-pin plastic flat-pack casing

Figure 1. SERCON816 Block Diagram



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1 GENERAL DESCRIPTION

The SERCOS interface controller SERCON816 is an integrated circuit for SERCOS interface communication systems. The SERCOS interface is a digital interface for communication between systems which have to exchange information cyclically at short, fixed intervals (62,5 s to 65 ms). It is appropriate for the synchronous operation of distributed control or test equipment (e.g. connection between drives and numeric control).

A SERCOS interface communication system consists of one master and several slaves. These units are connected by a fiber optical ring. This ring starts and ends at the master. The slaves regenerate and repeat their received data or send their own telegrams. By this method the telegrams sent by the master are received by all slaves while the master receives data telegrams from the slaves. The optical fiber assures a reliable high-speed data transmission with excellent noise immunity.

The SERCOS interface controller contains all the hardware-related functions of the SERCOS interface and considerably reduces the hardware costs and the computing time requirements of the microprocessor. It is the direct link between the electro-optical receiver and transmitter and the microprocessor that executes the control algorithms. The SERCON816 can be used both for SERCOS interface masters and slaves.

The circuit contains the following functions (Fig. 1):

– Interface to the microprocessor with a data bus width of 8 or 16 bits and with control lines according to Intel or Motorola standards.
– A serial interface for making a direct connection with the optical receiver and transmitter of the fiber optic ring or with drivers to an electric ring or bus. Data and clock regeneration, the repeater for ring topologies and the serial transmitter and receiver are integrated. The signals are monitored and test signals generated. The serial interface operates up to 16 Mbaud without external circuitry.
– A dual port RAM (2048 * 16 bit) for control and communication data. The organization of the memory is flexible.
– Telegram processing for automatic transmission and monitoring of synchronous and data telegrams. Only transmission data which is intended for the particular interface user is processed. The transmitted data is either stored in the internal RAM (single or double buffer) or transferred via direct memory access (DMA). The transmission of service channel information over several communication cycles is executed automatically.

In addition to the SERCOS interface the SERCON816 can also be used for other real-time communications tasks. As an alternative to the fiber optical ring also bus topologies with RS-485 signals are supported (Fig. 4). The SERCON816 is therefore suitable for a wide range of applications.
Remark: The SERCON816 is based on the former SERCON410B SERCOS interface controller.

Figure 2. SERCON816 Pin Configuration

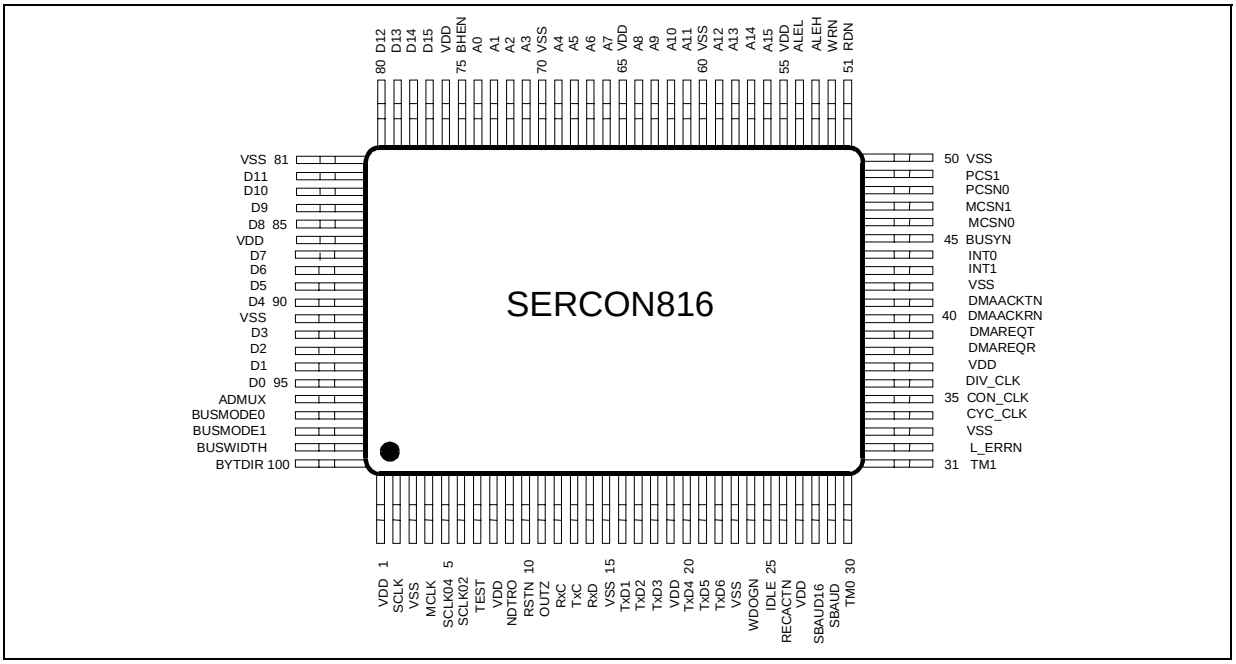


Figure 3. SERCON816 with Ring Connection (SERCOS interface)

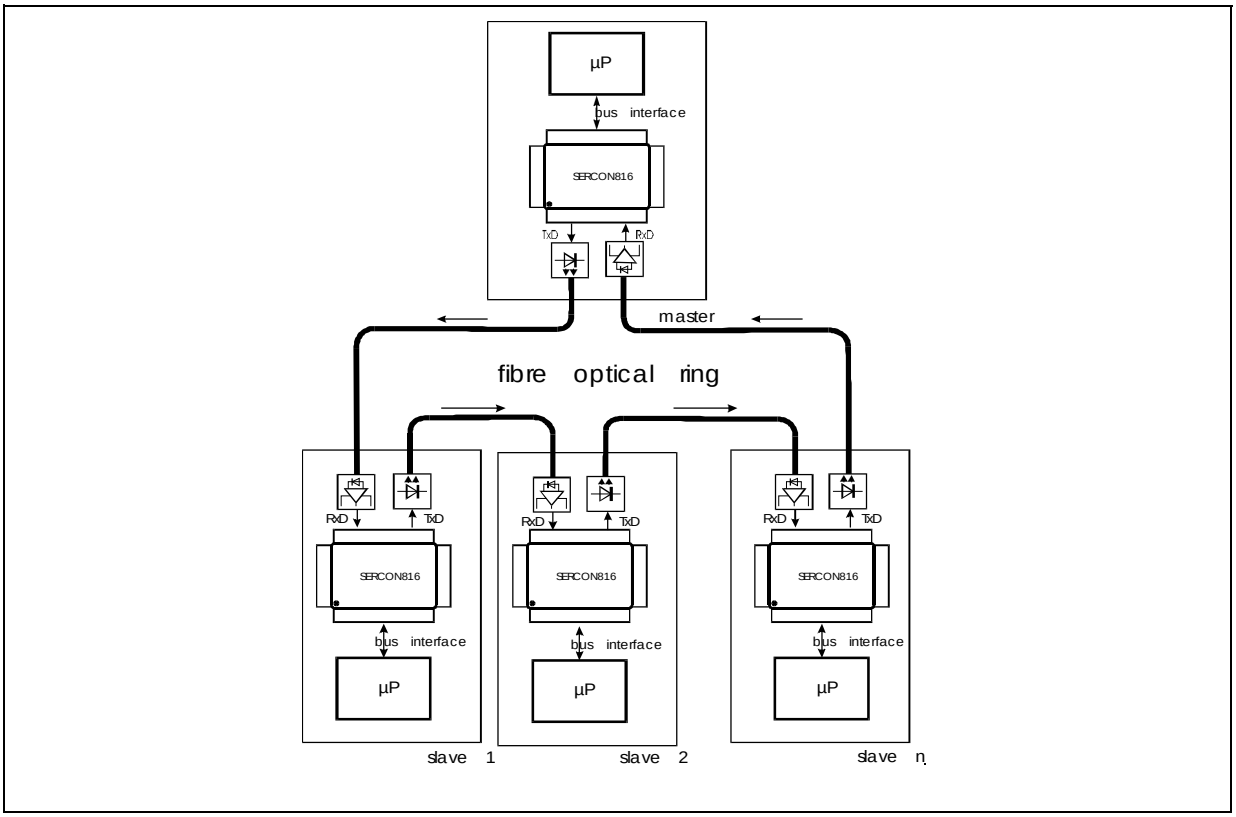
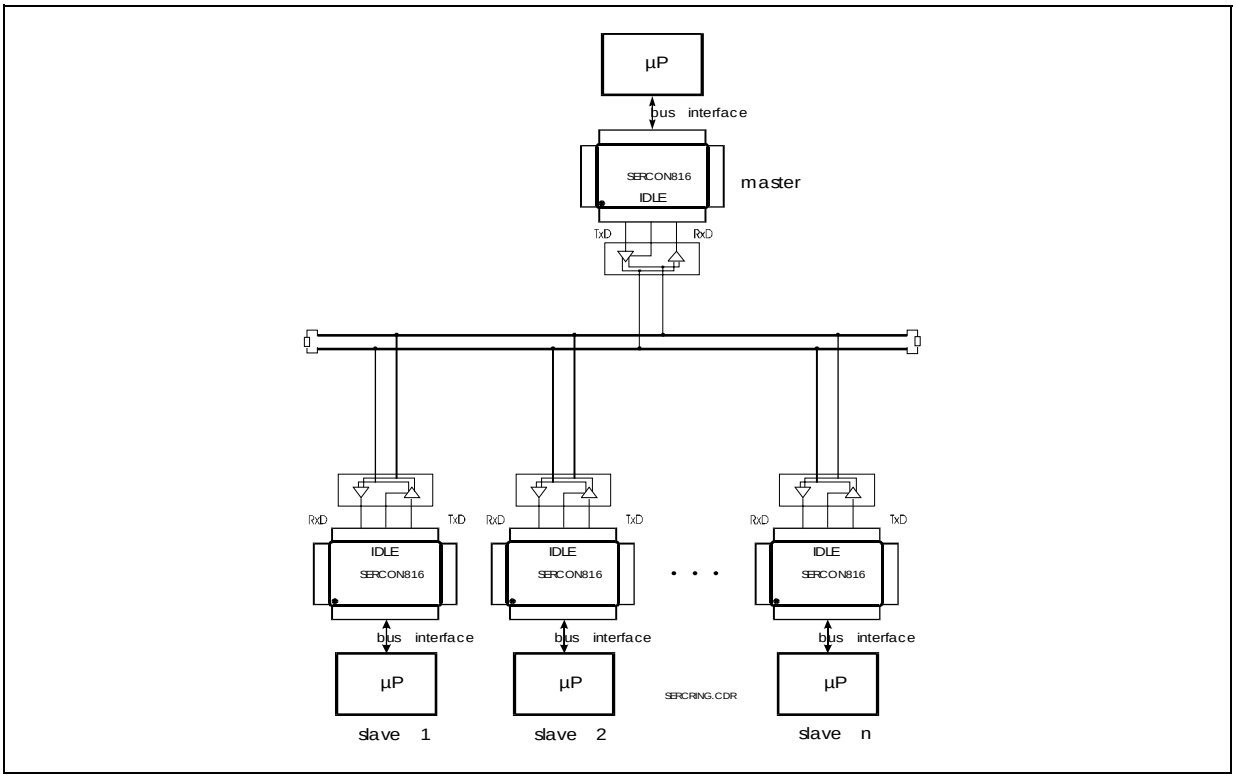


Figure 4. SERCON816 with RS-485 bus connection



2 PIN DESCRIPTION

Table 1. SERCON816 I/O Port Function Summary

Signal(s)	Pin(s)	IO	Function
D15-0	77-80, 82-85, 87-90, 92-95	I/O	Data bus: for 8-bit-wide bus interfaces, data is written to and read via D7-0, for 16-bit-wide bus interfaces via D15-0. When ADMUX is 1, the address which is stored in the address latch with ALEL and ALEH is input via D15-0.
ALEL, ALEH	54, 53	I	Address latch enable, low and high, active high: they are only used when ADMUX is 1. When ALEL/ALEH is 1, the signals go from the data bus to the address bus, when ALEL/ALEH = 0, they store the address. When ADMUX is 0, ALEL/ALEH have to be connected to VDD.
RDN	51	I	Read: for the Intel bus interface, data is read when RDN is 0. For the Motorola bus interface, data is read or written to when RDN is 0 (BUSMODE1 = 0) or RDN is 1 (BUSMODE1 = 1).
WRN	52	I	Write: for the Intel bus interface, data is written to when WRN is 0. For the Motorola bus interace, WRN selects read (WRN = 1) and write (WRN = 0) operations of the data bus.
BHEN	75	I	Byte high enable, active low: in the 16-bit bus mode, data is transferred via D15-8 when BHEN is 0.
MCSN0, MCSN1	46,47	I	Memory chip select, active low: to access the internal RAM MCSN0 and MCSN1 must be 0.
PCSN0, PCS1	48,49	I	Periphery chip select, active low (PCSN0) and active high (PCS1): to access the control registers PCSN0 must equal 0 and PCS1 must equal 1.
BUSYN	45	O	RAM busy, active low: becomes active if an access to an address of the dual port RAM is performed simultaneously to an access to the same memory location by the internal telegram processing.
DMAREQR	38	O	DMA request receive, active high: becomes active if data from the receive FIFO can be read. At the beginning of the read operation of the last word of the receive FIFO, DMAREQR becomes inactive.
DMAACKRN	40	I	DMA acknowledge receive, active low: when DMAACKRN is 0, the receive FIFO is read, independent of the levels on A6-1 and the chip select signals.
DMAREQT	39	O	DMA request transmit, active high: becomes active when data can be written to the transmit FIFO. DMAREQT becomes inactive again at the beginning of the last write access to the transmit FIFO.
DMAACKTN	41	I	DMA acknowledge transmit, active low: when DMAACKTN is 0, the transmit FIFO is written to when there is a bus write access independent of the levels on A6-1 and the chip select signals.
ADMUX	96	I	Address data bus: when ADMUX is 0 A15-0 are the address inputs, when ADMUX is 1 A15-0 are the outputs of the address latch.
BUSMODE0, BUSMODE1	97,98	I	Bus mode: BUSMODE0 = 0 turns on the Intel bus interface (RDN = read, WRN = write), BUSMODE0 = 1 selects the Motorola interface (RDN = data strobe, WRN = read/write). BUSMODE1 selects the 0-active data strobe (BUSMODE1 = 0) or the 1-active data strobe (BUSMODE1 = 1).
BUSWIDTH	99	I	Bus width: selects the 8-bit- (0) or the 16-bit-wide interface (1).
BYTEDIR	100	I	Byte address sequence: when BYTEDIR is 0, A0 = 0 addresses the lower 8 bits of a word (low byte first), when BYTEDIR is 1, the upper 8 bits of a word are addressed (high byte first).
INT0, INT1	44,43	O	Interrupts, active low or active high. Interrupt sources and signal polarity are programmable.
SBAUD16	28	I	Baud rate and SERCON410B compatible mode: SBAUD and SBAUD16 selects the baud rate for the serial interface. If SBAUD16 is '1' the SERCON410B compatible mode is selected.
SBAUD	29	I	Baud rate. Can be overwritten by the microprocessor.

Table 1. SERCON816 I/O Port Function Summary (continued)

Signal(s)	Pin(s)	IO	Function
RxD	14	I	Receive data for the serial interface.
RxC	12	O	Receive clock for the serial interface. Output of the internally generated receive clock.
RECACTN	26	O	Receive active, active low. Indicates that the serial receiver is receiving a telegram.
TxD1	16	O	Transmit data. The pin can be switched to a high impedance state.
TxD6-2	22,21,20, 18,17	O	Transmit data or output port. The pins either output the serial data or can be used as parallel output ports. When they output transmit data, each pin can be switched to a high impedance state individually.
TxC	13	O	Transmit clock for the serial interface. Output for the internally generated transmit clock.
IDLE	25	O	Transmitter active, active low. When transmitting own data IDLE is 0.
DMAREQT	39	O	DMA request transmit, active high: becomes active when data can be written to the transmit FIFO. DMAREQT becomes inactive again at the beginning of the last write access to the transmit FIFO.
DMAACKTN	41	I	DMA acknowledge transmit, active low: when DMAACKTN is 0, the transmit FIFO is written to when there is a bus write access independent of the levels on A6-1 and the chip select signals.
ADMUX	96	I	Address data bus: when ADMUX is 0 A15-0 are the address inputs, when ADMUX is 1 A15-0 are the outputs of the address latch.
BUSMODE0, BUSMODE1	97,98	I	Bus mode: BUSMODE0 = 0 turns on the Intel bus interface (RDN = read, WRN = write), BUSMODE0 = 1 selects the Motorola interface (RDN = data strobe, WRN = read/write). BUSMODE1 selects the 0-active data strobe (BUSMODE1 = 0) or the 1-active data strobe (BUSMODE1 = 1).
BUSWIDTH	99	I	Bus width: selects the 8-bit- (0) or the 16-bit-wide interface (1).
BYTEDIR	100	I	Byte address sequence: when BYTEDIR is 0, A0 = 0 addresses the lower 8 bits of a word (low byte first), when BYTEDIR is 1, the upper 8 bits of a word are addressed (high byte first).
INT0, INT1	44,43	O	Interrupts, active low or active high. Interrupt sources and signal polarity are programmable.
SBAUD16	28	I	Baud rate and SERCON410B compatible mode: SBAUD and SBAUD16 selects the baud rate for the serial interface. If SBAUD16 is ‘1’ the SERCON410B compatible mode is selected.
SBAUD	29	I	Baud rate. Can be overwritten by the microprocessor.
RxD	14	I	Receive data for the serial interface.
RxC	12	O	Receive clock for the serial interface. Output of the internally generated receive clock.
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TxD1	16	O	Transmit data. The pin can be switched to a high impedance state.
TxD6-2	22,21,20, 18,17	O	Transmit data or output port. The pins either output the serial data or can be used as parallel output ports. When they output transmit data, each pin can be switched to a high impedance state individually.
TxC	13	O	Transmit clock for the serial interface. Output for the internally generated transmit clock.
IDLE	25	O	Transmitter active, active low. When transmitting own data IDLE is 0.
TM0, TM1	30,31	I	Turn on test generator: TM0 = 0 switches TxD1-6 to contiuous signal light, TM1 = 0 switch-over to zero bit stream. The processor can overwrite the level of TM1-0. Select repeater mode at reset time: TM1=0 and TM2=0 repeater off, all other repeater on.

Table 1. SERCON816 I/O Port Function Summary (continued)

Signal(s)	Pin(s)	IO	Function
WDOGN	24	O	Watchdog output (active low)
L_ERRN	32	O	Line error, active low: goes low when signal distortion is too high or when the receive signal is missing. The operating mode is programmed by the processor.
CYC_CLK	34	I	SERCOS interface cycle clock: CYC_CLK synchronizes the communication cycles. The polarity is programmable.
CON_CLK	35	O	Control clock: becomes active within a communication cycle. Time, polarity and width are programmable.
DIV_CLK	36	O	Divided control clock: becomes active several times within a communication cycle or once in several communication cycles. Number of pulses, start time, repetition rate and polarity are programmable, the pulse width is 1 µs.
SCLK	2	I	Serial clock for clock regeneration: the maximum frequency is 64 MHz.
SCLKO2	6	O	Clock output: outputs the SCLK clock divided by 2 or 1.
SCLKO4	5	O	Clock output: outputs the SCLK clock divided by 4 or 2.
MCLK	4	I	Master clock for telegram processing and timing control, frequency 12 to 64 MHz.
RSTN	10	I	Reset, active low. Must be zero for at least 50 ns after power on.
TEST	7	I	Test, active high. Has to be tied to VSS.
OUTZ	11	I	Puts outputs into high impedance state, active high: OUTZ is 1 puts all pins into a high impedance state. The clocks are turned off and the circuit is reset. For the in-circuit test and for turning on the power-down mode.
NDTRO	9	O	NAND tree output. For the test at the semiconductor manufacturers and for the connection test after board production. NDTRO is not set to a high impedance state.
VSS	3,15,23,33 ,42,50,60, 70,81,91		Ground pins:
VDD	1,8,19,27, 37,55,65, 76,86		Power supply +5 V ± 5%.

3 ELECTRICAL (DC AND AC) CHARACTERISTICS

3.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to 6.5	V
V_I	Input voltage	-0.5 to V_{DD} + 0.5	V
V_O	Output voltage	-0.5 to V_{DD} + 0.5	V
T_{STG}	Storage temperature	-55 to +150	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating temperature	-40	85	°C
T_J	Chip junction temperature	-40	125	°C
V_{DD}	Operating supply voltage	4.75	5.25	V
f_{SCLK}	Clock frequency SCLK	32[1]	64	MHz
f_{MCLK}	Clock frequency MCLK	12[2]	64	MHz

Notes: 1. Only if PLL is used (SBAUD16=0)
2. For normal operation, during testing f_{MCLK} = 0 is possible

3.3 ELECTRICAL CHARACTERISTCS

(V_{DD} = 5V ± 5% T_{amb} = -40 °C to +85 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage (TTL) All inputs				0.8	V
V_{IH}	High level input voltage (TTL) All inputs		2.0			V
V_{hyst}	Schmitt trigger hysteresis L_ERRN, TXD6-1, MCLK, SCLK, RSTN, ADMUX, BUSMODE1-0, BUSWIDTH, BYTEDIR, TM1-0, SBAUD16, SBAUD, TEST, OUTZ, RXD, CYC_CLK		0.4		0.7	V
I_{IL}	Low level input current with pull-up D15-0, A15-0, TXD6-1, ADMUX, BUSMODE1-0, BYTEDIR, TM1-0, SBAUD16, SBAUD, TEST, OUTZ, RXD, CYC_CLK, BHEN, MCSN1-0, PCSN0, PCS1, DMAACKTN, DMAACKRN	$V_I = V_{SS}$	-40	-100	-240	µA
I_{IH}	High level input current with pull-down MCLK, SCLK, RSTN, ALEH, ALEL	$V_I = V_{DD}$	40	100	240	µA
Rup	Equivalent pull-up resistance	$V_I = V_{SS}$	23	50	112.5	KOhm
Rdn	Equivalent pull-down resistance	$V_I = V_{DD}$	23	50	112.5	KOhm
V_{OL}	Low level output voltage, all O- and I/O-pins except TXD6-1, L_ERRN	I_{OI} = -4 mA			0.4	V
V_{OH}	High level output voltage, all O- and I/O-pins except TXD6-1, L_ERRN	I_{OH} = +4 mA	2.4			V

3.3 ELECTRICAL CHARACTERISTCS (continued)

(V_{DD} = 5V ± 5% T_{amb} = -40 °C to +85 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage, pins TXD6-1, L_ERRN	I_{OI} = -8 mA			0.4	V
V_{OH}	High level output voltage, pins TXD6-1, L_ERRN	I_{OH} = +8 mA	2.4			
I_{OZ}	Tri-state output leakage	V_O = 0 V or V_{DD}			1	µA
I_{KLU}	I/O latch-up current	$V<V_{SS}$ $V>V_{DD}$	200			mA
V_{ESD}	Electrostatic protection	Leakage < 1 µA, human body model	2000			V
C_{PIN}	Pin capacitance			10		pF

3.4 Power Dissipation

(V_{DD} = 5V ± 5% T_{amb} = -40 °C to +85 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_D	Power dissipation	16 Mbaud, MCLK=64 MHz		850[1]		mW
P_{DA}	Maximum allowed power dissipation	T_A=+85°, no air flow			1000	mW

Notes: 1. estimated

3.4.1 Power Dissipation Considerations

Most of the current consumed by CMOS devices is alternate current (AC) which is charging and discharging the capacitances of the pins and internal nodes. The current consumption rises with the frequency at which the pins and internal nodes will toggle and with the capacitances connected to the pins of the device:

$$P = f \cdot C \cdot V^2 \quad \text{(C=capacitance, V=voltage, f=frequency)}$$

For applications which require low power consumption or exceeds the maximum allowed power consumption the following is required:

- Connect unused pins to pull-up or pull-down resistors
- Minimize the capacitive load on the pins
- Reduce clock frequency of SCLK and MCLK
- Minimize accesses to the internal RAM and control registers

The maximum allowed power consumption is limited by the maximum allowed chip junction temperature and by the number of VCC/VDD pins. The chip junction temperature is influenced by the ambient temperature and the package thermal resistance. The ambient temperature could be influenced by the application through a good temperature management like heat sinks or ambient air cooling.

Typical current consumption: measured at 5V (VCC/VDD) and 25°C

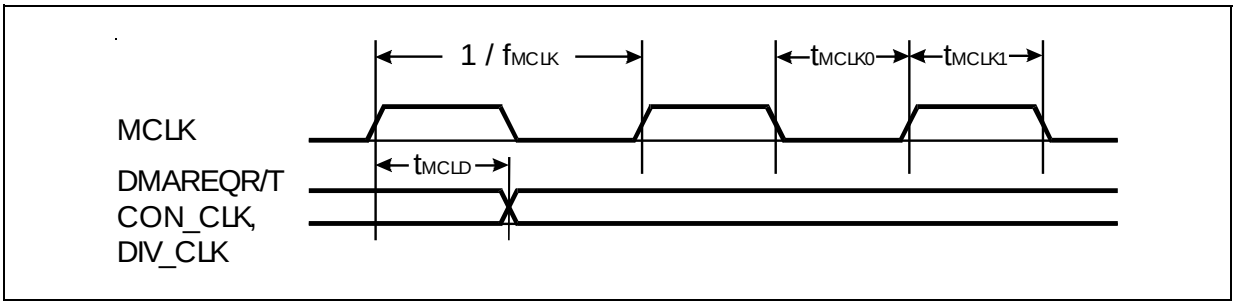
Mode	f_{SCLK} (MHz)	f_{MCLK} (MHz)	Current (mA)
410B	64	32	30
816	64	32	80

3.5 AC Electrical Characteristics

(C_{load} = 50 pF, V_{DD} = 5 V ± 5% T_{amb} = -40 °C to +85 °C)

3.5.1 Clock Input MCLK

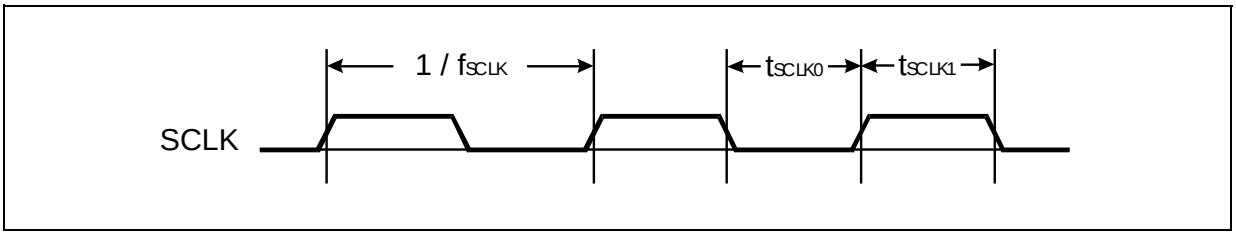
Figure 5. Timing of clock MCLK and related outputs



Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MCLK}	Clock frequency MCLK	12		64	MHz
t_{MCLK0}	MCLK low	6			ns
t_{MCLK1}	MCLK high	6			ns
t_{MCLD}	Output delay rising edge MCLK to DMAREQR/T, CON_CLK, DIV_CLK			20	ns
f_{MCLK}	Baudrate 2 Mbit/s	12		64	MHz
f_{MCLK}	Baudrate 4 Mbit/s	12		64	MHz

3.5.2 Clock Input SCLK

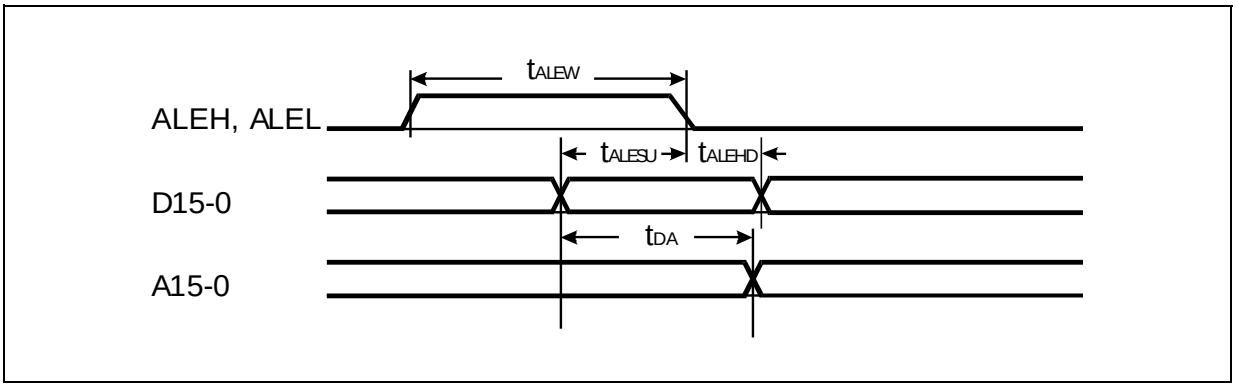
Figure 6. Timing of Clock SCLK



Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCLK}	Clock frequency SCLK				
	PLL used (SBAUD16=0)	32		64	MHz
	PLL unused (SBAUD16=1)			64	MHz
t_{SCLK0}	SCLK low	6			ns
t_{SCLK1}	SCLK high	6			ns

3.5.3 Address Latch

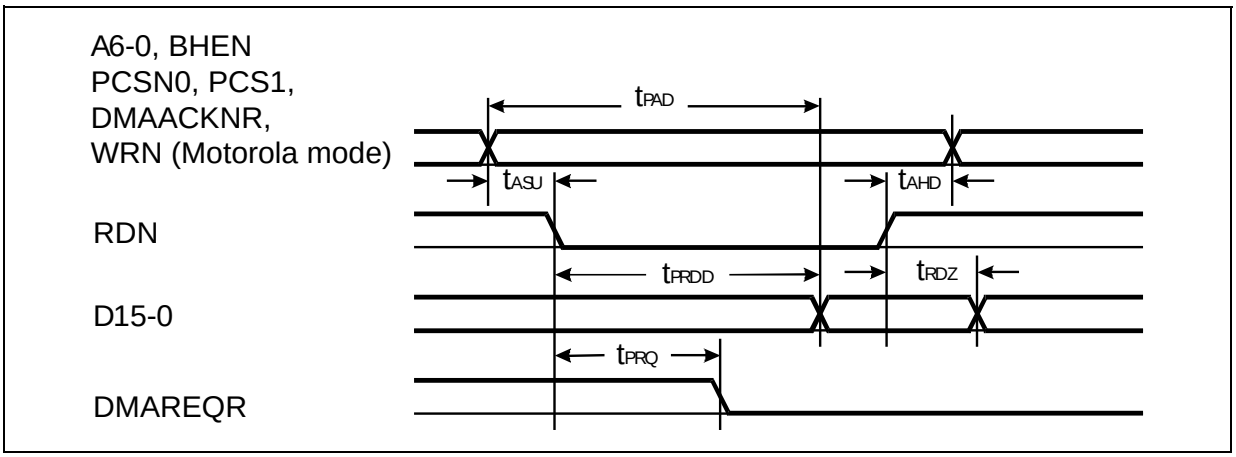
Figure 7. Address Latch



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{ALEW}	Pulse width ALEL, ALEH	10			ns
T_{ALESU}	Setup time D15-0 to falling edge ALEH, ALEL	5			ns
T_{ALEHD}	hold time falling edge ALEH, ALEL to D15-0	5			ns
t_{DA}	Delay from D15-0 to A15-0			20	ns

3.5.4 Read Access of Control Registers

Figure 8. Read Access of Control Registers

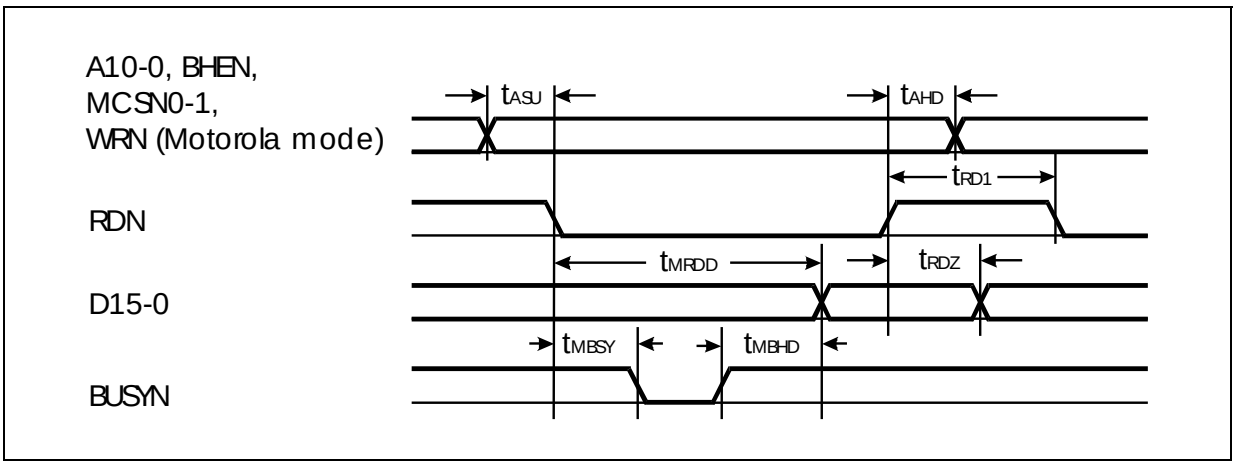


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ASU}	Setup time A6-0, (Note 1)	10			ns
	Setup time BHEN, PCSN0, PCS1, DMAACKNR, WRN (only Motorola mode), (Note 1)	0			ns
t_{AHD}	Hold time A6-0, BHEN, PCSN0, PCS1, DMAACKNR, WRN (only Motorola mode) to rising edge RDN (Intel Motorola mode with low active strobe) or falling edge RDN (Motorola mode with high active strobe)	0			ns
t_{PAD}	Access time A6-0, BHEN, PCSN0, PCS1, DMAACKNR, WRN (only Motorola mode) to D15-0 valid			30	ns
t_{PRDD}	Access time RDN to D15-0 valid			30	ns
t_{RDZ}	Delay RDN to D15-0 high-Z			20	ns
t_{PRQ}	Delay RDN to DMAREQR low			20	ns

Note: 1. Setup time input signals to falling edge RDN (Intel or Motorola mode with low active strobe) or rising edge RDN (Motorola mode with high active strobe)

3.5.5 Read Access of Dual Port RAM

Figure 9. Read Access of Dual Port RAM

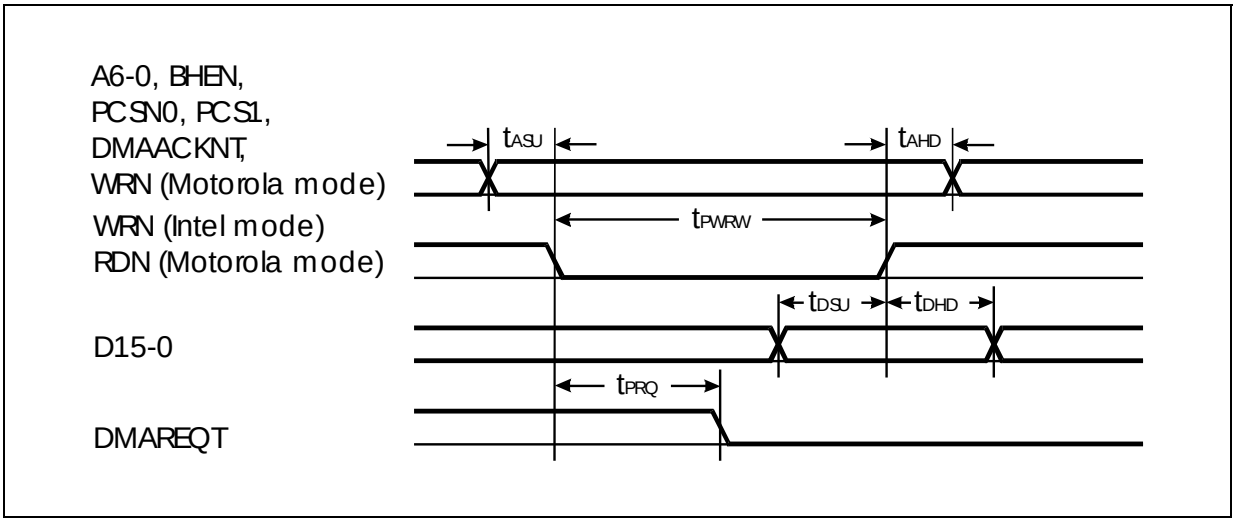


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ASU}	Setup time A11-0, (Note 1)	10			ns
	Setup time MCSN0-1, if both signals are activated simultaneously. (Note 1)	5			ns
	Setup time MCSN0-1, if one of these both signals is activated 10 ns earlier. (Note 1)	0			ns
	Setup time BHEN, WRN (only Motorola mode), (Note 1)	0			ns
t_{AHD}	hold time A11-0, BHEN, MCSN0-1, WRN (only Motorola mode) to rising edge RDN (Intel Motorola mode with low active strobe) or falling edge RDN (Motorola mode with high active strobe)	0			ns
t_{RDNCLK}	Cycle time of RAM read clock SBAUD16 = 1 ($f_{RDNCLK} = f_{SCLK}$) SBAUD16 = 0 ($f_{RDNCLK} = 2 * f_{SCLK}$)		 $1 / f_{SCLK}$ $0.5 / f_{SCLK}$		
t_{MRDD}	access time RDN to D15-0 valid			$2 * t_{RDNCLK} + 30$	ns
t_{MBSY}	delay RDN to BUSYN low			15	ns
t_{MBHD}	Delay BUSYN high to D15-0 valid			$2 * t_{RDNCLK} + 30$	ns
t_{RDZ}	Delay RDN to D15-0 high-Z			20	ns
t_{RD1}	RDN and WRN high after end of read access	15			ns

Notes: 1. Setup time input signals to falling edge RDN (Intel or Motorola mode with low active strobe) or rising edge RDN (Motorola mode with high active strobe)

3.5.6 Write Access to Control Registers

Figure 10. Write Access to Control Registers

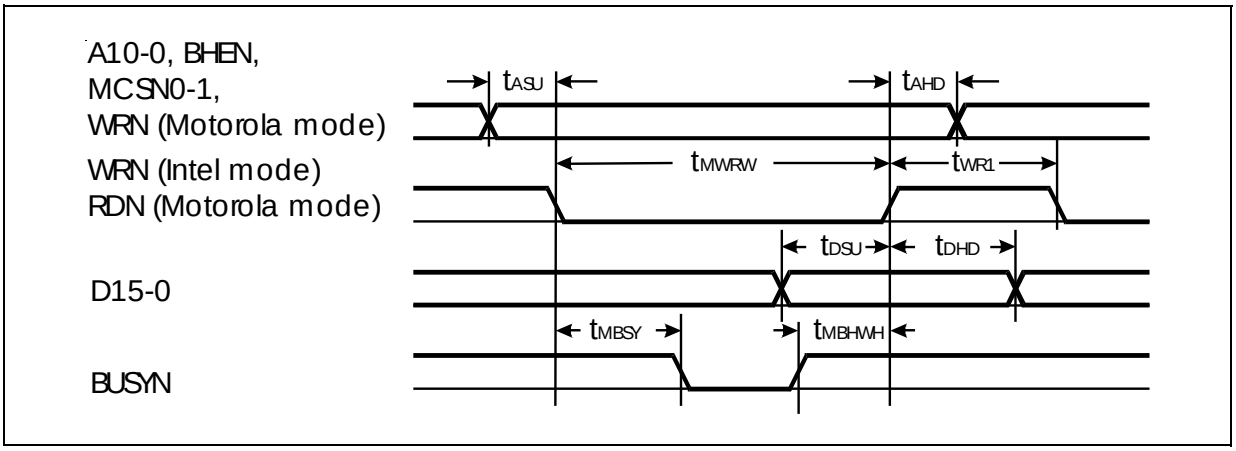


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ASU}	Setup time A6-0, (Note 1)	10			ns
	Setup time BHEN, PCSN0, PCS1, DMAACKNR, WRN (only Motorola mode), (Note 1)	0			ns
t_{AHD}	hold time A6-0, BHEN, PCSN0, PCS1, DMAACKNT, WRN (only Motorola mode) to rising edge WRN (Intel mode) or RDN (Motorola mode, strobe active low) or falling edge RDN (Motorola mode, strobe active high)	0			ns
t_{PWRW}	pulse width WRN (Intel mode) or RDN (Motorola mode)	20			ns
t_{DSU}	setup time D15-0 to end of write access	10			ns
t_{DHD}	hold time D15-0 to end of write access	5			ns
t_{PRQ}	delay WRN or RDN to DMAREQT low			20	ns

Notes: 1. Setup time input signals to falling edge WRN (Intel mode) or RDN (Motorola mode with low active strobe) or rising edge RDN (Motorola mode with high active strobe)

3.5.7 Write Access to DUAL Port RAM

Figure 11. Write Access to DUAL Port RAM



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ASU}	Setup time A11-0, (Note 1)	10			ns
	Setup time MCSN0-1, if both signals are activated simultaneously. (Note 1)	5			ns
	Setup time MCSN0-1, if one of these both signals is activated 10 ns earlier. (Note 1)	0			
	Setup time BHEN, WRN (only Motorola mode), (Note 1)	0			ns
t_{AHD}	hold time A11-0, BHEN, MCSN0-1, WRN (only Motorola mode) to rising edge of WRN (Intel mode) or RDN (Motorola mode with low active strobe) or falling edge RDN (Motorola mode with high active strobe)	0			ns
t_{MWRW}	Pulse width WRN or RDN	20			ns
t_{DSU}	Setup time D15-0 to end of write access	10			ns
t_{DHD}	Hold time D15-0 after end of write access	5			ns
t_{MBSY}	Delay WRN or RDN (begin of write access) to BUSYN low			15	ns
t_{MBHWH}	Setup time BUSYN high to end of write access	15			ns
t_{WR1}	WRN and RDN high after end of write access	15			ns

Notes: 1. Setup time input signals to falling edge WRN (Intel mode) or RDN (Motorola mode with low active strobe) or rising edge RDN (Motorola mode with high active strobe)

4 CONTROL REGISTERS AND RAM DATA STRUCTURES

4.1 Control Register Addresses

The following table is an overview of the control registers. The address is the word address which is input by A6-1. To calculate the byte address, the value has to be multiplied by two. All control registers can be written to and read (R/W), with the exception of the control bits that initiate an action (W).

The status registers can only be read (R). When control registers which contain bits that are not used or can only be read, are written to, these bits can be set to 0 or 1; they are not evaluated internally. If control registers are read with bits that are not used, these bits are set to 0.

A6-1	Bits	Name	R/W	Value	Function
00H	0-15	VERSION	R	0010H	Circuit code (**0010H**)
01H - 2AH	0-15	Please refer to SERCON816 Reference Guide for a detailed description of the control registers.			

4.2 Data Structures within the RAM

In this RAM the first eleven words have a fixed meaning.

A10-1	Contents
0-1	COMPT0-1: Start of transmission blocks 0-1
2-9	SCPT0-7: Address service containers 0-7
10	NMSTERR: Error counter MST

The rest of the RAM can be divided into data structures as required.

4.2.1 Telegram Headers

A telegram header for receive telegram contains the following five control words:

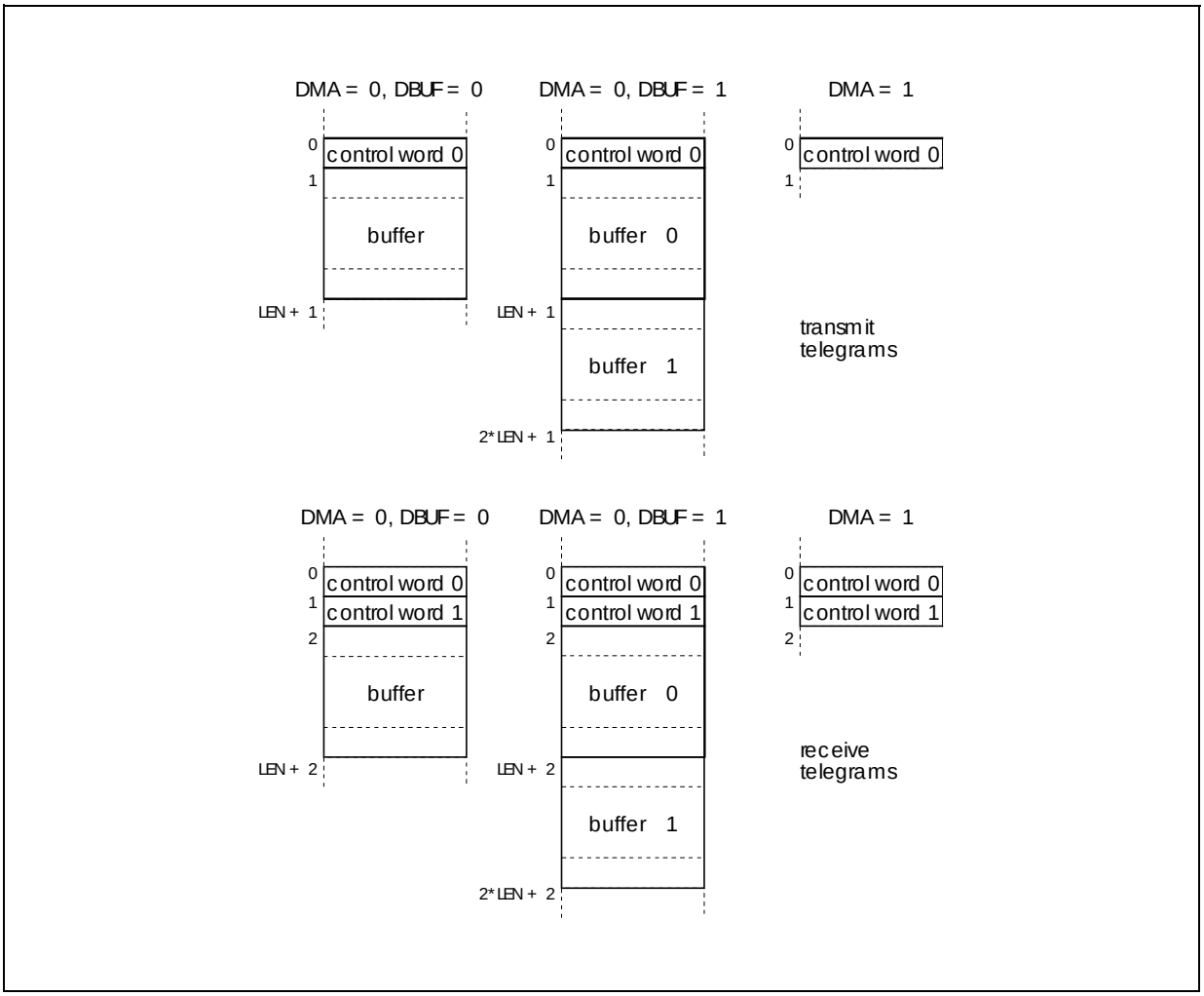
Index	Bit	Name	Function
0	0-7	ADR	Telegram address
	8	DMA	Data storage in the internal RAM (DMA = 0) or DMA transfer (DMA = 1)
	9	DBUF	Data in the RAM: single buffer (DBUF = 0) or double buffer (DBUF = 1)
	10	VAL	For single buffering (DMA = 0, DBUF = 0) or DMA transfer (DMA = 1): telegram data is invalid (VAL = 0) or valid (VAL = 1); for double buffering (DMA = 0, DBUF = 1): data in buffer 0 (VAL = 0) or buffer 1 (VAL = 1) is valid. Modified by controller at beginning and end of receive telegrams.
	11	ACHK	Telegrams are received if the address is valid (ACHK = 1) or independent on the received address (ACHK = 0). The received address is stored at ADR.
	12	TCHK	The time of receiving is checked (TCHK = 1) or not checked (TCHK = 0).
	13	RERR	The last telegram was free of error (RERR = 0) or errored or not received (RERR = 1).
	14	0	Marker bit for telegram header of receive telegram.
	15	0	Marker bit for telegram header.
1	0-15	TRT	Time for the start of telegram in µs after end of MST.
2	0-15	TLEN	Length of telegram in data words (not including address).
3	0-10	PT	Word address within the RAM of the next telegram header or the end marker.
	9-15		(Not used)
4	0-15	NERR	Error counter

4.2.2 Data Containers

A data container comprises one or two 16-bit control words as well as a variable number of data words. If the data is stored in the internal RAM (DMA = 0) and a single buffer is used (DBUF = 0), the data container has one buffer. Using RAM storage and double buffering (DBUF = 1), two data buffers are needed. In case of DMA transfer (DMA = 1) the data container only comprises the control words (Fig. 12). The structure of the two control words depends on whether a telegram is transmitted or received:

Index	Bit	Name	Function
0	0-9	LEN	Number of 16-bit data words of the data block.
	10	SVFL	Flag, whether data block uses service container (SVFL = 1).
	11-13	NSV	Number of service container, which is used (0 - 7).
	14	SCMASTER	Processing of service container in slave mode (SCMASTER = 0) or master mode (SCMASTER = 1).
	15	LASTDC	Last data container of the telegram (1) or further data containers follow (0).
1	0-15	POS	Position of the data block within the telegram in number of words. The first data record of a telegram has POS = 0 (only in case of receive telegrams).

Figure 12. Structure of Data Containers



4.2.3 End Marker

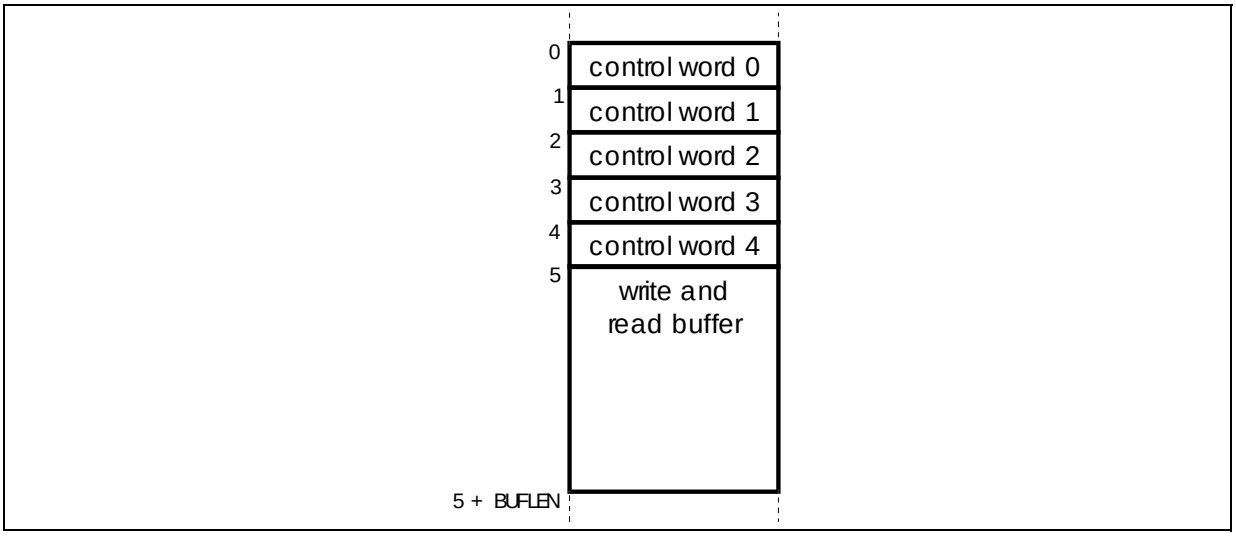
The end marker comprises two 16-bit words:

Index	Bit	Name	Function
0	0-13		(Not used)
	14	1	Marker bit for the end marker.
	15	1	Marker bit for the end marker.
1	0-15	TEND	Time after end of MST at which the last telegram has ended (in µs).

4.2.4 Service Containers

A service container contains 5 control words and a buffer (BUFLEN words, max. length 255)

Figure 13. Structure of Service Container



For master mode (SCMASTER = 1) the control words are coded as follows:

Index	Bit	Name	Function
0	0	HS_MDT	Handshake-bit in MDT
	1	L/S_MDT	Read/write in MDT
	2	END_MDT	End in MDT
	3-5	ELEM_MDT	Data element type in MDT
	6	SETEND	END_MDT is to be set
	7	M_BUSY	Service container waits for interaction of microprocessor (M_BUSY = 1)
	8-9	NINFO_WRITE	Number of info words in write buffer (1 to 4)
	10-11		(Not used)
	12	INT_ERR	Slave reports error
	13	INT_END_WRBUF	End of write buffer is reached
	14	INT_END_RDBUF	End of read buffer is reached
	15		(Not used)
1	0	HS_AT	Handshake bit in AT
	1	BUSY_AT	Busy bit in AT
	2	ERR_AT	Error bit in AT
	3	CMD_AT	Command modification bit in AT
	4-6		(Not used)
	7	RECERR	Last transmission was correct (0) or erroneous (1)
	8-9	NINFO_READ	Number of info words in read buffer (1 to 4)
	10-15		(Not used)
2	0-7	WRDATPT	Pointer to present position in write buffer
	8-15	WRDATLAST	Pointer to last position in write buffer
3	0-7	RDDATPT	Pointer to present position in read buffer
	8-15	RDDATLAST	Pointer to last position in read buffer
4	0-7	ERR_CNT	Error counter
	8	BUSY_CNT	Error counts differences of handshake (0) or BUSY cycles (1)
	9	INT_SC_ERR	Interrupt due to protocol error
	10	INT_HS_TIMEOUT	Interrupt due to handshake timeout
	11	INT_BUSY_TIMEOUT	Interrupt BUSY timeout
	12	INT_CMD	Slave has set command modification bit
	13-15		(Not used)

The coding of the five control words depends on the mode of the service channel. Using the slave mode (SCMASTER = 0) they have the following structure:

Index	Bit	Name	Function
0	0	HS_AT	Handshake bit in AT
	1	BUSY_AT	Busy bit in AT, also waiting for microprocessor interaction
	2	ERR_AT	Error bit in AT
	3	CMD_AT	Command modification bit in AT
	4-6	ELEM	Data element of present transmission
	7	L/S	Read (0)/write (1) of present transmission
	8-9	NINFO_WRITE	Number of info words in write buffer (1 to 4)
	10-11		(Not used)
	12	INT_ELEM_CHANGE	Master has modified data element or read/write
	13	INT_END_WRBUF	End of write buffer is reached
	14	INT_END_RDBUF	End of read buffer is reached
	15	INT_END_MDT	Master reports end via END_MDT-bit
1	0	HS_MDT	Handshake bit in MDT
	1	L/S_MDT	Read/write in MDT
	2	END_MDT	End bit in MDT
	3-5	ELEM_MDT	Data element in MDT
	6		(Not used)
	7	RECERR	Last transmission was correct (0) or erroneous (1)
	8-9	NINFO_READ	Number of info words in read buffer (1 to 4)
	10-15		(Not used)
2	0-7	WRDATPT	Pointer to present position in write buffer
	8-15	WRDATLAST	Pointer to last position in write buffer
3	0-7	RDDATPT	Pointer to present position in read buffer
	8-15	RDDATLAST	Pointer to last position in read buffer
4	0-8		(Not used)
	9	INT_SC_ERR	Interrupt due to protocol error
	10-15		(Not used)

5 ADDITIONAL SPECIFICATIONS, TOOLS AND SUPPORT

5.1 Additional Specifications

Reference Manual SERCON816

The reference manual (160 pages) for the SERCON816 Asic contains a complete and very detailed specification of the SERCON816 Asic, including a description of the pinning of the controller, microprocessor interface, serial interface, telegram processing, master and slave modes, additional modes, control and RAM data structures, programming examples, electrical and mechanical characteristics of the chip, differences between SERCON816 and SERCON410B controller.

SERCOS interface specification

The SERCOS interface specification (IEC/EN 61491) contains a detailed description of the transfer medium and physical layer, data transfer and data link layer, protocol structure and data contents, communication phases, functional handling and error handling, list and description of identifier numbers.

I/O functions are described in a separate document.

5.2 Hardware and Software Components

Master and slave routines (driver software) for the SERCON816 controller are available from several suppliers world-wide. Furthermore different boards for a wide range of computer interfaces are offered, including ISA-, VME-, PCI- and PC/104 bus systems.

5.3 Tools

Different development and testing tools are available for SERCOS interface.

These tools include bus monitors, configuration and simulation tools, as well as tools for conformance testing.

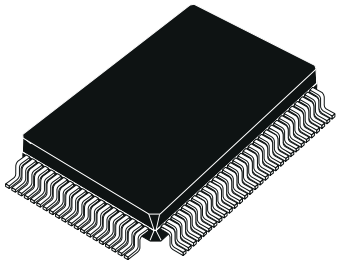
For all specification and additional application notes please contact:

Interests Group SERCOS interface e. V.

6 PACKAGE MECHANICAL DATA: SERCON816 100 PIN PLASTIC QUAD FLAT PACK PACKAGE (PQFP100)

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



PQFP100