




MK2731-03C MPEG Audio Clock Synthesizer

Description

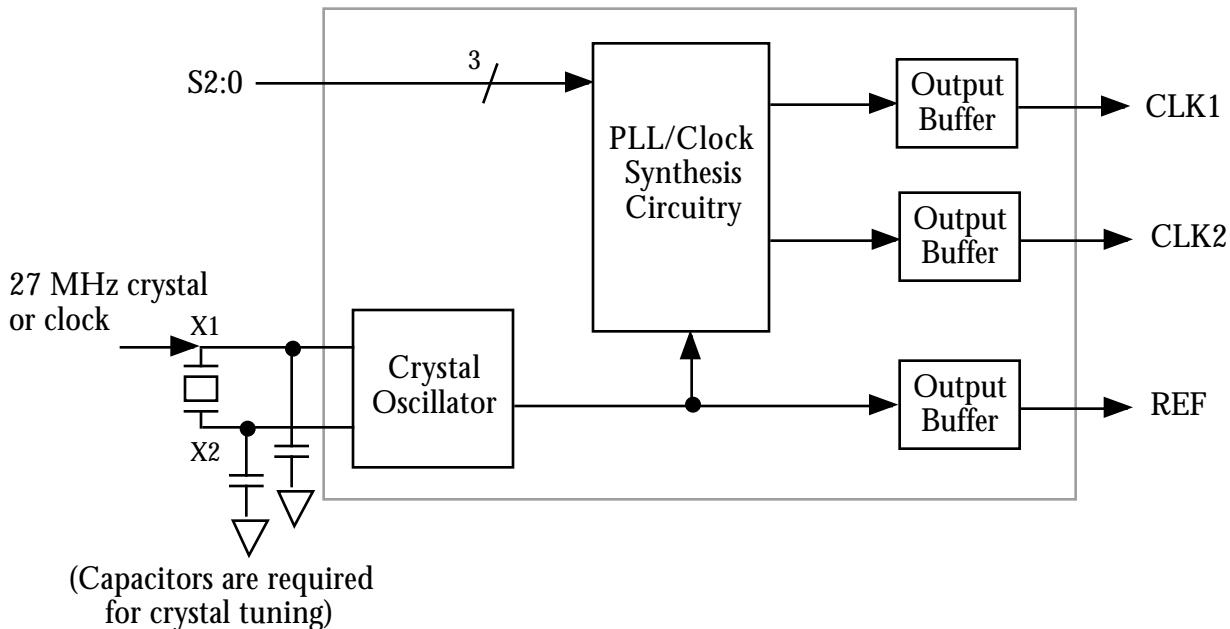
The MK2731-03 is a low cost, low jitter, high performance PLL clock synthesizer designed to replace oscillators and PLL circuits in set-top box and multimedia systems. Using our proprietary analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive crystal or clock input to produce up to three output clocks. All of the audio frequencies are synthesized exactly, with zero ppm error, and locked to the 27 MHz clock.

MicroClock manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult MicroClock to eliminate VCXOs, crystals and oscillators from your board.

Features

- Packaged in 16 pin narrow SOIC 
- Produces exact audio clocks from the video
- Uses a crystal or clock input
- Zero ppm synthesis error in all clocks
- All frequencies are frequency locked
- 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3V or 5V operating voltage

Block Diagram





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Pin Assignment

MK2731-03C

X2	□ 1	16	□ REF
X1	□ 2	15	□ NC
VDD	□ 3	14	□ CLK2
VDD	□ 4	13	□ S0
GND	□ 5	12	□ NC
GND	□ 6	11	□ S1
S2	□ 7	10	□ CLK1
GND	□ 8	9	□ DC

16 pin narrow (150 mil) SOIC

Output Clock Select Table (MHz)

Input	S2	S1	S0	CLK1	CLK2	REF
27	0	0	0	Off	8.192	Off
27	0	0	1	Off	11.2896	Off
27	0	1	0	Off	12.288	Off
27	0	1	1	Off	24.576	Off
27	1	0	0	4.096	8.192	27
27	1	0	1	5.6448	11.2896	27
27	1	1	0	6.144	12.288	27
27	1	1	1	12.288	24.576	27

Key: 0 = connect pin directly to ground
 1 = connect pin directly to VDD
 Off = clock stopped low

Pin Descriptions

Number	Name	Type	Description
1	X2	XO	Crystal connection to a 27 MHz fundamental crystal. Leave unconnected for clock input.
2	X1	XI	Crystal connection to a 27 MHz fundamental crystal. Can also be connected to input clock.
3	VDD	P	VDD. Connect to VDD.
4	VDD	P	VDD. Connect to VDD.
5	GND	P	Connect to ground.
6	GND	P	Connect to ground.
7	S2	I	Clock Select 2. Selects outputs per table above.
8	GND	P	Connect to ground.
9	DC	-	Do not connect anything to this pin.
10	CLK1	O	Clock output 1 determined by status of S2, S1, S0. See table above.
11	S1	I	Clock Select 1. Selects outputs per table above.
12	NC	-	No Connect. Nothing is connected internally to this pin.
13	S0	I	Clock Select 0. Selects outputs per table above.
14	CLK2	O	Clock output 2 determined by status of S2, S1, S0. See table above.
15	NC	-	No Connect. Nothing is connected internally to this pin.
16	REF	O	Reference crystal output or off. See table above.

Key: I = Input, O = output, P = power supply connection



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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless noted)					
Operating Voltage, VDD		3.13		5.50	V
Input High Voltage, VIH, X1 pin only		(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, X1 pin only			VDD/2	(VDD/2)-1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		25		mA
Short Circuit Current	Each output		±100		mA
Input Capacitance	S2, S1, S0		7		pF
Frequency synthesis error	All clocks			0	ppm
AC CHARACTERISTICS (VDD = 5.0V unless noted)					
Input Crystal or Clock Frequency			27.00		MHz
Input Crystal Accuracy				±30	ppm
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At 1.4V	40		60	%
Maximum Absolute Jitter, short term		see table on following page			

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

The MK2731-03 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF should be connected between VDD and GND on pins 3 and 5, as close to the MK2731-03 as possible. A series termination resistor of 33Ω may be used for each clock output. The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel resonant, fundamental, AT cut 27 MHz. For accurate tuning of the output when a crystal input is used, capacitors should be connected between X1 and ground, and X2 and ground. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = $(C_L - 10) \times 2$. So for a crystal with 16 pF load capacitance, two 12 pF caps can be used.



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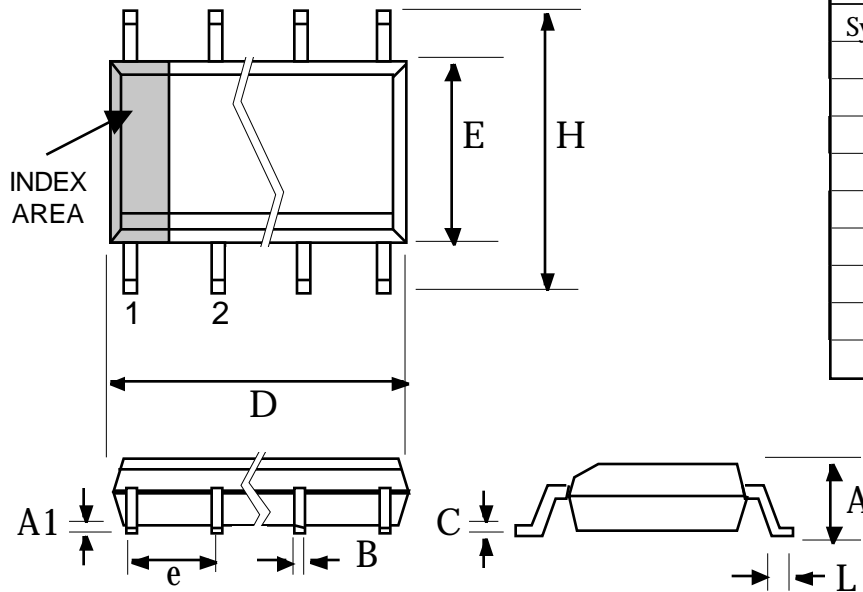
Jitter Measurements

S2	S1	S0	CLK2 (MHz)	5V		3.3V	
				one sigma (ps)	typical max (\pm ps)	one sigma (ps)	typical max (\pm ps)
0	0	0	8.192	45	110	92	185
0	0	1	11.2896	25	60	42	110
0	1	0	12.288	24	70	49	130
0	1	1	24.576	32	90	52	150

Notes: 1. Jitter is about equal at 25°C and 70°C

Package Outline and Package Dimensions

16 pin SOIC narrow



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2731-03S	MK2731-03S	tubes	16 pin SOIC	0-70 °C
MK2731-03STR	MK2731-03S	tape and reel	16 pin SOIC	0-70 °C

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