Product Preview

LCD Monitor On-Screen Display II - 16 (LMOSD2-16)
CMOS

MC141585

DW SUFFIX
SOIC PACKAGE

ORDERING INFORMATION
MC141585   SOIC

This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto a LCD monitor. Because of the large number of fonts, 512 fonts including 496 standard fonts and 16 mulit-color fonts, LMOSD2-16 is suitable to be adopted for the multi-language monitor application especially. It minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision. Programmable hatch pattern generator is added for individual pixel inspection.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. The full OSD menu is formed of 15 rows x 30 columns which can by freely positioned on anywhere of the monitor screen by changing vertical or horizontal delay.

Special functions such as character background color, blinking, bordering or shadowing, four-level windows with programmable size, row double height and double width, programmable vertical height of character and row-to-row spacing, and full-screen erasing and Fade-In/Fade-Out are also incorporated. There are 8 color selections for any individual character display with row intensity attribute and window intensity attribute to expand the color mixture on OSD menu.

PIN ASSIGNMENT

V_{SS}	1	16	V_{SS}
PIXin	2	15	R
NC	3	14	G
V_{DD}	4	13	B
$\overline{HSYNC}$	5	12	FBKG
$\overline{RESET}$	6	11	VDD(I)
SDA	7	10	$\overline{VSYNC}$
SCL	8	9	V_{DD}

- Totally 512 Fonts Including 496 Standard Fonts and 16 Multi-Color Fonts.
- 10x18 or 12x18 Font Matrix Selection
- Maximum Pixel CLK of 80MHz
- Maximum input resolution of 1580 dots/line(PIXin/HSYNC ratio)
- Wide Operating Frequency: max. 150KHz for Monitor
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- 7-Color Selection for Characters background
- True 16-Color Selection for Windows
- Shadowing on Windows with Programmable Shadow Width/Height/Color
- Fancy Fade-In/Fade-Out Effects
- Programmable Height of Character to Meet Multi-Sync Requirement
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
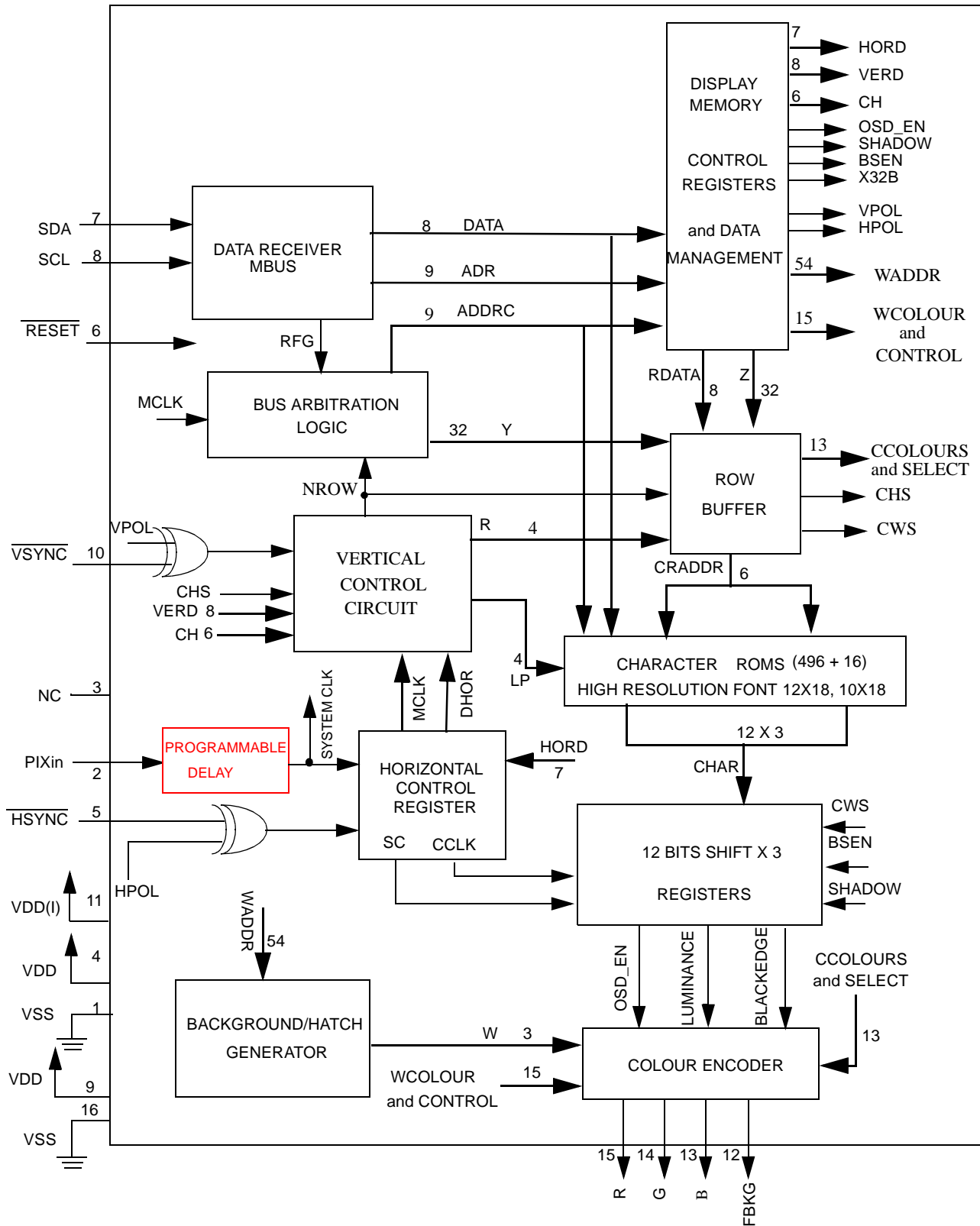- Programmable Vertical and Horizontal Positioning for Display Centre
- M_BUS (IIC) Interface with Address $7A
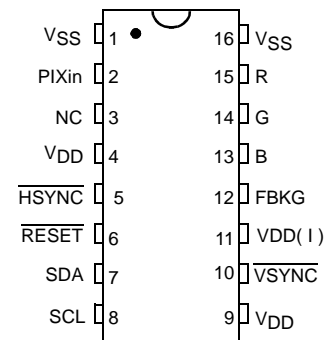
- This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	− 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} − 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

**AC ELECTRICAL CHARACTERISTICS** ($V_{DD}/V_{DD(I)}$ = 5.0+/-5% V, V_{SS} = 0 V, TA = 0-70C) (Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, and FBKG) C_{load} = 30 pF				
t_r	Rise Time (Refer to Figure 1)	—	3	—	ns
t_f	Fall Time (Refer to Figure 1)	—	3	—	ns
t_{setup}	Setup time (Refer to Figure 3)				
	Programmable Propagation Delay Step = 0	TBD	—	—	ns
	Programmable Propagation Delay Step = 1	TBD	—	—	ns
	Programmable Propagation Delay Step = 2	TBD	—	—	ns
	Programmable Propagation Delay Step = 3	TBD	—	—	ns
	Programmable Propagation Delay Step = 4	TBD	—	—	ns
	Programmable Propagation Delay Step = 5	TBD	—	—	ns
	Programmable Propagation Delay Step = 6	TBD	—	—	ns
	Programmable Propagation Delay Step = 7	TBD	—	—	ns
t_{hold}	Hold time (Refer to Figure 3)	TBD	—	—	ns
tpd	Output Signal (R, G, B and FBKG) C_{load} = 30 pF				
	Propagation Delay of output to pixel clock(Figure 2):				
	Programmable Propagation Delay Step = 0	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 1	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 2	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 3	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 4	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 5	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 6	TBD	—	TBD	ns
	Programmable Propagation Delay Step = 7	TBD	—	TBD	ns
PIXin	Pixel clock input	—	—	80	MHz
$F_{\overline{HSYNC}}$	$\overline{HSYNC}$ Input Frequency	—	—	150K	Hz
$F_{\overline{VSYNC}}$	$\overline{VSYNC}$ Input Frequency	—	—	200	Hz

DC CHARACTERISTICS V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage (R,G,B,FBKG) , I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage (R,G,B,FBKG), I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	— 0.7 V_{DD}	— —	0.3 V_{DD} —	V V
V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	— 0.7 V_{DD}	— —	0.3 V_{DD} —	V V
V_{IL} V_{IH}	Input Voltage of PIXin pin Logic Low Logic High	— 4.0	— —	1 —	V V
I_{II}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	μA
I_{II}	Input Current ($\overline{HSYNC}$,$\overline{VSYNC}$,$\overline{RESET}$, SDA, SCL)	– 10	—	+ 10	μA
I_{DD}	Supply Current (No Load on Any Output) at V_{DD}=5.0V	—	—	+ 26	mA
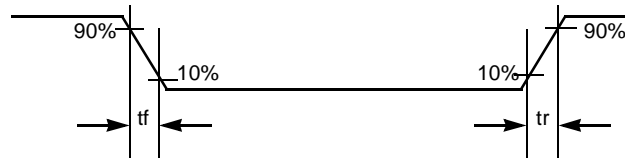
Figure 1. Switching Characteristics
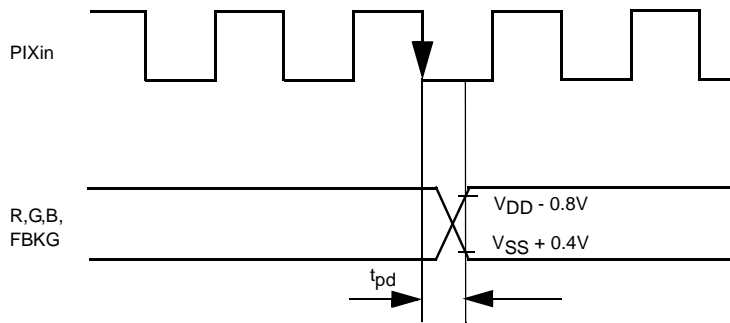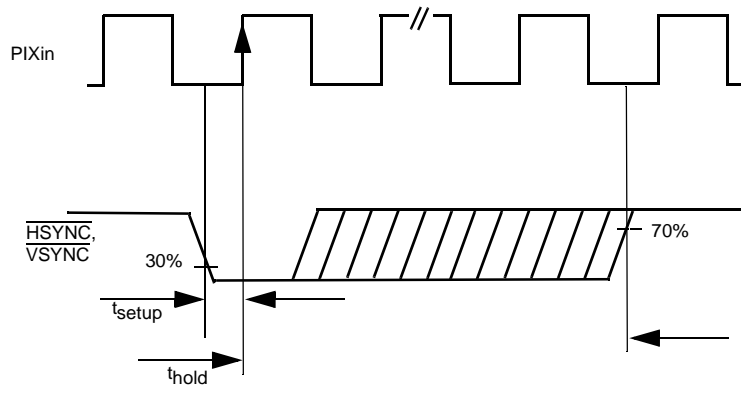

Figure 2. Propagation Delay Diagram

Figure 3. Setup/Hold Timing Diagram

PIN DESCRIPTION

VSS(Pin 1)
This is the ground pin for the chip.

PIXin (Pin 2)
This is the Pixel clock input for chip. The MC141585 chip is driven by this pixel clock for all the logics inside.

NC (Pin 3)
No connection.

V$_{DD}$ (Pin 4)
This is the +5V power pin for the chip.

$\overline{\text{HSYNC}}$ (Pin 5)
This pin inputs a horizontal synchronize signal. It is negative polarity by default. The leading edge of $\overline{\text{HSYNC}}$ synchronizes its internal horizontal timing. The maximum input ratio between PIXin/HSYNC should not greater than 1580 for displaying 12X18 font matrix. For displaying 10X18 font matrix, this ratio should not greater than 1280.

$\overline{\text{RESET}}$ (Pin 6)
An active low signal will reset ROW15 and ROW16 control registers. Refer to Control Registers section for default settings. A proper RC network have to be tighted to this pin to ensure the device initialize properly during power up. Refer to the application diagram.

SDA (Pin 7)
Data and control message are being transmitted to this chip from a host MCU via M_bus systems. This wire is configurated as a uni-directional data line. (Detailed description of protocols will be discussed in the M_BUS section).

SCL (Pin 8)
A separate synchronizing clock input from the transmitter is required for M_Bus protocol. Data is read at the rising edge of each clock signal.

V$_{DD}$ (Pin 9)
This is the power pin for the digital logic of the chip.

$\overline{\text{VSYNC}}$ (Pin 10)
Similar to Pin 5, this pin inputs a vertical synchronize signal to synchronize the vertical control circuit. It is negative polarity by default.

V$_{DD}$(I) (Pin 11)
This is the voltage supply of RGB outputs when low intensity of Windows/ROW is selected. The RBG output level would be equal to VDD(I) in this case. Please refer to Row Attribute/Window registers for more detail. The input voltage for this pin should be equal to or less than V$_{DD}$(Pin 17) for normal operation.

FBKG (Pin 12)
This pin will output a logic high while displaying characters or windows. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13, 14, 15)
LMOSD2-16 color outputs in CMOS level to the host monitor. These three signals are open drain outputs if 3_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V$_{SS}$ (Pin 24)
This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION
MC141585 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via M_BUS. Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the LMOSD2-16 is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the LMOSD2-16 functions such as programmable vertical length (from 16 lines to 63 lines), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

M_BUS Serial Communication
This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 400 kbps.The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure
Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the

LMOSD2-16 circuitry of MC141585, so that the received information can then be displayed.
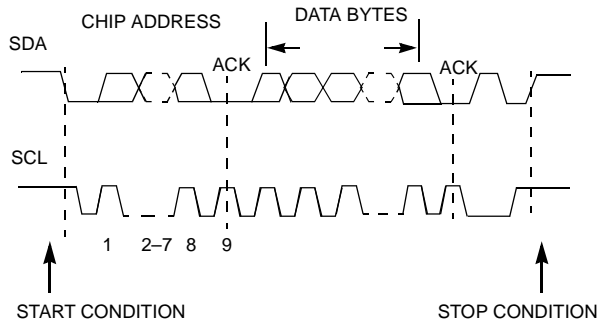

Figure 4. M_BUS Format

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, two register blocks, display registers, attribute/control registers, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:
(a) R - > C- > I -> R - > C - > I - > . . . .
(b) R - > C - > I - > C - > I - > C - > I. . . . . . .
(c) R - > C - > I - > I - > I - > . . - > I$_{dummy}$ - > I$_{dummy}$ - > I - > I. . .

NOTE: - R means row byte.
- C means column byte.
- I means data byte.
- In format (c), two dummy data bytes(col 30,

col 31)have to be inserted after the last data byte(col 29) at the end of each row, before the first data byte of the next row.

To differentiate the display row address from attribute area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).
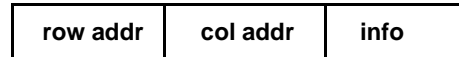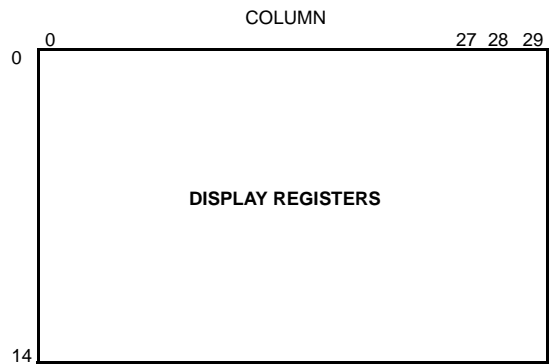
row addr	col addr	info

Figure 5. Data Packet for Display Data

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care   D: valid data

Figure 6. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:
(a) R - > C- > I -> R - > C - > I - > . . . .
(b) R - > C - > I - > C - > I - > C - > I. . . . . . .
(c) R - > C - > I - > I - > I - > . .- > I$_{row\ attr.}$ - > I$_{dummy}$ - > I - > I. . .

NOTE: - R means row byte.

- C means column byte.
- I means data byte.
- In format (c), one dummy data byte(col 31) has to be inserted after the row attribute data byte (col 30) at end of each row, before the first character attribute data byte of the next row.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).
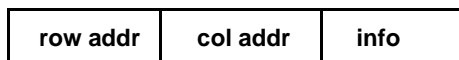
row addr	col addr	info

Figure 7. Data Packet for Attribute/Control Data
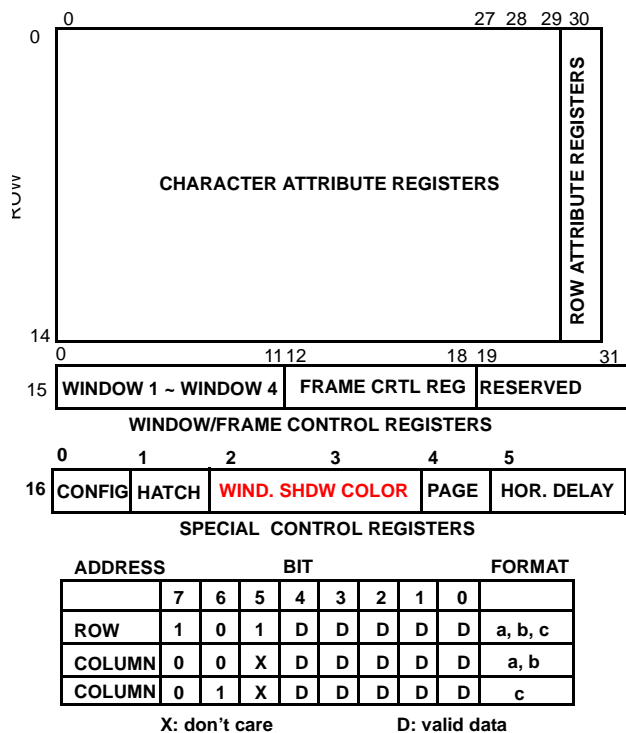
Figure 8. Address Bit Patterns for Attribute/Control Data

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	1	D	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care   D: valid data

MEMORY MANAGEMENT

All the internal programmable area can be divided into two parts including (1) Display Registers (2) Attribute/Control Registers. Please refer to the following two figures for the corresponding memory map.
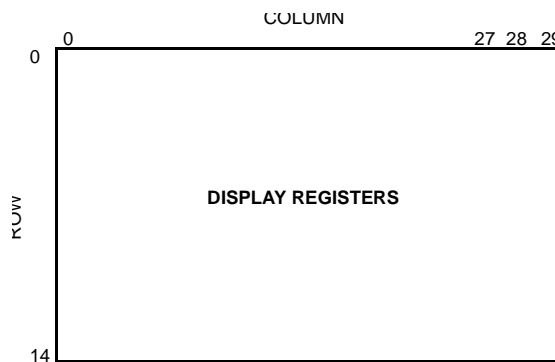

Figure 9. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 logical selected ROM fonts.
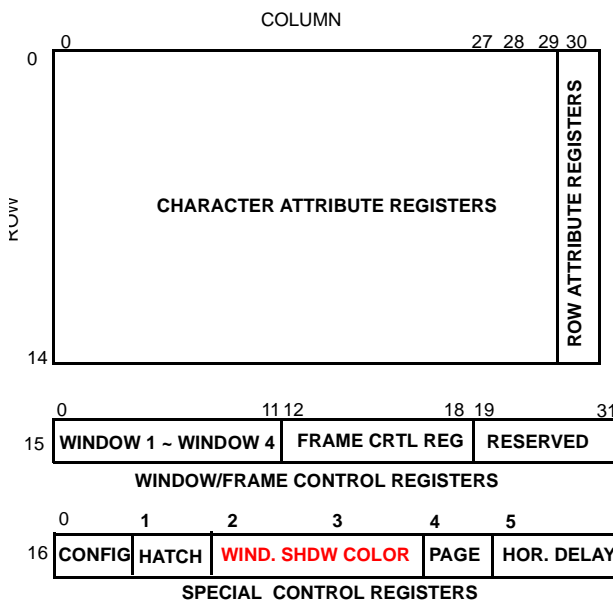

Figure 10. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color and 3-bit to define its background. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. as well as background. Every data row associate with one attribute register, which locate at coln 30 of their respective

rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control, frame function control. Four window control registers for each of four windows together with four frame control registers occupy the first 18 columns of row 15 space. These control registers will be described on the "REGISTERS" section. ROW 16, COL 0 - 4 contain special function registers for pattern generation and page ROM selection.

User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

REGISTERS

(I) Display Register

Display Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
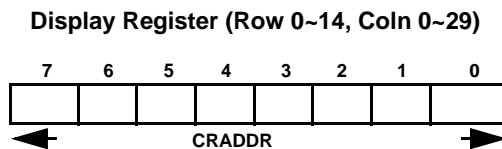
◄──────────── CRADDR ────────────►

Bit 7-0 CRADDR - This eight bits address one of the 256 characters or symbols resided in the 256 character ROM . The 256 character ROM is compose of Bank A, Bank B and Bank C. Bank A is fixed 128-ROM(address $00-$7F), Bank B is first page 64-ROM(address $80-$BF) and Bank C is second page 64-ROM(address $C0-$FF). Total addressable ROM is 256 out of 512 physical ROM. Pages(Page 1 to Page 6) in Bank B and Bank C can be selected by Page Selection Register, ROW16 COL 4.

(II) Attribute Registers

Character Attribute Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
X	BGR	BGG	BGB	BLINK	R	G	B
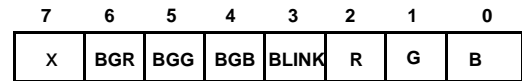
Bit 6-4   These three bits define the color of the background for the correspondent characters. If all three bits are clear, no background will be shown(transparent). Therefore, total seven background colors can be selected.

Bit 7   Don't Care.

Bit 3   BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

Bit 2-0   These three bits are the color attribute to define the color of the associated character/symbol.

Table 1. The Character/Window /Window shadow Color Selection

	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Row Attribute Register (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
					R_INT	CHS	CWS
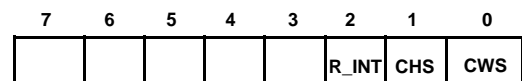
Bit 2   R_INT - Row intensity bit controls the color intensity of the displayed character/symbol on the corresponding row. Setting this bit to 0 means low intensity in this ROW and R,G,B output voltage level will be equal to $V_{DD}(I)$. Set this bit to 1 will switch the supply source of R,G,B back to VDD for high intensity. Default setting is 0.

The low intensity function is not supported for the characters inside a high intensity windows and such characters will still be high intensity even though R_INT is set 0. But inside a low intensity window, the characters can be selected to high or low intensity. Refer to W_INT bit description in the window register for selecting the window intensity.
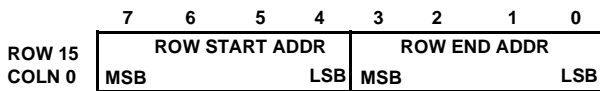
Bit 1   CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

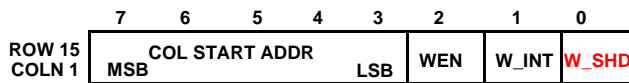Bit 0   CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

(III) Window/Control/Frame Register

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	MSB	ROW START ADDR		LSB	MSB	ROW END ADDR		LSB

Row 15 Coln 1

|	7	6	5	4	3	2	1	0
ROW 15 COLN 1	MSB	COL START ADDR		LSB	WEN	W_INT	W_SHD

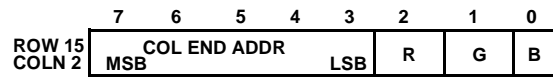Bit 2   WEN - It enables the window 1 generation if this bit is set.

Bit 1   W_INT - This additional color related bit provides the color intensity selection for window 1. Setting this bit to 0 means low intensity in this window and R,G,B output voltage level will be equal to $V_{DD}(I)$. Set this bit to 1 will switch the supply source of R,G,B back to VDD. Default setting is 0.

Bit 0   W_SHD - Shadowing on Window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17 and the shadow color can be selected in Window Shadow Color Registers at row16 Column 2 and 3. See the following figure and the related frame control register for detail.
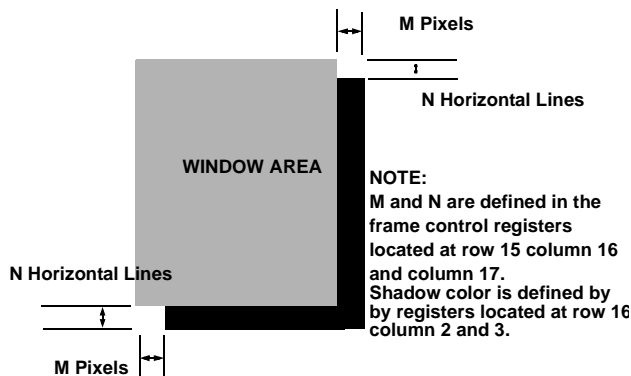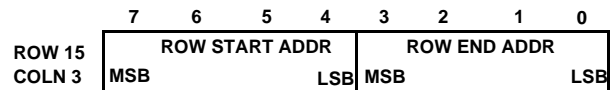

Window Shadowing

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	MSB	COL END ADDR			LSB	R	G	B

Bit 2-0   R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	MSB	ROW START ADDR		LSB	MSB	ROW END ADDR		LSB

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	MSB	COL START ADDR		LSB	WEN	W_INT	W_SHD

Bit 2   WEN - It enables the window 2 generation if this bit is set.

Bit 1   W_INT - This additional color related bit provides the color intensity selection for window 2. Setting this bit to 0 means low intensity in this window and R,G,B output voltage level will be equal to $V_{DD}(I)$. Set this bit to 1 will switch the supply source of R,G,B back to VDD. Default setting is 0.

Bit 0   W_SHD - Shadowing on Window. Set this bit to activate the window 2 shadowing.

Row 15 Coln 5

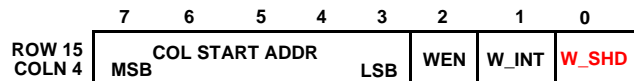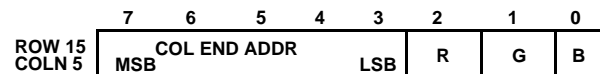|	7	6	5	4	3	2	1	0
ROW 15 COLN 5	MSB	COL END ADDR			LSB	R	G	B

Bit 2-0   R, G and B - Controls the color of window 2. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR MSB			LSB		WEN	W_INT	W_SHD

Bit 2   WEN - It enables the window 3 generation if this bit is set.

Bit 1   W_INT - This additional color related bit provides the color intensity selection for window 3. Setting this bit to 0 means low intensity in this window and R,G,B output voltage level equals to $V_{DD}(I)$. Set this bit to 1 will switch the supply source of R,G,B back to VDD. Default setting is 0.

Bit 0   W_SHD - Shadowing on Window. Set this bit to activate the window 3 shadowing.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 3. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	COL START ADDR MSB			LSB		WEN	W_INT	W_SHD

Bit 2   WEN - It enables the window 4 generation if this bit is set.

Bit 1   W_INT - This additional color related bit provides the color intensity selection for window 4. Setting this bit to 0 means low intensity in this window and R,G,B output voltage level will be equal to $V_{DD}(I)$. Set this bit to 1 will switch the supply source of R,G,B back to VDD. Default setting is 0.

Bit 0   W_SHD - Shadowing on Window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 4. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
ROW 15 COLN 12	VERTD MSB							LSB

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
ROW 15 COLN 13	MSB			HORD				LSB

Bit 7-0 HORD - Horizontal starting position for character display. 8 bits give a total of 256 steps and each increment represents 5 or 6 dots(10x18 or 12x18 font) movement shift to the right on the monitor screen. The movement of each step is base on half character size. The default value is 15.

Character Height Control Register Row 15 Coln 14

	7	6	5	4	3	2	1	0
ROW 15 COLN 14	X	0	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7   X - Don't care.

Bit 6   Reserved. Set to 0 for normal operation.

Bit 5-0   CH5-CH0 - This six bits will determine the displayed character height. LMOSD2 adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH

is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result.

Formula of character height is:

$H = N \times 18 + (CH3 : CH0)$

$N = 1$ if CH5:CH4=0,0 or 0,1

$N = 2$ if CH5:CH4=1,0

$N = 3$ if CH5:CH4=1,1

CHARACTER ENLARGEMENT

16≤CH<32   32≤CH<48   48≤CH<64

18 lines (1+16+1)

Built-in font
(12x18 matrix)
when CH=16

24 lines (1+22+1)

Display character
when CH=22

27 lines (1+25+1)

Display character
when CH=25
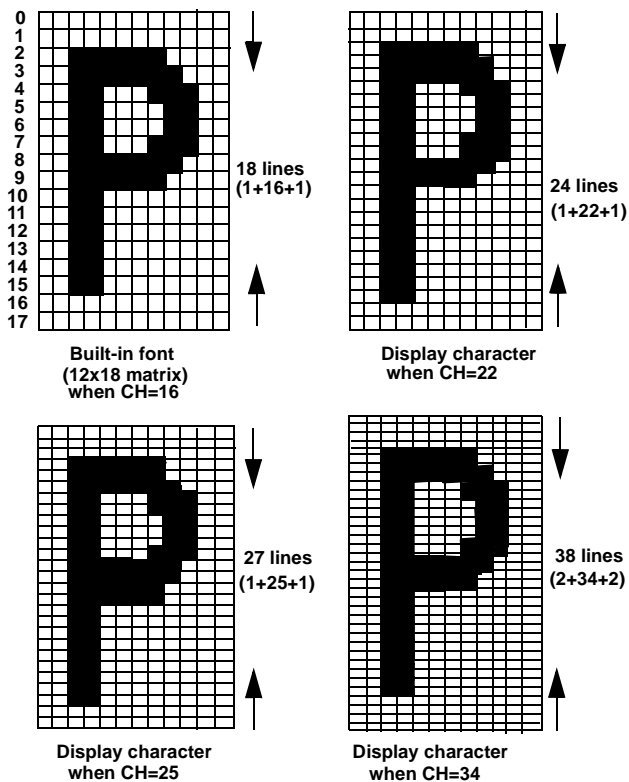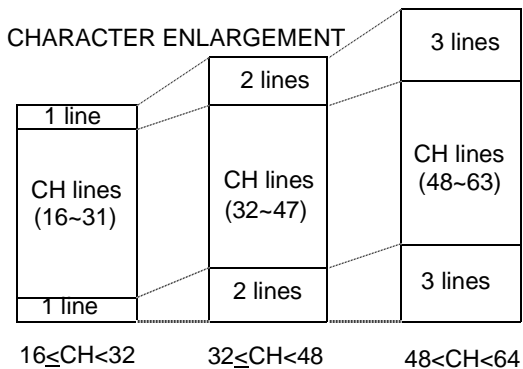
38 lines (2+34+2)

Display character
when CH=34

Figure 11. Variable Character Height

Figure 9 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

$H = CH + N$

Where   H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

N = 2 when 16≤CH<32

N = 4 when 32≤CH<48

N = 6 when 48≤CH<64

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW	X	X	X	FAD	0

Bit 7   OSD_EN - OSD circuit is activated when this bit is set.

Bit 6   BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5   SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Note: Both bordering and character shadowing functions are not supported when displaying multi-color characters($00-$10). BSEN & SHADOW bits should be kept "0" while there are multi-color characters displayed in the OSD menu.

Bit 4-2 Don't care.

Bit 1   FAD - It enables the fade-in/fade-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

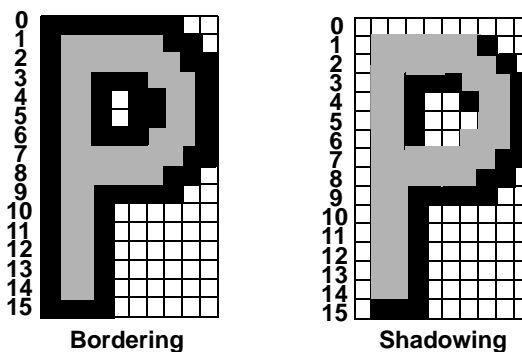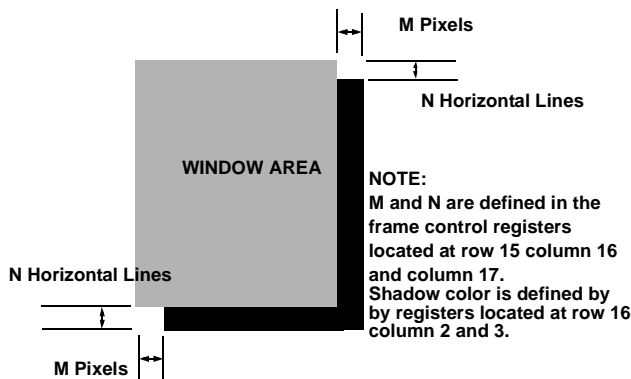Bit 0   Reserved - Set to "0" for normal operation.

Bordering   Shadowing

Figure 12. Character Bordering and Shadowing

M Pixels

N Horizontal Lines

WINDOW AREA

NOTE:
M and N are defined in the frame control registers located at row 15 column 16 and column 17.
Shadow color is defined by by registers located at row 16 column 2 and 3.

N Horizontal Lines

M Pixels

Window Shadowing

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
ROW 15 COLN 16	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 2. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 3. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

	7	6	5	4	3	2	1	0
ROW 15 COLN 18	MSB	RSPACE			LSB	TRIC	HPOL	VPOL

Bit 7-3 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on. It can be used for Portrait monitor too when icon design is rotated 90 degree.

Bit 2   TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1   HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{HSYNC}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0   VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{VSYNC}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

• **NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.**

(IV) Special Control Registers

Chip Configuration Register(Row16, Coln0)

7	6	5	4	3	2	1	0
CLR	FSS	INV	FSW	VE	HE	DE	DIV

Bit 7   CLR - By writing "1" to this bit, all display memory from Row 0 to Row 14 are all cleared but not affecting Control registers..

Bit 6   FSS - Font Size Selection

  1: 10x18 font size selected

  0: 12x18 font size selected

Bit 5   INV - Inverse the test pattern outputs from white to black and black to white vice versa.

Bit 4   FSW - Full Screen White Enable, setting "1" to this bit all the screen shown white. The vertical and horizontal hatch lines enabled by Bit 3 & Bit 4 in this register will be overridden. Full Screen White can be inversed by setting INV bit to "1".

Bit 3   VE - Vertical Line Enable, while writing "1" to this bit, the vertical hatch lines will be shown by the settings of V3, V2, V1, V0 in Hatch Line Space Register.

Bit 2   HE - Horizontal Line Enable, while writing "1" to this bit, the horizontal hatch lines will be shown by the settings of H3, H2, H1, H0 in Hatch Line Space Register.

Note:Compared with OSD outputs, FSW and the Hatch lines generation are at the lowest priority. In addition,when these test pattern are activated, the video signal from PC will be disable.

Bit 1   DE - PIXin Divider enable.

Bit 0   DIV - "0" divided by 2; "1" divided by 3.

Hatch Line Space Register(Row16, Coln1)

7	6	5	4	3	2	1	0
H_3	H_2	H_1	H_0	V_3	V_2	V_1	V_0

Bit 7-4 H3, H2, H1, H0 define line space of horizontal hatch lines.Zero is not allowed. Default value is 1.

t 3-0   V3, V2, V1, V0 define line space of vertical hatch lines. Zero is not allowed. Default value is 1.

The space is defined by the formula below:

Space of Horizontal Hatch lines = (H3, H2, H1, H0) X 3 + 3

Space of Vertical Hatch Lines = (V3, V2, V1, V0) X 4 + 4

The hatch lines are white when the INV bit is not set. The whole hatch pattern will be inversed by setting INV bit to "1".

Windows Shadow Color Register 1(Row16,Coln2)

7	6	5	4	3	2	1	0
X	R_2	G_2	B_2	X	R_1	G_1	B_1

This register defines the shadow colors of window 1 and window 2.

Bit 7   X, Don't Care.

Bit 6-4 R2, G2, B2 define the shadow color for window 2.

Bit 3   X, Don't Care.

Bit 2-0 R1, G1, B1 define the shadow color for window 1.

Windows Shadow Color Register 1(Row16,Coln3)

7	6	5	4	3	2	1	0
X	R_4	G_4	B_4	X	R_3	G_3	B_3

This register defines the shadow colors of window 3 and window 4.

Bit 7   X, Don't Care.

Bit 6-4 R4, G4, B4 define the shadow color for window 4.

Bit 3   X, Don't Care.

Bit 2-0 R3, G3, B3 define the shadow color for window 3.

Page Selection Registers(Row16,Coln4)

7	6	5	4	3	2	1	0
X	C_2	C_1	C_0	X	B_2	B_1	B_0

Bank A is fixed 128-ROM(address 00-7F). The register define the address pointers of Bank B(address 80-BF) and Bank C(address C0-FF) by A0-A2 and B0-B2.

Bit 7   X, Don't Care.

Bit 6-4 C2, C1, C0 define the page selected to Bank C.

Bit 3   X Don't Care.

Bit 2-0 B2, B1, B0 define the page selected to Bank B.

The default page in bank B is page 1 and page 2 for bank C.

The definition of page number is listed in Table 5.

Table 4. Page ROM selection

	BANK B			BANK C		
	B2	B1	B0	C2	C1	C0
Page 1	0	0	0	0	0	0
Page 2	0	0	1	0	0	1
Page 3	0	1	0	0	1	0
Page 4	0	1	1	0	1	1
Page 5	1	0	0	1	0	0
Page 6	1	0	1	1	0	1
Reserve	1	1	0	1	1	0
Reserve	1	1	1	1	1	1

Output Programmable Delay Register(Row16, Coln5)

7	6	5	4	3	2	1	0
X	X	X	X	X	D_2	D_1	D_0
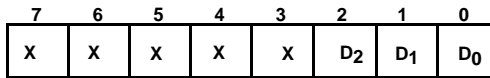
Bit 7-3 X - Don't care.

Bit 2-0 D2-D0 - These 3 bits define the propagation delay of R,G,B and FBKG outputs. When D2-D0 are all zero, there is no additional delay for outputs. Increase these 3 bits will increase the additional delay. The default setting after power on is zero.

   Figure 13 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 13 for horizontal and vertical delays: fixed delays from the leading edge of HSYNC and VSYNC signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD.

   When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of VSYNC of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame.

   Figure 14 illustrates the timing of output signals as a function of window. Line 3 of the two characters is used to illustrate the timing signals. The shaded area depicts the window area. The left hand side characters are embodied in a window.
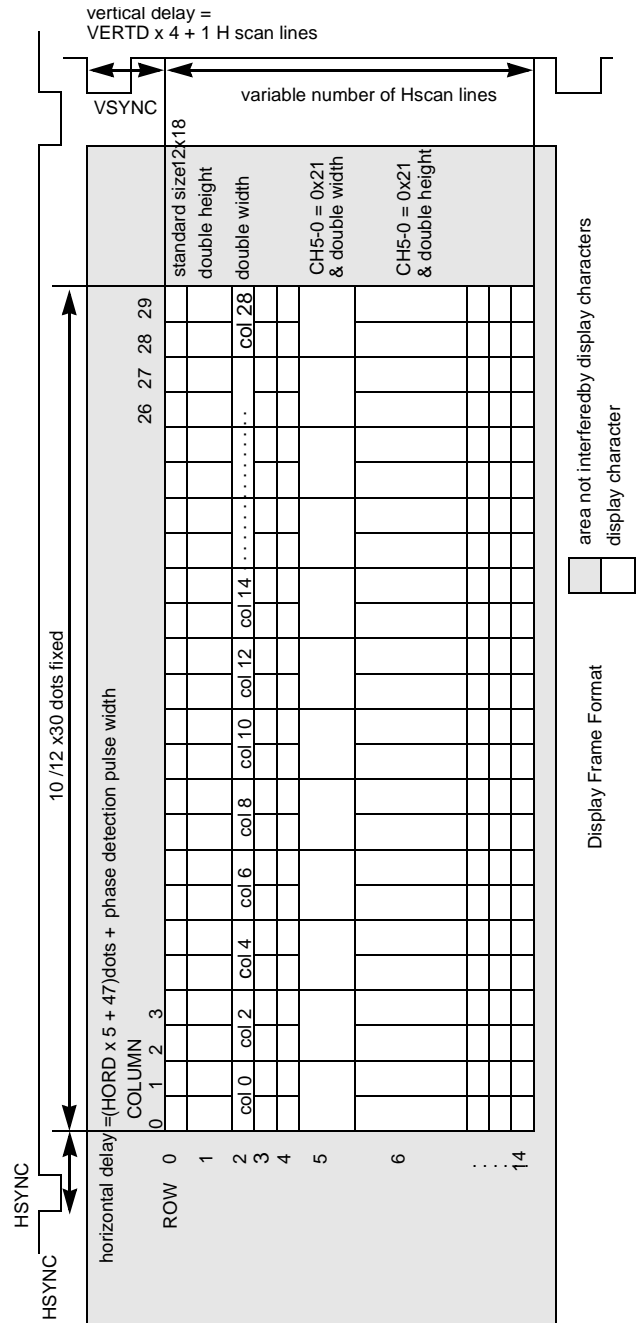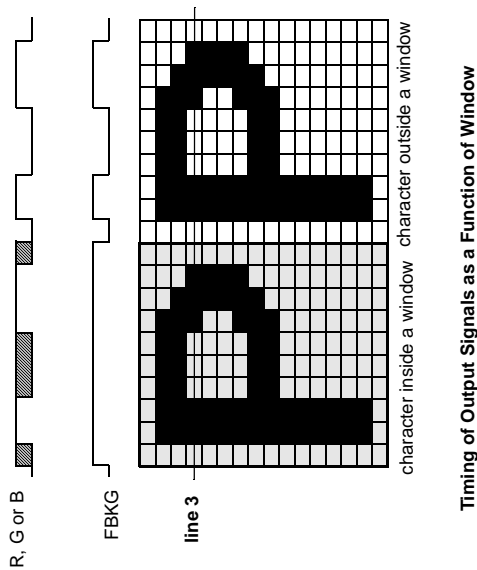

Figure 13. Display Frame Format

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 10x18 or 12x18 matrix, and let its spaces be equally located in the four sides of the matrix.
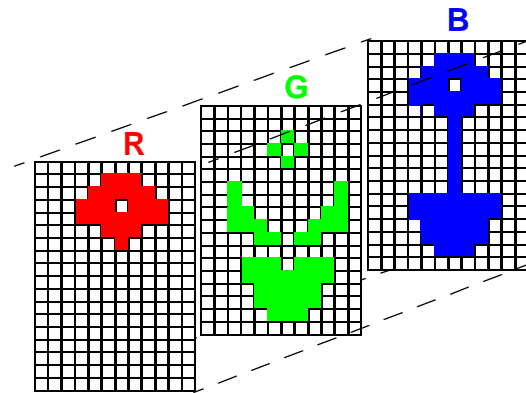
In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 10 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font

Multi-Color Font

The color font comprises three different R, G and B fonts. When the code of color font is accessed, the separate R/G/B dot pattern conbime to a multi-color font. When editing color fonts, there are 9 items for selection. They are eight colors and transparent option for selections in font editor. Please refer to following diagram.
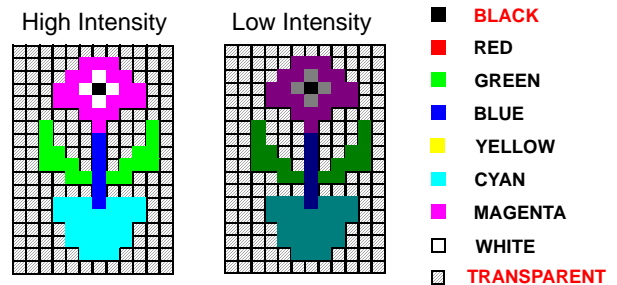
Color Font Dot Matrix

Displayed Color Font

High Intensity   Low Intensity

- ■ BLACK
- ■ RED
- ■ GREEN
- ■ BLUE
- ■ YELLOW
- ■ CYAN
- ■ MAGENTA
- □ WHITE
- ▨ TRANSPARENT

Figure 14. Timing of Output Signals

R, G or B

FBKG

line 3

character inside a window   character outside a window

Timing of Output Signals as a Function of Window

A software called MC141585 FONT EDITOR in IBM PC environment was written for MC141585 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141585. 16 Color fonts are located in addresses $01-10. The character $00 is pre-defined for blank character, the character $7F is pre-defined for full-filled character.

ROM

MC141585 contains 512 character ROM. Physical ROM includes 128-ROM Page 0 and six 64-ROM Pages(1-6). User can define these character ROM in mask ROM layer. Addressable/logical ROM includes Bank A, Bank B and Bank C. Bank A address range is $00-7F where 16 color fonts locate in $01-$10, blank in $00 and fill in $7F. It is direct mapping of Page 0. Bank B address range is $80-BF and Bank C address range is $C0-FF. Content of Bank B and Bank C are selected by Page Selection Register which determine the Page mapping, Page1 to Page 6.
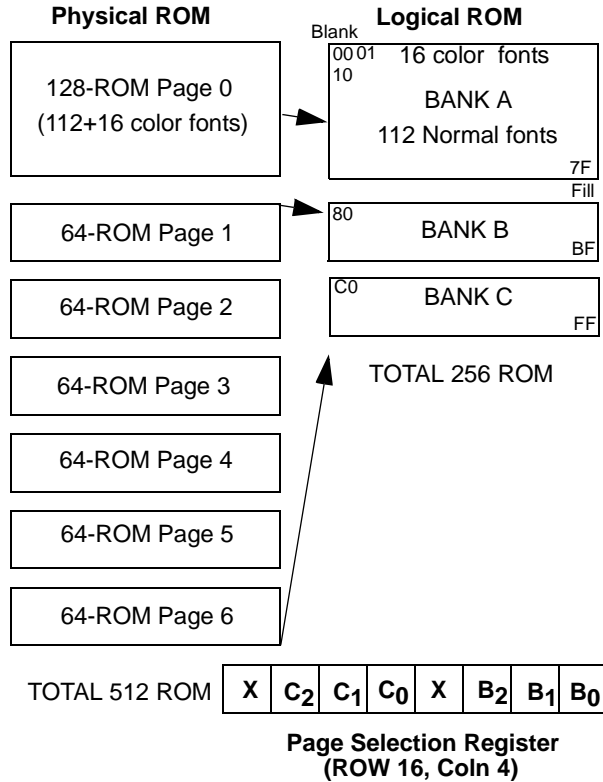

Figure 15. Character ROM Mapping

10x18 and 12x18 Font

There is no physcial difference between 10x18 and 12x18 fonts inside MC141585 character ROM. All the 512 characters are masked in 12x18 format.

But once the FSS bit in Special Register (ROW16:Coln0) is set to 1, the RGB output will change to 10x18 display format. That is, only the first 10 dots in every line of the original character will be displayed, the last two dots will be omitted.Then all characters in OSD menu will be in 10x18 display format . So do not use the two dots at right most in the 12x18 dot matrix when designing 10x18 fonts for custom mask ROM:
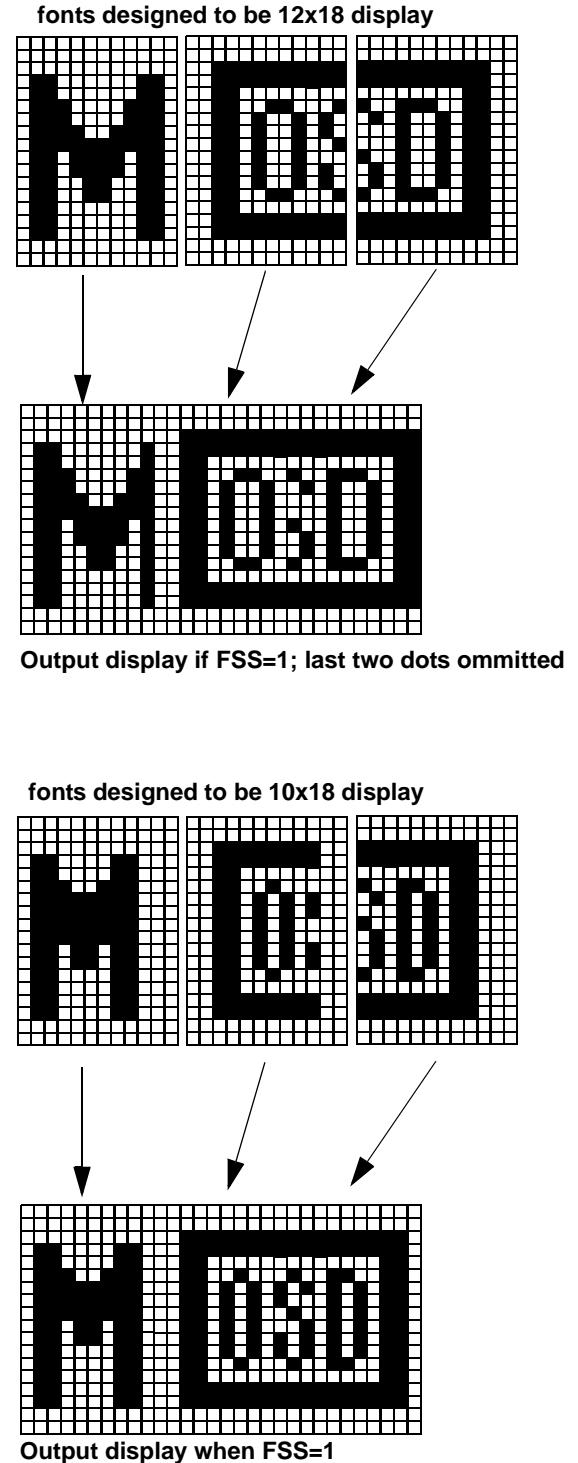
fonts designed to be 12x18 display

Output display if FSS=1; last two dots ommitted

fonts designed to be 10x18 display

Output display when FSS=1

Figure 16. 12x18 &10x18 fonts

Icon Combination

User can create On-Screen menu based on those characters and icons. Please refer to Table 6 for Icon combination. Address $00(space) & $7F(full-filled) are pre-defined characters for testing, address $01-10(H) are location of multi-color fonts.

ROM CONTENT

Figures 15 – 22 show the ROM content of MC141585. Mask ROM is optional for custom parts.

Table 5. Contents for the Page ROMS

PAGE 0 (00-7F)
Multi-color fonts
Numeric & Geometry
PAGE 1 (80-BF)
English & European(large capitcal)
PAGE 2 (C0-FF)
English & European(small capitcal)
PAGE 3 (100-13F)
Japanese
PAGE 4 (140-17F)
Japanese
PAGE 5 (180-1BF)
Korean
PAGE 6 (1CF-1FF)
Additional symbols

NOTE:The address ranges shown in above table refer to the physical address inside Mask ROM. These addresses will only be useful in designing the custom fontset using the LMOSD2 font editor. The logical addressable space for display characters will only be 00-FF after desired ROM pages for BANK B & C are selected.
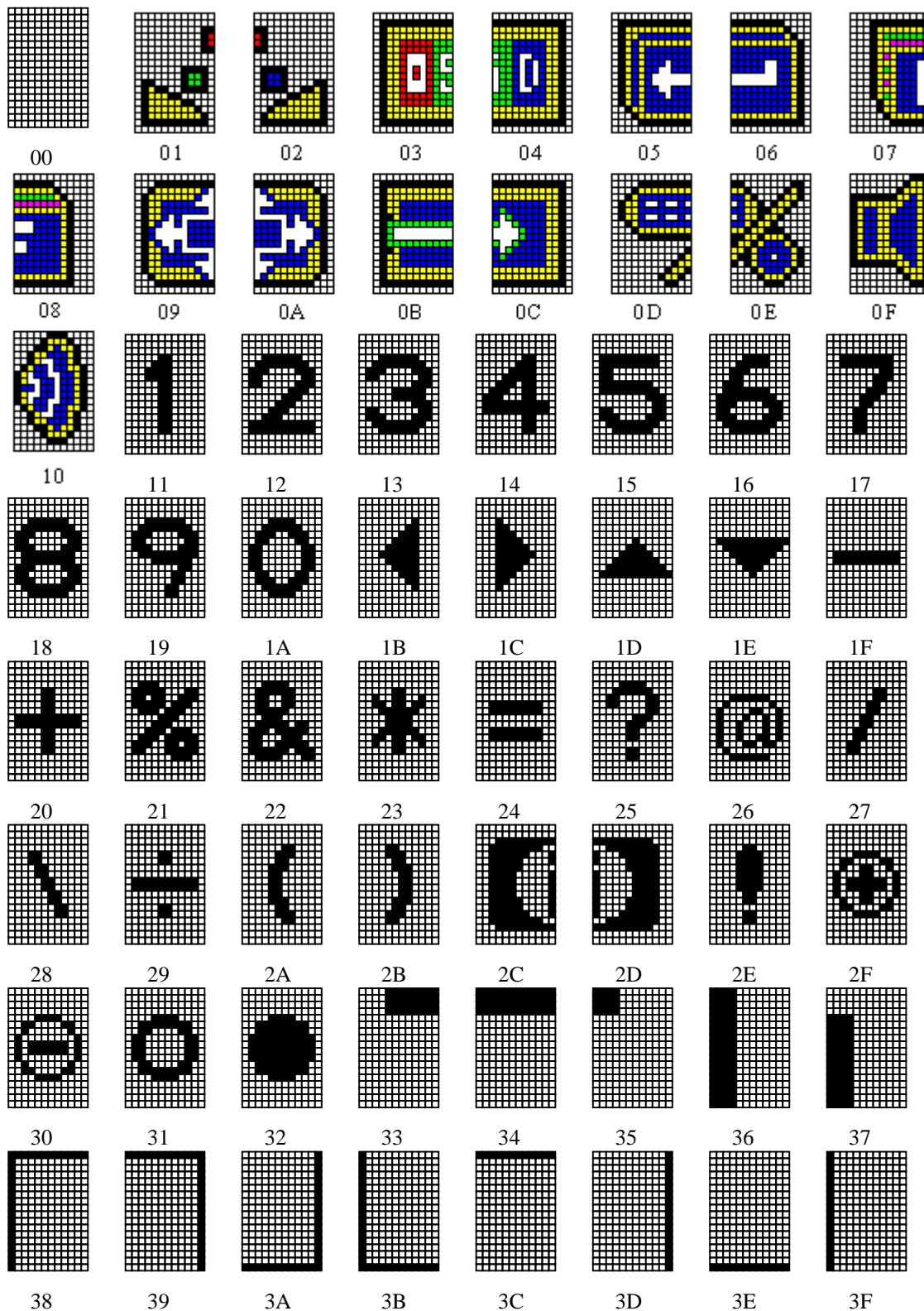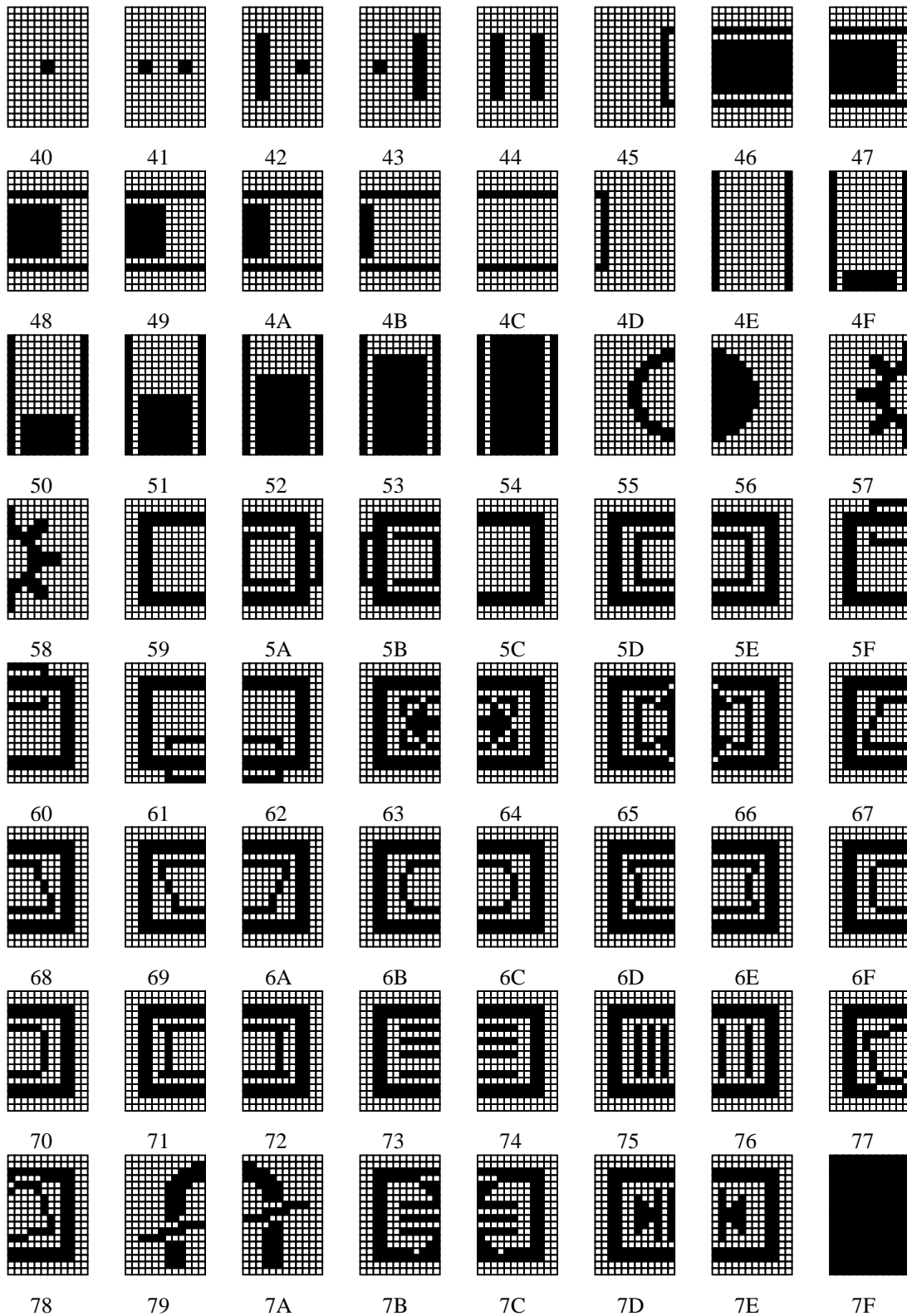
Figure 1. ROM contents for PAGE 0 ($00-$3F)

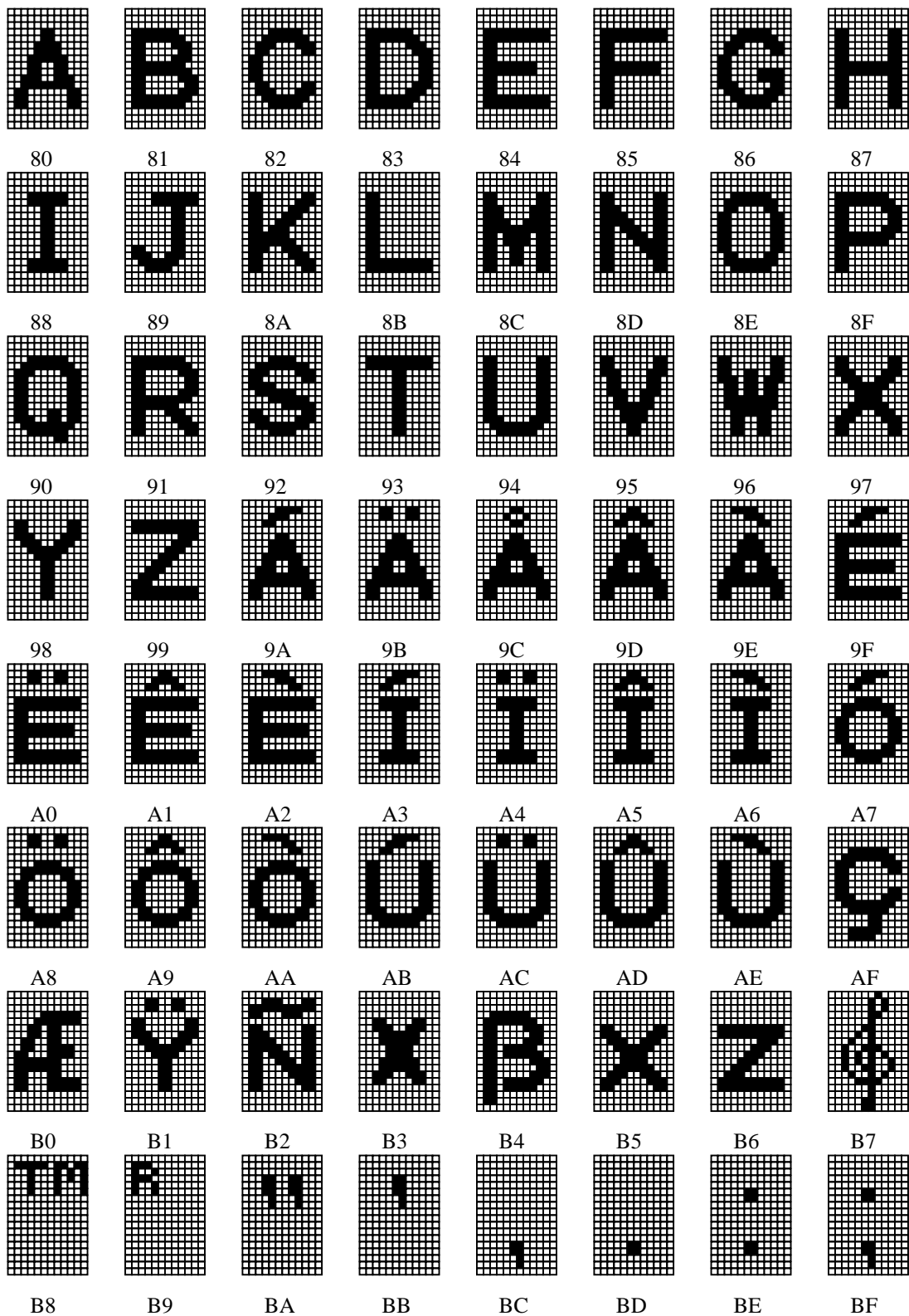**Figure 2. ROM contents for PAGE 0 ($40-$7F)**

Figure 3. ROM contents for PAGE 1

NOTE : The logical addresses shown above assumes PAGE1 is selected for BANK B. If it is selected for BANK C, each address is increased by 40(H).

a	b	c	d	e	f	g	h
C0	C1	C2	C3	C4	C5	C6	C7
i	j	k	l	m	n	o	p
C8	C9	CA	CB	CC	CD	CE	CF
q	r	s	t	u	v	w	x
D0	D1	D2	D3	D4	D5	D6	D7
y	z	â	ä	ã	å	â	é
D8	D9	DA	DB	DC	DD	DE	DF
ë	ê	è	í	ï	î	ì	ó
E0	E1	E2	E3	E4	E5	E6	E7
ö	ô	õ	ú	ü	û	ù	ç
E8	E9	EA	EB	EC	ED	EE	EF
æ	ÿ	ñ	×	ß	#	$	¥
F0	F1	F2	F3	F4	F5	F6	F7
↑	↓	←	→				
F8	F9	FA	FB	FC	FD	FE	FF

Figure 4. ROM contents for PAGE 2

**NOTE : The logical addresses shown above assumes PAGE1 is selected for BANK C. If it is
selected for BANK B, each address is decreased by 40(H).**

80	811	82	83	84	85	86	87
88	89	8A	8B	8C	8D	8E	8F
90	91	92	93	94	95	96	97
98	99	9A	9B	9C	9D	9E	9F
A0	A1	A2	A3	A4	A5	A6	A7
A8	A9	AA	AB	AC	A2	AE	AF
B0	B1	B2	B3	B4	B5	B6	B7
B8	B9	BA	BB	BC	BD	BE	BF

Figure 5. ROM contents for PAGE 3

NOTE : The logical addresses shown above assumes PAGE 3 is selected for BANK B. If it
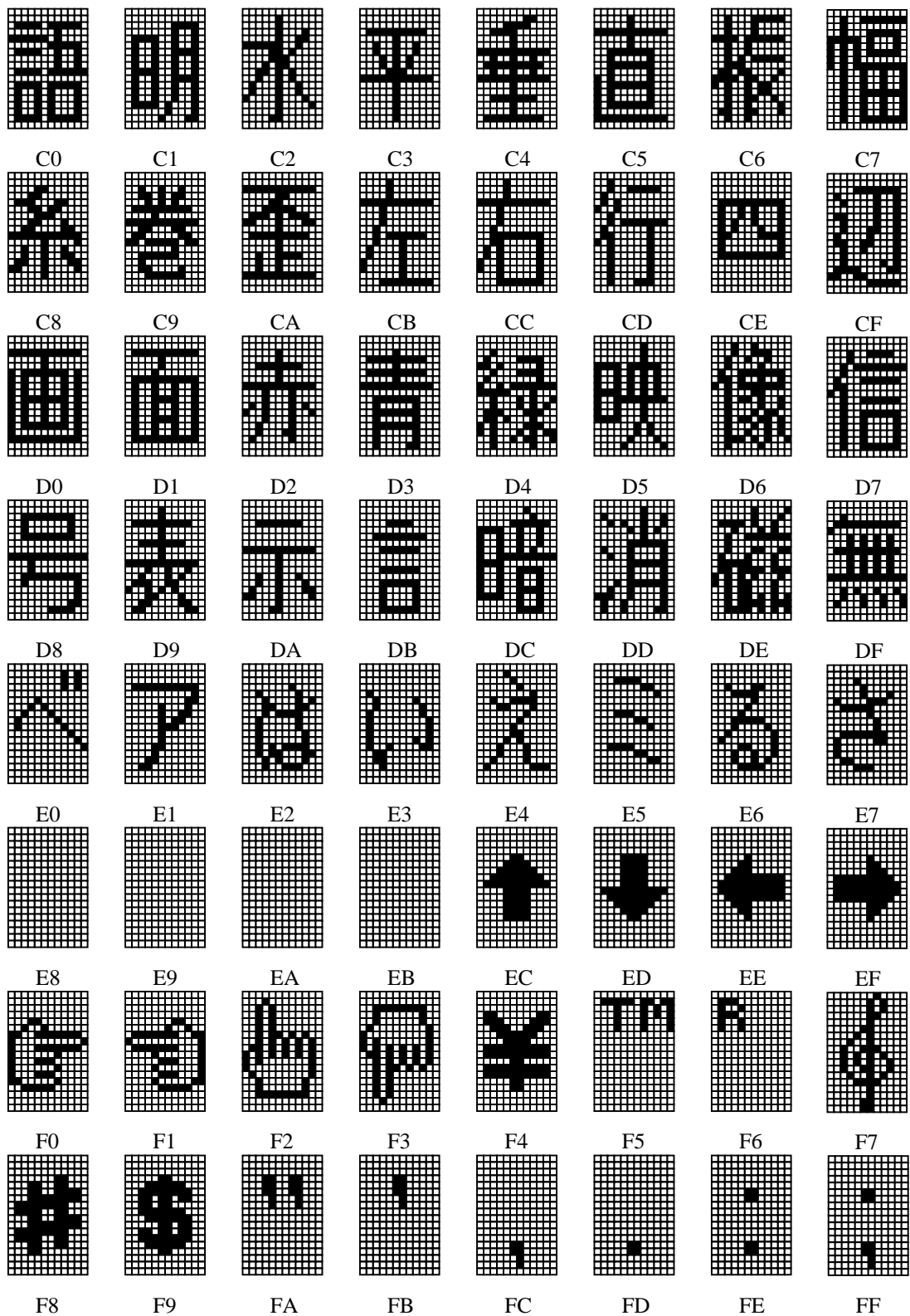**is selected for BANK C, each address is increased by 40(H).**

Figure 6. ROM contents for PAGE 4

NOTE : The logical addresses shown above assumes PAGE 4 is selected for BANK C. If it is selected for BANK B, each address is decreased by 40(H).

Figure 7. ROM contents for PAGE 5

NOTE : The logical addresses shown above assumes PAGE 5 is selected for BANK B. If it is selected for BANK C, each address is increased by 40(H).

C0 C1 C2 C3 C4 C5 C6 C7
C8 C9 CA CB CC CD CE CF
D0 D1 D2 D3 D4 D5 D6 D7
D8 D9 DA DB DC DD DE DF
E0 E1 E2 E3 E4 E5 E6 E7
E8 E9 EA EB EC ED EE EF
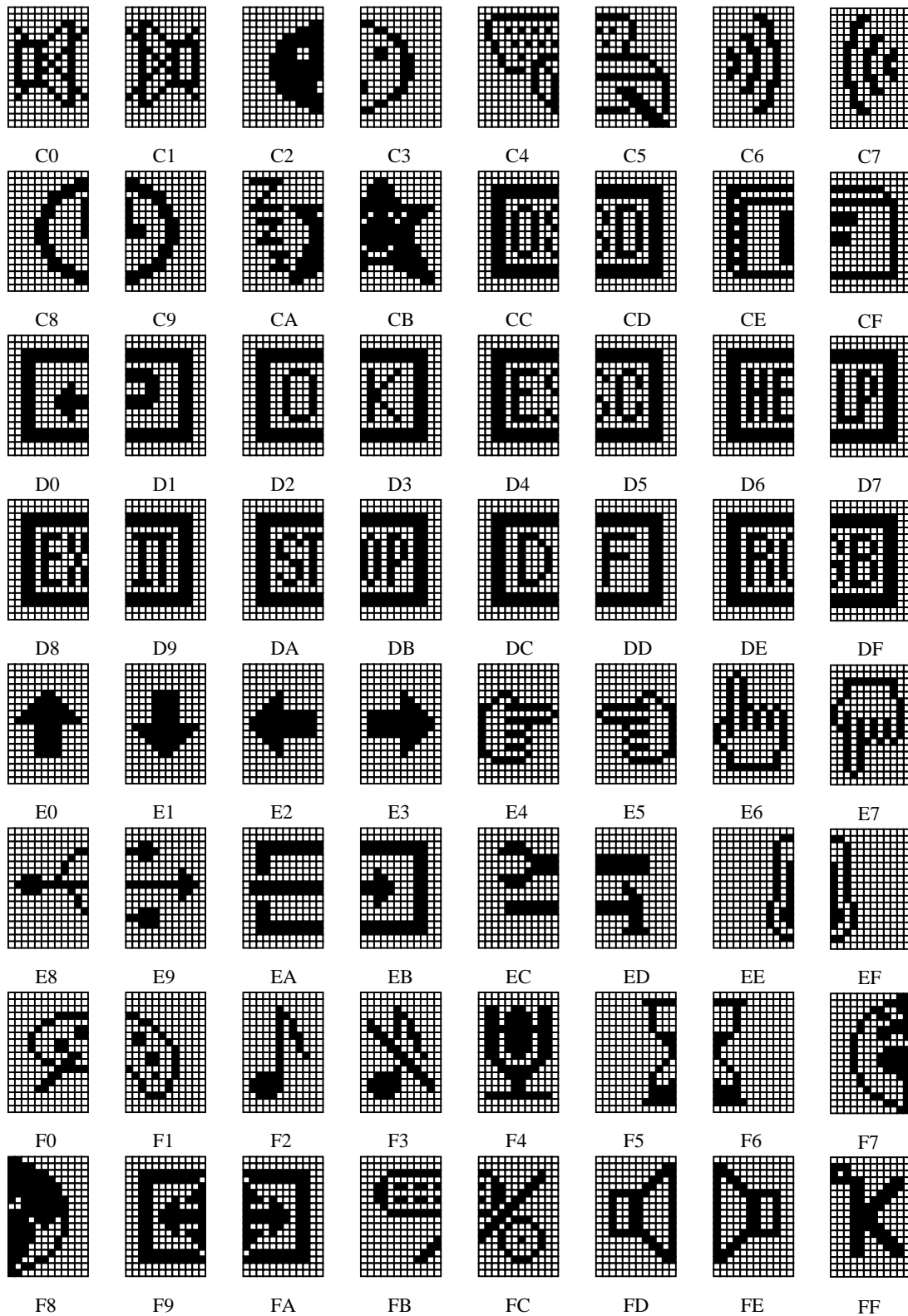F0 F1 F2 F3 F4 F5 F6 F7
F8 F9 FA FB FC FD FE FF

Figure 8. ROM contents for PAGE 6

NOTE : The logical addresses shown above assumes PAGE 6 is selected for BANK C. If it is
selected for BANK B, each address is decreased by 40(H).

APPLICATION DIAGRAM

MC141585

CMOS level RGB outputs

DC supply for low intensity output

Power on RESET

IIC BUS