

MOS FIELD EFFECT TRANSISTOR μ PA1720

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The μ PA1720 is N-Channel MOS Field Effect Transistor designed for DC / DC Converters and power management application of notebook computers.

FEATURES

· Low On-Resistance

RDS(on)1 = 25.0 m Ω MAX. (VGS = 10 V, ID = 4.0 A)

 $R_{DS(on)2} = 33.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.5 \text{ V, Ip} = 4.0 \text{ A)}$

 $R_{DS(on)3} = 38.0 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = 4.0 \text{ V, Ip} = 4.0 \text{ A)}$

- Low Ciss: Ciss = 800 pF TYP.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1720G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0)	VDSS	30	V	
Gate to Source Voltage (Vps = 0)	Vgss	±20	V	
Drain Current (DC)	$I_{D(DC)}$	±8	Α	
Drain Current (Pulse) Note1	ID(pulse)	±32	Α	
Total Power Dissipation (T _A = 25 °C) Note2	Рт	2.0	W	
Single Avalanche Current Note3	las	8.0	Α	
Single Avalanche Energy Note3	Eas	6.4	mJ	
Channel Temperature	Tch	150	°C	
Storage Temperature	Tstg	-55 to + 150	°C	

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

3. Starting Tch = 25 °C, Rg = 25 Ω , Vgs = 20 V \rightarrow 0 V

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

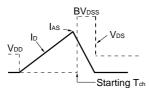


ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

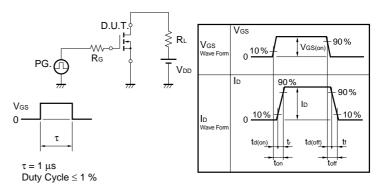
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 4.0 A		20.0	25.0	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 4.0 A		25.5	33.0	mΩ
	RDS(on)3	Vgs = 4.0 V, ID = 4.0 A		29.0	38.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 4.0 A	3.0	7.0		S
Drain Leakage Current	IDSS	Vps = 30 V, Vgs = 0 V			10	μΑ
Gate to Source Leakage Current	lgss	Vgs = ±16 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V		800		pF
Output Capacitance	Coss	V _G S = 0 V		250		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		96		pF
Turn-on Delay Time	t d(on)	ID = 4.0 A		20		ns
Rise Time	tr	VGS(on) = 10 V		80		ns
Turn-off Delay Time	td(off)	V _{DD} = 15 V		40		ns
Fall Time	tf	$R_G = 10 \Omega$		40		ns
Total Gate Charge	Q _G	ID = 8 A		14		nC
Gate to Source Charge	Qgs	V _{DD} = 24 V		2.3		nC
Gate to Drain Charge	Q _{GD}	V _G S = 10 V		3.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 8 A, VGS = 0 V		0.86		V
Reverse Recovery Time	trr	IF = 8 A, VGS = 0 V		30		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		40		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \Omega \\ \text{Vgs} = 20 \rightarrow 0 \text{V} \\ \end{array}$



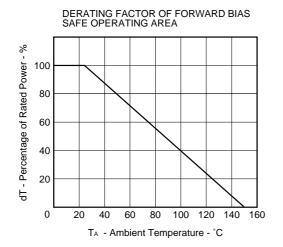
TEST CIRCUIT 2 SWITCHING TIME

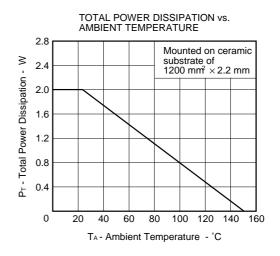


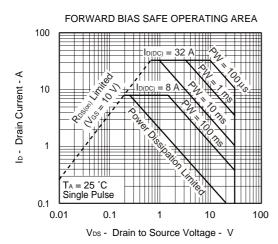
TEST CIRCUIT 3 GATE CHARGE



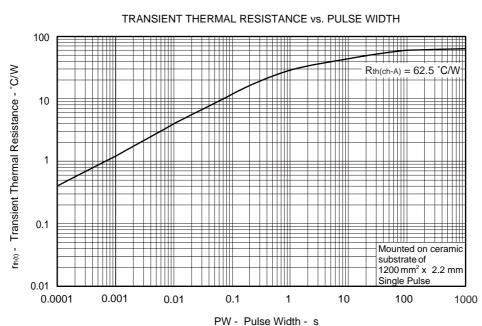
TYPICAL CHARACTERISTICS (TA = 25 °C)



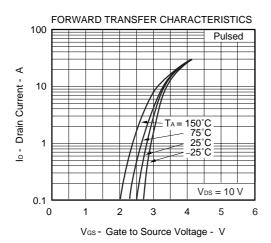


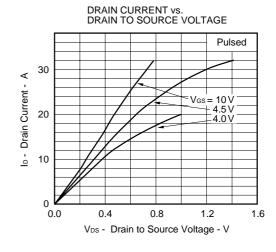


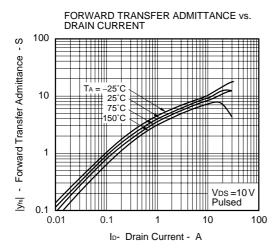
Remark Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

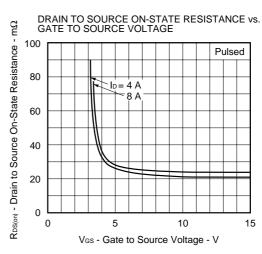


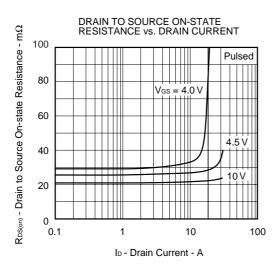
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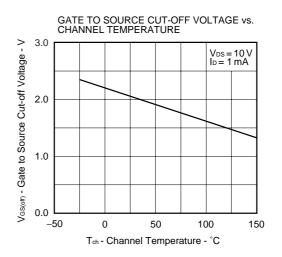


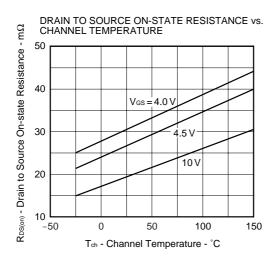


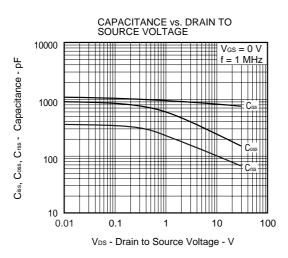


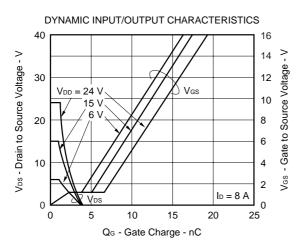


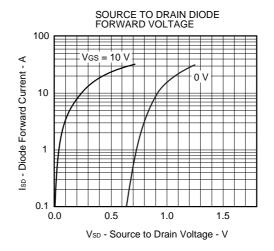


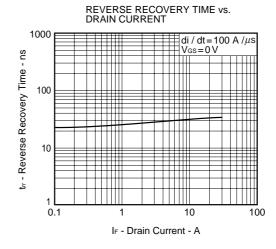




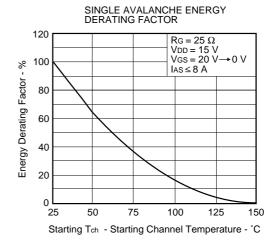








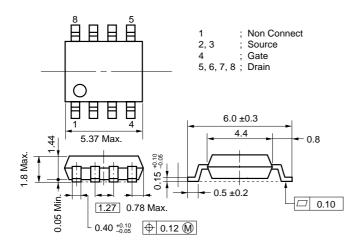
SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD 100 RG = 25 Ω VDD = 15 V VGS = 20 V \rightarrow 0 V Starting Tch = 25 °C Starting Tch = 25 °C FAST = 8 A 10 μ 10 μ 100 μ



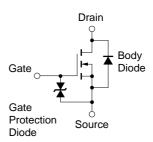


PACKAGE DRAWING (Unit: mm)

Power SOP8



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage

Exceeding the rated voltage may be applied to this device.

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