ML4802

PFC/PWM Controller Combo with Green Mode

GENERAL DESCRIPTION

The ML 4802 is a controller for power factor corrected, switched mode power supplies that offers Green Mode operation and reduced start-up and operating currents. Green Mode is an efficiency improving circuit feature which operates automatically in low power situations. This feature helps meet the demands of Energy Star™ programs.

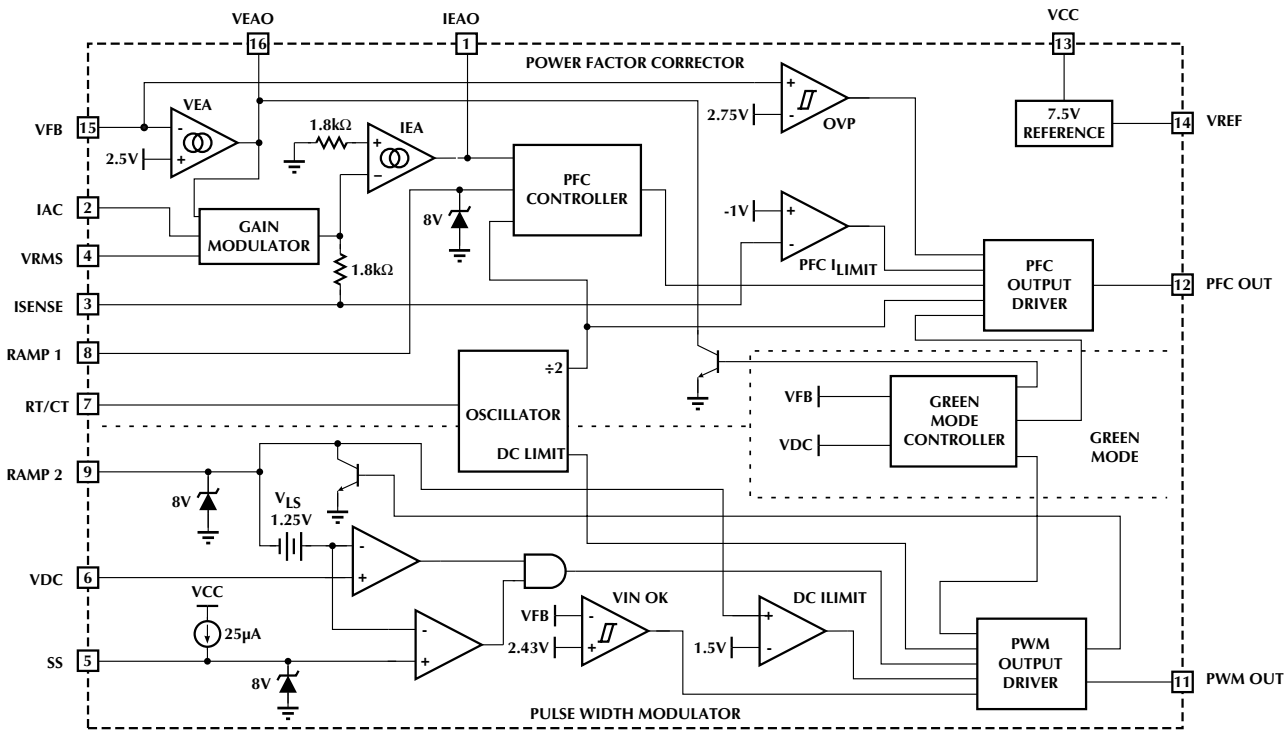
Power Factor Correction (PFC) offers the use of lower cost bulk capacitors, reduces power line loading and stress on the switching FETs. The ML4802 includes circuits for the implementation of a leading edge, average current, "boost" type power factor corrector and a trailing edge Pulse Width Modulator (PWM).

The PFC frequency of the ML4802 is automatically synchronized to be one half that of the PWM. This technique allows the user to design with smaller PWM components while maintaining the optimum operating frequency for the PFC. An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and brown-out protection.

FEATURES

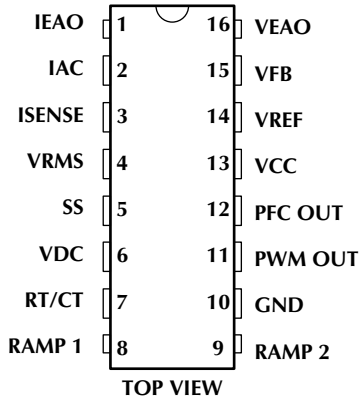
- Internally synchronized PFC and PWM in one IC
- Green Mode maximizes efficiency during low power standby operation
- Low supply current
  (Start-up 200µA typ., operating 5.5mA typ.)
- Average current continuous boost leading edge PFC
- High efficiency trailing edge PWM can be configured for current mode operation
- Reduced ripple current in the storage capacitor between the PFC and PWM sections
- PFC overvoltage comparator eliminates output "runaway" due to load removal
- Current fed gain modulator for improved noise immunity
- Overvoltage protection, UVLO, and soft start

BLOCK DIAGRAM



PIN CONFIGURATION

ML4802
16-Pin PDIP (P16)
16-Pin Narrow SOIC (S16N)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IEAO	PFC current error amplifier output
2	IAC	PFC gain control reference input
3	ISENSE	Current sense input to the PFC current limit comparator
4	VRMS	Input for PFC RMS line voltage compensation
5	SS	Connection point for the PWM soft start capacitor
6	VDC	PWM feedback voltage input
7	RT/CT	Connection for master (PWM) oscillator frequency setting components
8	RAMP 1	PFC ramp input
9	RAMP 2	PWM current feedback/overcurrent limit input
10	GND	Ground
11	PWM OUT	PWM driver output
12	PFC OUT	PFC driver output
13	VCC	Positive supply input
14	VREF	Buffered output for the internal 7.5V reference
15	VFB	PFC voltage error amplifier input
16	VEAO	PFC voltage error amplifier output

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VCC 18V
ISENSE Voltage .....–3V to 5V
Voltage on Any Other Pin .... GND – 0.3V to VCC + 0.3V
IREF 20mA
IAC Input Current 10mA
PeakCurrent, Source or Sink
PFC OUT, PWM OUT 500mA
PFC OUT, PWM OUT Energy Per Cycle 1.5µJ
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θja)
Plastic DIP ..... 80°C/W
Plastic SOIC ..... 105°C/W

OPERATING CONDITIONS

Temperature Range
ML4802CX ..... 0°C to 70°C
ML4802IX ..... –40°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCC = 15V, RT = 29.4kΩ, RRAMP1 = 15.4kΩ, CT = 270pF, CRAMP1 = 620pF, TA = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE ERROR AMPLIFIER						
	Input Voltage Range		0		5	V
	Transconductance	VNON INV = VINV, VEAO = 3.75V	20	35	50	µ℧
	Feedback Reference Voltage		2.4	2.5	2.6	V
	Input Bias Current	Note 2		-0.5	-1.0	µA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.2	0.5	V
	Source Current	ΔVIN = ±0.5V, VOUT = 6V	–1	–2.5	–4	µA
	Sink Current	ΔVIN = ±0.5V, VOUT = 1.5V	–1	–2.5	–4	µA
	Open Loop Gain		50	60		dB
	PSRR	11V < VCC < 16.5V	50	60		dB
CURRENT ERROR AMPLIFIER						
	Input Voltage Range		-1.5		2	V
	Transconductance	VNON INV = VINV, VEAO = 3.75V	50	100	150	µ℧
	Input Offset Voltage		–5	3	10	mV
	Input Bias Current			-0.5	-1.0	µA
	Output High Voltage		6.0	6.7		V
	Output Low Voltage			0.65	1.0	V
	Source Current	ΔVIN = ±0.5V, VOUT = 6V	-40	-70	-150	µA
	Sink Current	ΔVIN = ±0.5V, VOUT = 1.5V	40	70	150	µA
	Open Loop Gain		60	75		dB
	PSRR	11V < VCC < 16.5V	60	75		dB

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVP COMPARATOR						
	Threshold Voltage		2.65	2.75	2.85	V
	Hysteresis		175	250	325	mV
PFC ILIMIT COMPARATOR						
	Threshold Voltage		–0.9	–1	–1.1	V
	ΔPFC ILIMIT Threshold - Gain Modulator Output		120	220		mV
	Delay to Output			150	300	ns
DC ILIMIT COMPARATOR						
	Threshold Voltage		1.4	1.5	1.6	V
	Input Bias Current			±0.3	±1	µA
	Delay to Output			150	300	ns
VIN OK COMPARATOR						
	Threshold Voltage		2.33	2.43	2.55	V
	Hysteresis		0.8	1.0	1.2	V
GAIN MODULATOR						
	Gain (Note 3)	IAC = 100µA, VRMS = VFB = 0V	0.6	0.8	1.05	
		IAC = 50µA, VRMS = 1.2V, VFB = 0V	1.8	2	2.80	
		IAC = 50µA, VRMS = 1.8V, VFB = 0V	0.8	1	1.25	
		IAC = 100µA, VRMS = 3.3V, VFB = 0V	0.2	0.3	0.4	
	Bandwidth	IAC = 100µA		10		MHz
	Output Voltage	IAC = 250µA, VRMS = 1.15V, VFB = 0V	0.6	0.75	0.9	V
OSCILLATOR						
	Initial Accuracy	TA = 25ºC	188	200	212	kHz
	Voltage Stability	11V < VCC < 16.5V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	182		218	kHz
	Ramp Valley to Peak Voltage			2.5		V
	Dead Time	PFC Only	260	400		ns
	CT Discharge Current	VRAMP 2 = 0V, VRAMP 1 = 2.5V	3.5	5.5	7.5	mA
GREEN MODE						
VGMT-L	Green Mode Threshold Low	VGMT = VDC –VLS	70		275	mV
VGMT-H	Green Mode Threshold High	VGMT = VDC –VLS	360		580	mV
VLS	Level Shift			1.25		V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
	Output Voltage	TA = 25°C, I(VREF) = 1mA	7.4	7.5	7.6	V
	Line Regulation	11V < VCC < 16.5V		2	30	mV
	Load Regulation	1mA < I(VREF) < 10mA		2	20	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.35		7.65	V
	Long Term Stability	TJ = 125°C, 1000 Hours		5	25	mV
PFC						
	Minimum Duty Cycle	VIEAO > 4.0V			0	%
	Maximum Duty Cycle	VIEAO < 1.2V	85	90		%
	Output Low Voltage	IOUT = –20mA		0.4	0.8	V
		IOUT = –100mA		0.7	2.0	V
		IOUT = –10mA, VCC = 11V		0.8	1.5	V
	Output High Voltage	IOUT = 20mA	VCC - 0.8			V
		IOUT = 100mA	VCC - 2.0			V
	Rise/Fall Time	CL = 1000pF		50		ns
PWM						
DC	Duty Cycle Range		0-44	0-47	0-50	%
VOL	Output Low Voltage	IOUT = –20mA		0.4	0.8	V
		IOUT = –100mA		0.7	2.0	V
		IOUT = –10mA, VCC = 11V		0.8	1.5	V
VOH	Output High Voltage	IOUT = 20mA	VCC - 0. 8			V
		IOUT = 100mA	VCC - 2.0			V
	Rise/Fall Time	CL = 1000pF		50		ns
SUPPLY						
	Start-up Current	VCC = 12V, CL = 0		200	350	µA
	Operating Current	VCC = 14V, CL = 0		5	7	mA
	Undervoltage Lockout Threshold		12	13	14	V
	Undervoltage Lockout Hysteresis		2.5	2.8	3.1	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the VFB pin.

Note 3: Gain = K x 5.3V; K = (IMULO - IOFFSET) x IAC x (VEAO - 1.5V)$^{-1}$.

FUNCTIONAL DESCRIPTION

The ML4802 consists of a combined average-current-controlled, continuous boost Power Factor Corrector (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. It is distinguished from earlier combo controllers by its unique Green Mode operation and dramatically reduced start-up and operating currents. The PWM section has been optimized for use in current mode topologies. The PWM stage uses conventional trailing-edge duty cycle modulation, while the PFC uses leading-edge modulation. This patented leading/trailing edge modulation technique results in a higher useable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC bus capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the reduced ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the ML4802 runs at twice the frequency of the PFC, which allows the use of smaller PWM output magnetics and filter capacitors while holding down the losses in the PFC stage power components.

In addition to power factor correction, a number of protection features have been built into the ML4802. These include soft-start, PFC over-voltage protection, peak current limiting, brown-out protection, duty cycle limit, and under-voltage lockout.

GREEN MODE OPERATION

Green Mode automatically improves efficiency by up to 20% or more during low power operation. This feature is particularly helpful in meeting the demands of Energy Star™ programs. When the PWM's output falls to nominally 17% of its design maximum power, Green Mode operation is initiated. The upper Green Mode threshold corresponds roughly to 1/3 of rated full power level. In Green Mode, the PWM operates in a pulse-skipping mode. This significantly reduces the frequency of operation, and therefore the dissipation in the PWM output driver and switch. Since the pulse-skipping is synchronous to the PWM's master clock, the noise spectrum of the PWM retains a strong relationship to its spectrum during continuous-mode operation, which eases input and output filter design. PWM pulse frequency reductions in excess of 10:1 are common, with no increase in peak-to-peak output ripple. During Green Mode, the PFC also cycles on and off, running only as often as necessary to maintain its feedback voltage (VFB) between 2.25V and 2.5V (corresponding typical values of VBUSS are 382V and 425V). The PFC uses a built-in soft-start to minimize line current peaks and component stress when turning on. See Figure 1 for a flow chart detailing Green Mode and Normal Mode operation.

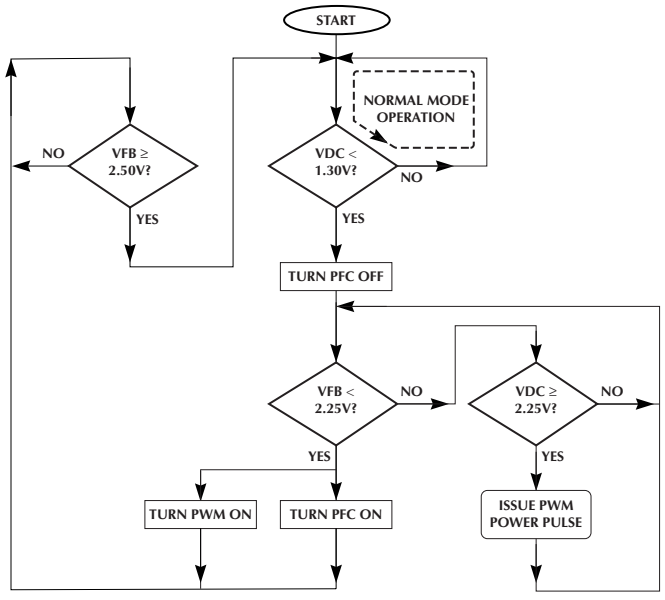


Figure 1. ML4802 Operational Flow Chart

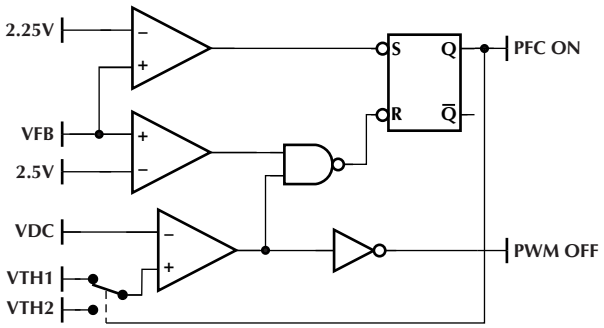


Figure 2. Green Mode Section Block Diagram

Entering Green Mode

The Green Mode Controller is detailed in Figure 2. Key to the ML4802's operation in Green-Mode is the fact that the PWM's output power is related to the voltage on the VDC (PWM Duty Cycle Control Voltage) pin by a known transfer characteristic. Therefore, the output power POUT drawn from an ML4802 supply can be inferred by monitoring the value of VDC fed back to the ML4802 from the (external) reference/error amplifier combination. When the output power taken from the PWM is reduced, the voltage on VDC will decrease. When VDC falls below VTH1 (1.30V typical), the part enters Green Mode operation. Once this happens, the threshold to which VDC is compared for further PWM operation is set to a higher value VTH2 (1.58V typical). This causes the PWM to enter a pulse-skipping mode while maintaining the desired output voltage. Pulse-skipping occurs because VTH2 is a higher voltage than VTH1, and because the PWM drive (PWMOUT) is disabled until VDC ≥ VTH2. Since the primary current of the PWM output transformer is determined by VTH2 in Green Mode, and VTH2 > VTH1, each PWM output pulse will carry slightly more energy during Green Mode operation than during all but the highest duty cycle regimes of continuous-mode operation. In Green Mode, the power in each PWM output pulse is:

$$P_{PULSE} \propto I_{PRIMARY(PWM)} \times V_{BUSS}$$

$$P_{PULSE} \propto (V_{GMT}/R_{SENSE[PWM]}) \times 380V$$

FUNCTIONAL DESCRIPTION (Continued)

On an instantaneous basis, an increase in VOUT above its programmed value will cause the error voltage presented to VDC to decrease. This will shut off PWMOUT to keep the loop in regulation. If the output voltage goes below its intended level, VDC will increase. When the feedback voltage VDC rises above VTH2, PWMOUT is re-enabled causing the output voltage to increase. This series of actions will repeat, maintaining the average VOUT at its design value. Since the PWM error amplifier gain is quite high in the average configuration, this action introduces no appreciable ripple on the PWM's DC output(s). One item to note here is that, to keep the pulse skipping action as clean as possible (that is, to prevent pulse grouping), a relatively fast error amplifier with an electrically quiet feedback path to VDC is desirable.

When the PWM enters its pulse-skipping mode, the PFC is shut off completely. The PWM then runs off of the energy stored in the PFC buss capacitor. During this period, the voltage on the buss capacitor will decay. When VBUSS falls below a user-set threshold VPFC1 (typically 382V), the PFC is turned on again, charging its output capacitor back to a higher voltage VPFC2 (typically 425V). Simultaneously, the threshold to which VDC is compared is switched back to VTH1. As soon as the output voltage of the PFC exceeds VPFC2, the PFC shuts off and VDC is again compared to VTH2. This cycle repeats as long as the power consumption from the PWM remains below the Green Mode threshold.

Exiting Green Mode

The ML4802 enters Green Mode at any time that VDC < VTH1. In order to reliably exit Green Mode, VTH1 must be used as the exit criterion as well (using VTH2 as a comparison voltage to exit Green Mode would eliminate the part's ability to skip pulses throughout the Green Mode power range). Therefore, once the voltage on VDC has set the part into Green Mode operation, the ML4802 can only exit Green Mode when the PFC is recharging the buss capacitor. As noted above, VDC is compared against VTH1 during the PFC recharge time. Another way of viewing this is as follows: every time the PFC turns on, the ML4802 exits Green Mode, and will either return to Green Mode or remain in continuous-mode operation depending upon whether the voltage on VDC exceeds VTH1. Note that this means that there will be brief periods of continuous PWM operation even while the output power drawn from the PWM is within the Green Mode range. This is a normal and harmless consequence of the ML4802's Green Mode logic.

GREEN MODE THRESHOLD

To a first approximation, the Green Mode Threshold as a percentage of the PWM's maximum rated power output is given by:

PGMT = (VGMT/VCURRENT LIMIT(PWM)) x POUT(MAX)

PGMT @ (0.25V/1.5V) = 0.167 x POUT(MAX)

For example, a flyback supply designed for 100W maximum output will nominally enter and exit Green Mode operation at 17W. Similarly, a 200W forward converter would have a Green Mode threshold of about 34W. In actual designs, the Green Mode threshold will often be at a slightly lower power level than is given by this simplified equation. This is principally due to the fact that VFB is an average-responding voltage, while POUT is inferred from the instantaneous peak current through RSENSE(PWM). On a short-term basis, the output current demand as sensed by VFB is essentially a DC level. This is not true of V(RAMP1), however: V(RAMP2) is given by (RSENSE(PWM) x IPRIMARY(PWM)), which for most designs is a combination of DC (pedestal) and peak (ramp) currents. It is the ramp current portion of IPRIMARY(PWM) which causes real-world designs to typically enter Green Mode at several percentage points lower output power than would otherwise occur.

POWER FACTOR CORRECTION

Power factor correction makes a non-linear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with, and proportional to, the line voltage, so the power factor is unity (one). A common class of non-linear load is the input of a most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect which occurs on the input filter capacitor in such a supply causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such a supply presents a power factor to the line of less than one (another way to state this is that it causes significant current harmonics to appear at its input). If the input current drawn by such a supply (or any other non-linear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with, and proportional to, the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the ML4802 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges, at twice line frequency, from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current which the converter draws from the power line matches the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. For the ML4802, a good value to use is 425V DC out, to allow for a high line of 270V AC while in Green Mode. The other condition is that the current which the converter is allowed to draw from the line at any given instant must be proportional to the line voltage. The first of these requirements is satisfied by establishing a suitable voltage

FUNCTIONAL DESCRIPTION (Continued)

control loop for the converter, which in turn drives a current error amplifier and switching output driver. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current which varies directly with the input voltage. In order to prevent ripple which will necessarily appear at the output of the boost circuit (typically about 10VAC on a 385V DC level, or about 40VAC during Green Mode operation) from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to 1/VIN2, which linearizes the transfer function of the system as the AC input voltage varies.

Since the boost converter topology in the ML4802 PFC is of the current-averaging type, no slope compensation is required.

PFC SECTION

Gain Modulator

Figure 3 shows a block diagram of the PFC section of the ML4802. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltage. There are three inputs to the gain modulator. These are:

1) A current representing the instantaneous input voltage (amplitude and waveshape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at IAC. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.

2) A voltage proportional to the long-term rms AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at VRMS. The gain modulator's output is inversely proportional to $VRMS^2$ (except at unusually low values of VRMS where special gain contouring takes over to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between VRMS and gain is designated as K, and is illustrated in the Typical Performance Characteristics.

3) The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

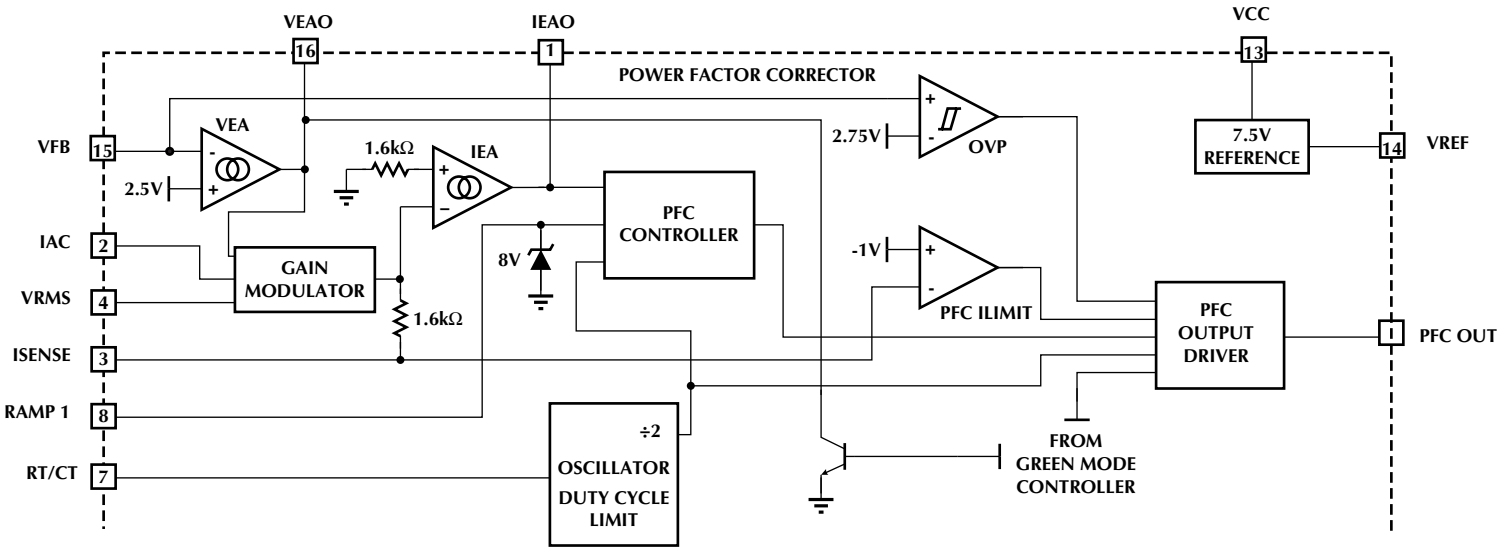


Figure 3. PFC Section Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general form for the output of the gain modulator is:

$$IGAINMOD = \frac{IAC \times VEAO}{VRMS^2} \times 1V$$

More exactly, the output current of the gain modulator is given by:

$$IGAINMOD = K \times (VEAO - 0.625V) \times IAC$$

where K is in units of V^{-1}.

Note that the output current of the gain modulator is limited to ≅ 500µA.

Current Error Amplifier

The current error amplifier's output controls the PFC duty cycle to keep the current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the ISENSE pin (current into ISENSE @ VSENSE/1.8kΩ). The negative voltage on ISENSE represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier. As stated above, the ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on ISENSE is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease to achieve a less negative voltage on the ISENSE pin.

There is a modest degree of gain contouring applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current-loop perturbations.

Cycle-By-Cycle Current Limiter

The ISENSE pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than –1.5V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

Overvoltage Protection

The OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to VFB. When the voltage on VFB exceeds 2.75V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB drops below 2.5V. The VFB should be set at a level where the active and passive external power components and the ML4802 are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 4 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to VREF to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on IEAO which prevents the PFC from immediately demanding a full duty cycle on its boost converter. This then works in conjunction with the low output current of the VEA to ensure low component stress at PFC startup.

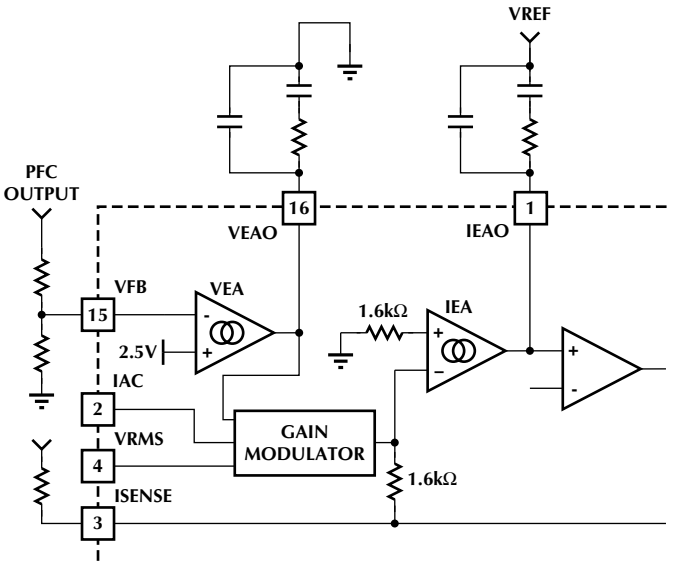


Figure 4. Compensation Network Connections for the Voltage and Current Error Amplifiers

FUNCTIONAL DESCRIPTION (Continued)

The major concern when compensating the ML4802's voltage loop error amplifier is that the current amplifier compensation is chosen to optimize frequency response while maintaining good stability. This leads to the following rules of thumb: the crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

For more information on compensating the current and voltage control loops, see Application Notes 33, 34, and 55. Application Note 16 also contains valuable information for the design of this class of PFC.

Oscillator

The oscillator frequency is determined by the values of RT and CT, which determine the ramp and off-time of the oscillator output clock:

$$fOSC = \frac{1}{tRAMP + DEADTIME}$$

The deadtime of the oscillator is derived from the following equation:

$$tRAMP = CT \times RT \times IN\left(\frac{VREF - 1.25}{VREF - 3.75}\right)$$

at VREF = 7.5V:

$$tRAMP = CT \times RT \times 0.51$$

The ramp of the oscillator may be determined using:

$$tDEADTIME = \frac{2.5V}{5.5mA} \times CT = 455 \times CT$$

The deadtime is so small (tRAMP >> tDEADTIME) that the operating frequency can typically be approximated by:

$$fOSC = \frac{1}{tRAMP}$$

EXAMPLE:
For the application circuit shown in the data sheet, with the oscillator running at:

$$fOSC = 200kHz = \frac{1}{tRAMP}$$

$$tRAMP = 0.51 \times RT \times CT = 1 \times 10^{-5}$$

Solving for RT x CT yields 1 x 10-4. Selecting standard components values, CT = 100pF, and RT = 100kΩ.

RAMP 1

The ramp voltage on this pin serves as a reference to which the PFC control signal is compared in order to set the duty cycle of the PFC switch. The external ramp voltage is derived from an RC network similar to the oscillator's. The PWM's oscillator sends a synchronous pulse every other cycle to reset this ramp.

The ramp voltage should be limited to no more than the output high voltage (6V) of the current error amplifier. The timing resistor values should be selected such that the capacitor will not charge past this point before being reset. In order to ensure the linearity of the PFC loop's transfer function and improve noise immunity, the charging resistor should be connected to the 13.5V VCC rather than the 7.5V reference. This will keep the charging voltage across the timing capacitor in the "linear" region of the charging curve.

The component value selection is similar to oscillator RC component selection.

$$fOSC = \frac{1}{tCHARGETIME + tDISCHARGETIME}$$

The charge time of RAMP 1 is derived from the following equations:

$$tCHARGE = \frac{2}{fOSC}$$

$$tCHARGE = C \times R \times 1n\left(\frac{VCC - RampValley}{VCC - RampPeak}\right)$$

At VCC = 13.5V and assuming RampPeak = 5V to allow for component tolerances:

$$tCHARGE = 0.463 \times R \times C$$

The capacitor value should remain small to keep the discharge energy and the resulting discharge current through the part small. A good value to use is the same value used in the pwm timing circuit (CT).

For the application circuit shown in Figure 7, using a 200kHz PWM and a 100pF timing capacitor yeilds RT:

$$Rt = \frac{1 \times 10^{-5}}{0.463 \times \left(100 \times 10^{-12}\right)}$$

$$Rt = 215k\Omega$$

FUNCTIONAL DESCRIPTION (Continued)

PWM SECTION

Pulse Width Modulator

The PWM section of the ML4802 is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device, from which it also derives its basic timing (at twice the PFC frequency in the ML4802). The PWM is primarily intended for current-mode operation. In current-mode applications, the PWM ramp (RAMP 2) is usually derived directly from a current sensing resistor in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DC ILIMIT, which provides cycle-by-cycle current limiting, is internally connected to RAMP 2.

No voltage error amplifier is included in the PWM stage of the ML4802, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of optocoupler feedback circuitry, an offset has been built into the PWM's RAMP 2 input which allows VDC to command a zero percent duty cycle for input voltages below 1.25V.

VIN OK Comparator

The VIN OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on VFB is less than its nominal 2.5V. Once this voltage reaches 2.5V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start commences.

PWM Control (RAMP 2)

RAMP 2 is the sampling point for a voltage representing the current in the primary of the PWM's output transformer, derived from a current sensing resistor.

PWM Current Limit

The DC ILIMIT pin is a cycle-by-cycle current limiter for the PWM section. It is connected internally to the PWM control pin. Should the input voltage at this pin ever exceed 1.5V, the output of the PWM will be disabled until the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle.

Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of 25µA supplies the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start-up delay can be programmed by the following equation:

$$CSS = tDELAY \times \frac{25\mu A}{1.25V}$$

where CSS is the required soft start capacitance, and tDELAY is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of CSS:

$$CSS = 5ms \times \frac{25\mu A}{1.25V} \cong 200nF$$

Generating VCC

The ML4802 is a voltage-fed part. It requires an external 15V±10% (or better) Zener shunt voltage regulator, or other controlled supply, to maintain the voltage supplied to the part at 15V nominal. This allows a low power dissipation while at the same time delivering 13V nominal of gate drive at the PWM OUT and PFC OUT outputs.

LEADING/TRAILING MODULATION

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output voltage is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON of the switch. Figure 5 shows a typical trailing edge control scheme.

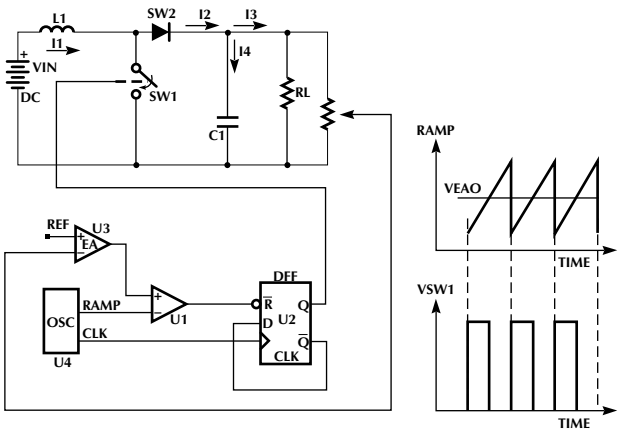


Figure 5. Typical Trailing Edge Control Scheme

FUNCTIONAL DESCRIPTION (Continued)

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 6 shows a leading edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1 (SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

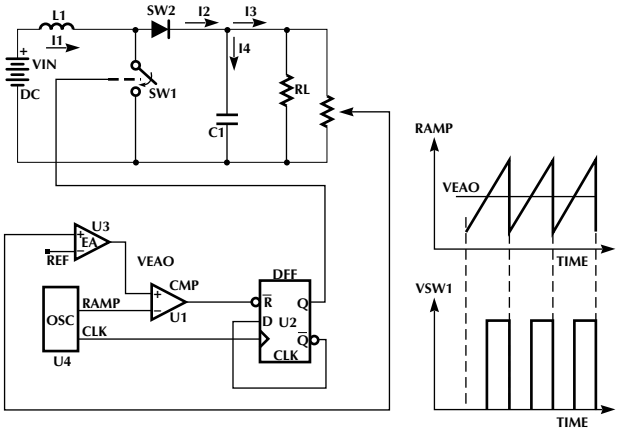


Figure 6. Leading/Trailing Edge Control Scheme

TYPICAL APPLICATIONS

Figure 7 is the application circuit for a complete 100W power factor corrected power supply, designed using the methods and general topology detailed in Application Note 33.

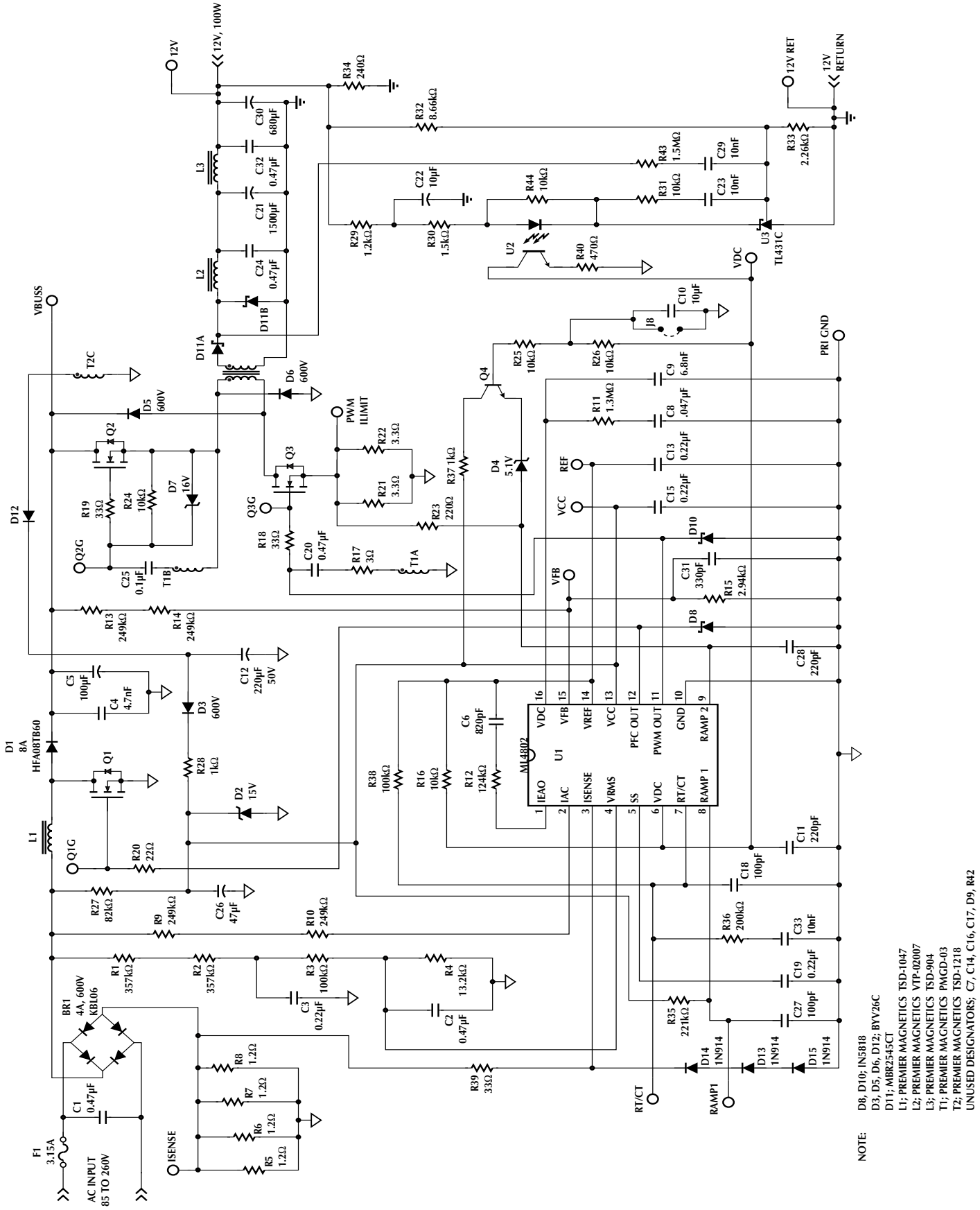
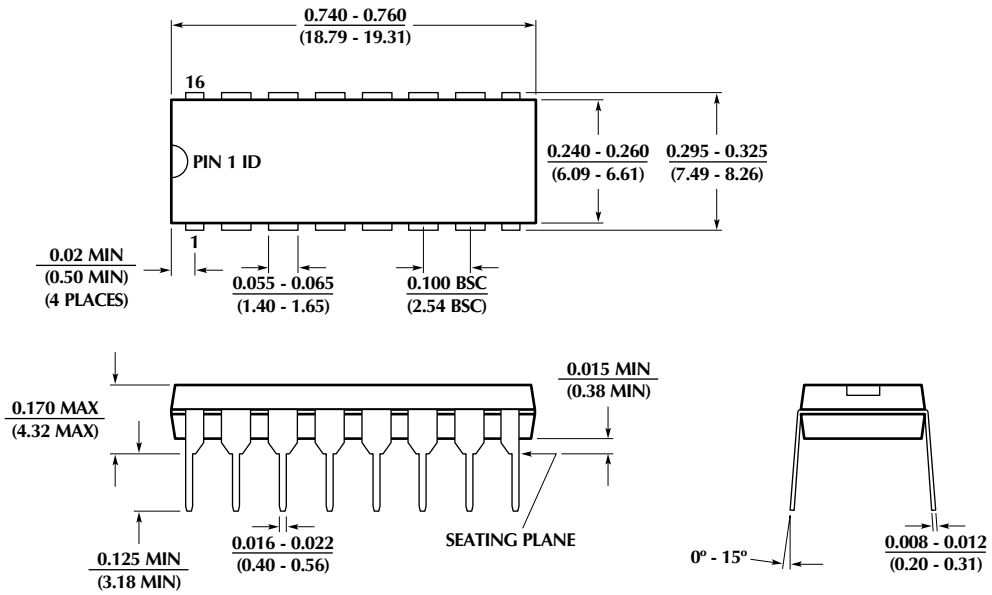


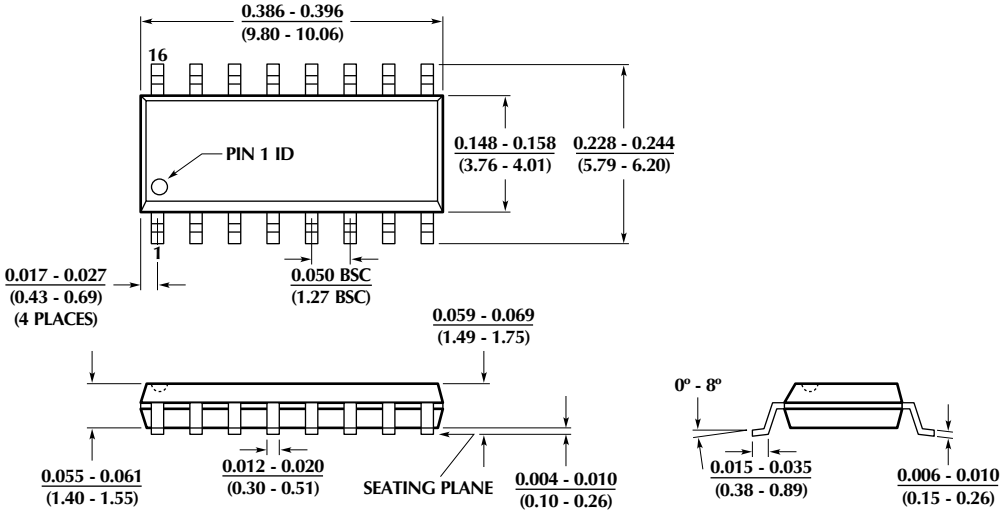
Figure 7. 100W Power Factor Corrected Power Supply

PHYSICAL DIMENSIONS inches (millimeters)

Package: P16
16-Pin PDIP



Package: S16N
16-Pin Narrow SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4802CP ML4802CS	0°C to 70°C 0°C to 70°C	16-Pin Plastic DIP (P16) 16-Pin Narrow SOIC (S16N)
ML4802IP ML4802IS	-40°C to 85°C -40°C to 85°C	16-Pin Plastic DIP (P16) 16-Pin Narrow SOIC (S16N)

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