8-Bit Synchronous Binary Up Counter

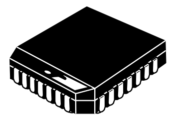
MC10E016
MC100E016

8-BIT SYNCHRONOUS BINARY UP COUNTER

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10H family, extended to 8-bits, as shown in the logic symbol.

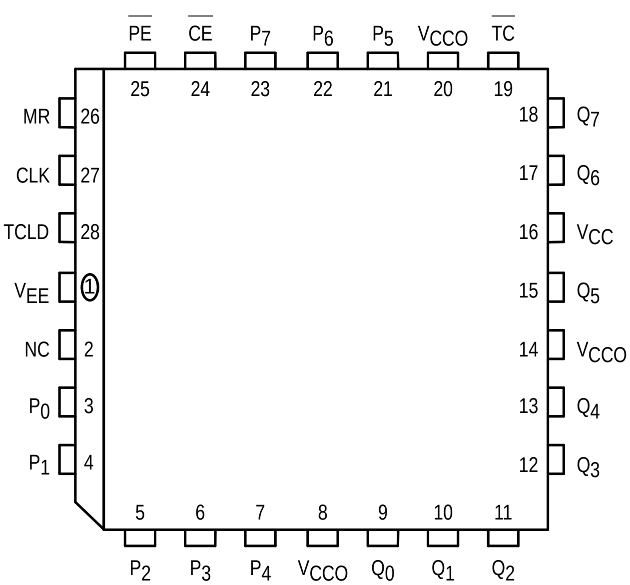
The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the TC feedback is disabled, and counting proceeds continuously, with TC going LOW to indicate an all-one state. When TCLD is HIGH, the TC feedback causes the counter to automatically reload upon TC = LOW, thus functioning as a programmable counter. The Q_n outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

- 700MHz Min. Count Frequency
- 1000ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

FUNCTION TABLE

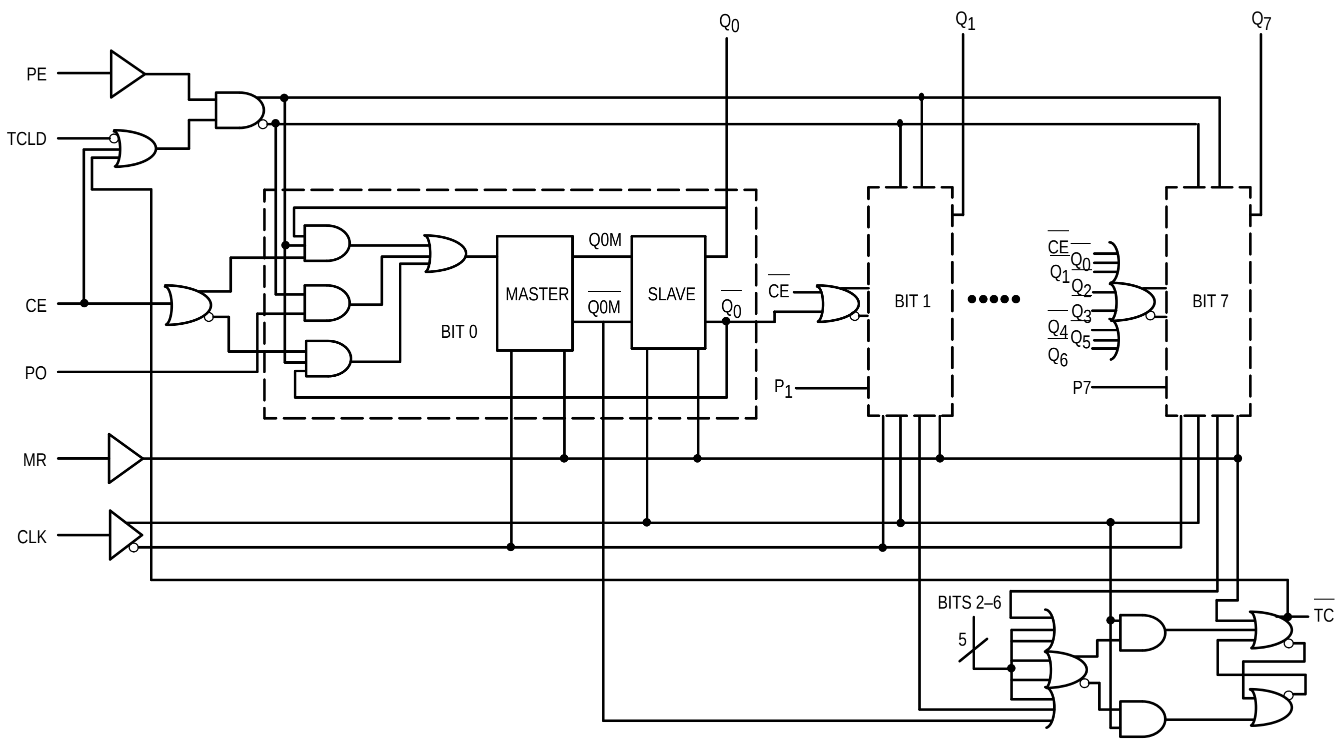
CE	PE	TCLD	MR	CLK	Function
X	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Q_n : = LOW, TC : = HIGH)

Z = clock pulse (low to high);
ZZ = clock pulse (high to low)

PIN NAMES

Pin	Function
P0 – P_7	Parallel Data (Preset) Inputs
Q_0 – Q_7	Data Outputs
$\overline{CE}$	Count Enable Control Input
PE	Parallel Load Enable Control Input
MR	Master Reset
$\overline{CLK}$	Clock
TC	Terminal Count Output
TCLD	TC-Load Control Input

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		151	181		151	181		151	181		
	100E		151	181		151	181		174	208		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
f_{COUNT}	Max. Count Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to Q	600	725	1000	600	725	1000	600	725	1000		
	MR to Q	600	775	1000	600	775	1000	600	775	1000		
	CLK to $\overline{TC}$	550	775	900	550	775	900	550	775	1050		
	MR to TC	625	775	1000	625	775	1000	625	775	1000		
t_s	Setup Time										ps	
	Pn	150	– 30		150	– 30		150	– 30			
	$\overline{CE}$	600	400		600	400		600	400			
	PE	600	400		600	400		600	400			
	TCLD	500	300		500	300		500	300			
t_h	Hold Time											
	Pn	350	100		350	100		350	100			
	$\overline{CE}$	0	– 400		0	– 400		0	– 400			
	PE	0	– 400		0	– 400		0	– 400			
	TCLD	100	– 300		100	– 300		100	– 300			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_r t_f	Rise/Fall Times										ps	
	20 - 80%	300	510	800	300	510	800	300	510			

FUNCTION TABLE

Function	PE	CE	MR	TCLD	CLK	P7-P4	P3	P2	P1	P0	Q7-Q4	Q3	Q2	Q1	Q0	TC
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

Applications Information

Cascading Multiple E016 Devices

For applications which call for larger than 8-bit counters multiple E016s can be tied together to achieve very wide bit width counters. The active low terminal count (TC) output and count enable input (CE) greatly facilitate the cascading of E016 devices. Two E016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 1 below pictorially illustrates the cascading of 4 E016s to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an E016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the TC output and the necessary setup time of the CE input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the TC propagation delay and the CE setup time). Figure 1 shows EL01 gates used to control the count enable inputs, however, if the frequency of operation is lower a slower, ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is 500MHz and that for a 16-bit counter is 625MHz.

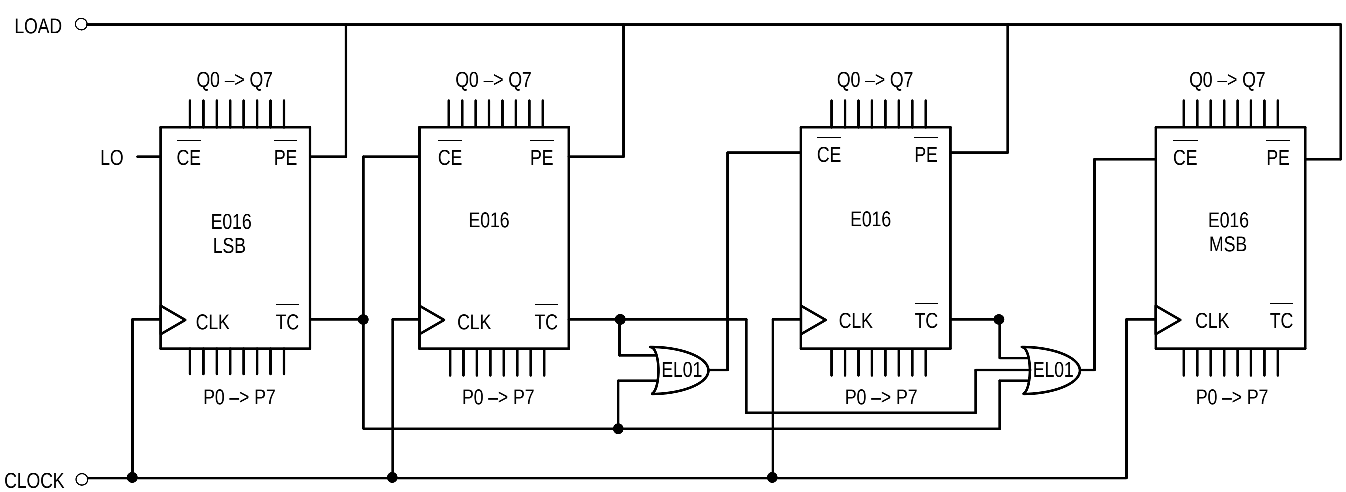


Figure 1. 32-Bit Cascaded E016 Counter

Applications Information (continued)

Note that this assumes the trace delay between the $\overline{TC}$ outputs and the CE inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn’s) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 2 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

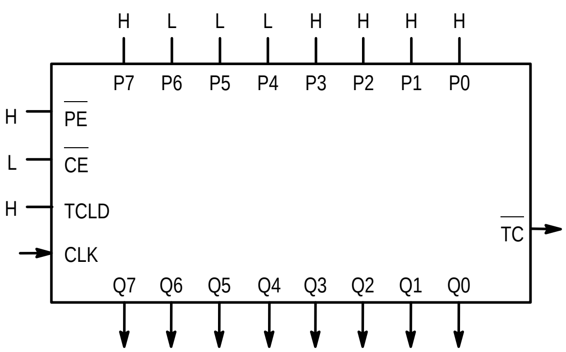


Figure 2. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn’s = 256 – 113 = $8F_{16}$ = 1000 1111

where:
P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 2 will result in the waveforms of Figure 3. Note that the TC output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the E016 and the TC output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 1. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single E016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the TC pins must be used for multiple E016 divider chains.

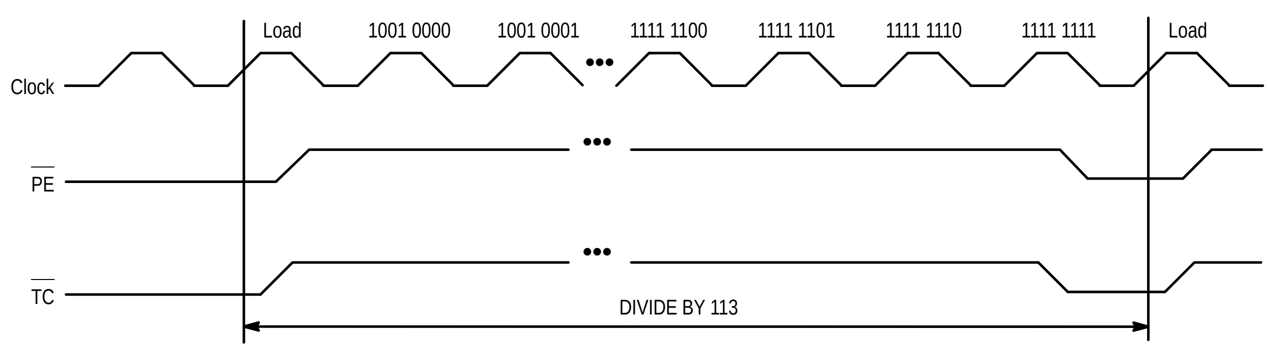


Figure 3. Divide by 113 E016 Programmable Divider Waveforms

Applications Information (continued)

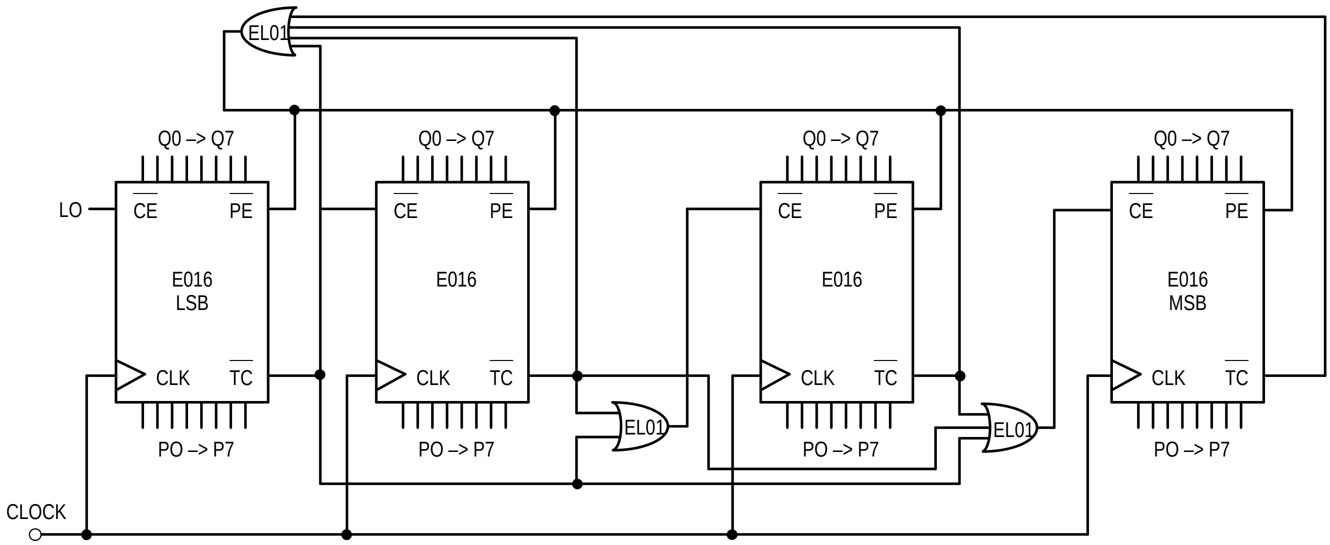


Figure 4. 32-Bit Cascaded E016 Programmable Divider

Figure 4 on the following page shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EL01 OR gates were used. For lower frequency applications a slower OR gate could replace the EL01. Note that for a 16-bit divider the OR function feeding the PE (program enable) input CANNOT be replaced by a wire OR tie as the TC output of the least significant E016 must also feed the CE input of the most significant E016. If the two TC outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the PE feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Maximizing E016 Count Frequency

The E016 device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

OUTLINE DIMENSIONS

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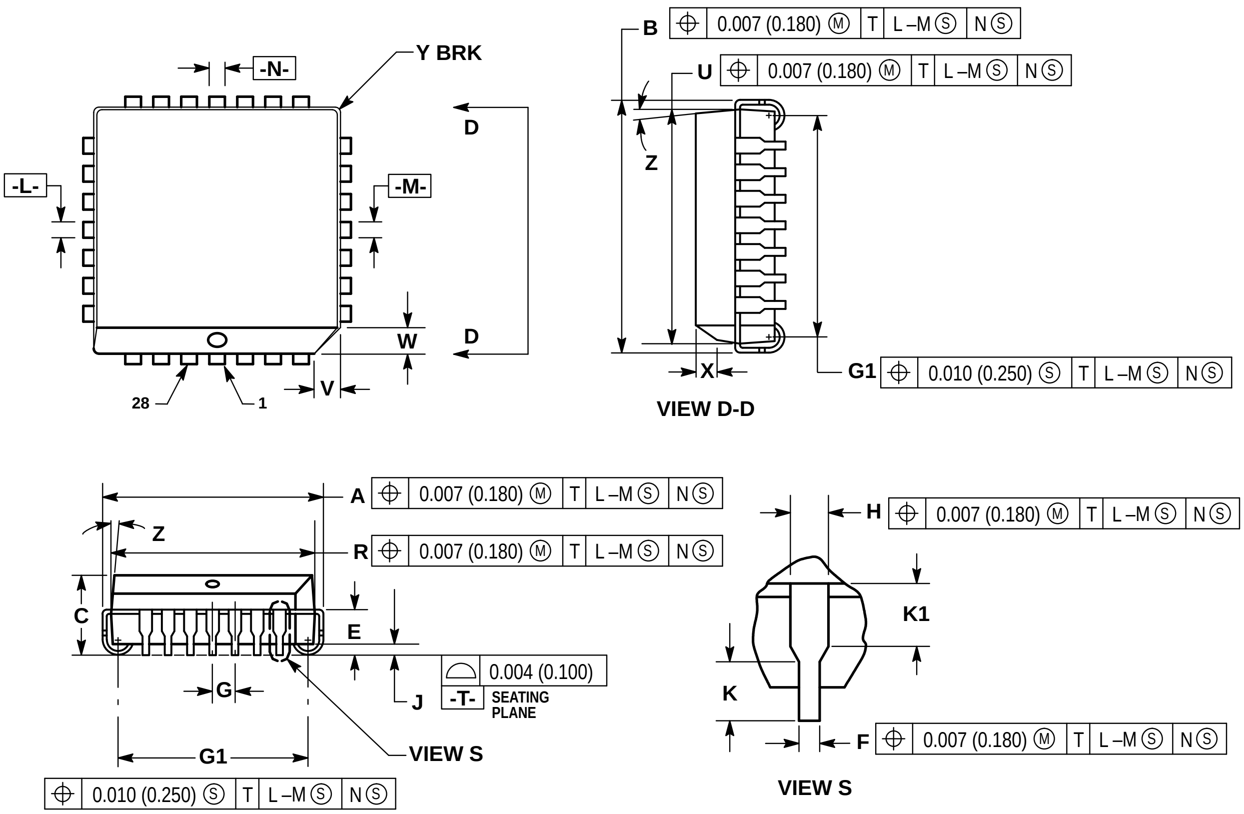
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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