HEWLETT® PACKARD

2.0 Amp IGBT Gate Drive Optocoupler with Integrated Over-current Protection and Fault Feedback

Preliminary Technical Data

HCPL-3160

Features

- **Integrated IGBT Desaturation Protection**
- **Integrated Optically Isolated IGBT Fault Status Feedback**
- **CMOS Compatible INPUT and FAULT Status Indicator**

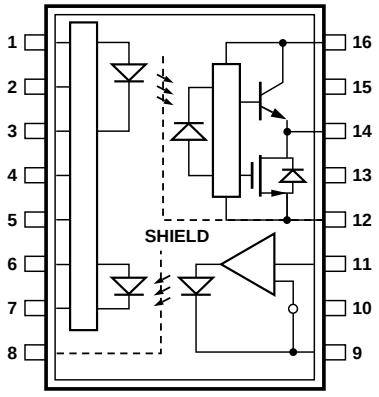
Actual Size

- **Small Printed Circuit Board Footprint (SO-16 Package)**
- **-40℃ to 100℃ Operating Temperature**
- **Suitable for Integration in Power Modules**
- **2.0 A Minimum Peak Output Current**
- **15 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V**
- **V_{IORM} = 890 V_{PEAK}**

Description

The HCPL-3160 provides low cost, area efficient IGBT gate drive that includes desaturation or over current detection and local IGBT shutdown. The integrated fault feedback optocoupler notifies the controller when the IGBT is shutdown due to a desaturation or over current condition.

Functional Diagram



This data sheet represents the latest information at the time of publication of this catalog. All specifications subject to change. Samples available Fall 1996.

Fault Circuit Operation

A typical desaturation protected IGBT gate drive application circuit using the HCPL-3160 is shown in Figure 1. The IGBT collector to emitter voltage is monitored through D_{DESAT}. When the IGPT is *on* and V_{DESAT} exceeds the internal reference voltage of 7 V the IGBT gate is "softly" turned-off by M2 to prevent large di/dt generation. The LED2 driver is also activated, which drives the internal feedback LED2 and notifies the controller of the IGBT fault by bringing the FAULT output low. The FAULT output remains low until RESET is brought low. (Note if a separate reset line is not required, RESET can be connected to Vin on the circuit board. In this case, the FAULT output will be reset on the next PWM cycle that Vin goes low.) The FAULT output is an open collector which allows the FAULT outputs from all the HCPL-3160s in a drive to be connected together in a "wired OR" forming a single fault bus for interfacing with the micro-controller. The ENABLE input can also be connected to this fault bus. With this connection all IGBTs in a drive are shutdown without micro-controller intervention once a fault is detected on a single IGBT.

C_{BLANK} disables the fault detection circuitry for a time period sufficient for normal IGBT turn-on. C_{BLANK} is held low by Q1 when the IGBT is off.

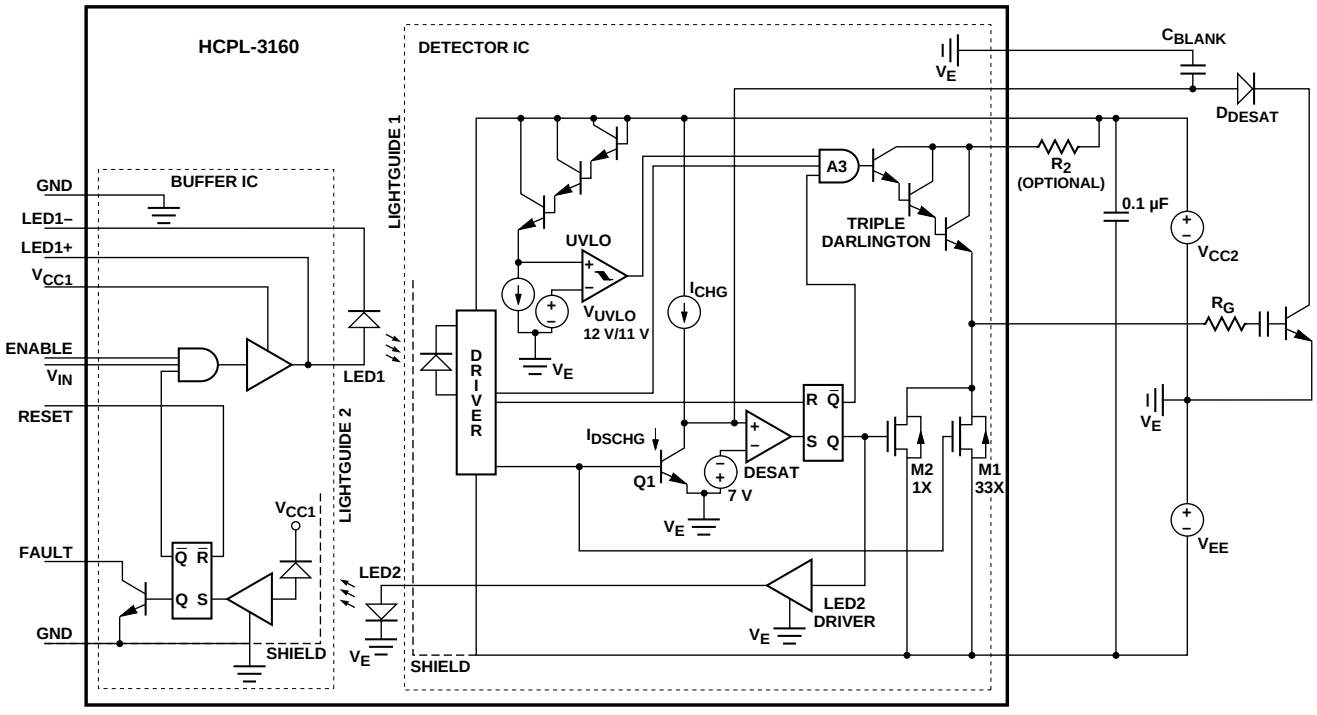


Figure 1. IGBT Gate Drive with Desaturation Protection and Fault Feedback.

Preliminary Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 to 100°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions
Logic Low Voltages	INPUT RESET FAULT ENABLE			0.8	V	
Logic High Voltages	INPUT RESET FAULT ENABLE	2.0			V	
High Level Output Current	I_{OH}	0.5	1.5		A	$V_O = V_{CC2}$ -4 V
		2.0			A	$V_O = V_{CC2}$ 15 V
Low Level Output Current	I_{OL}	0.5	2.0		A	$V_O = V_{EE}$ + 2.5 V
		2.0			A	$V_O = V_{EE}$ + 15
High Level Output Voltage	V_{OH}	V_{CC2}-4	V_{CC2}-3		V	I_O = -100 mA
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA
High Level Supply Current	I_{CC1H}			12	mA	Vin = 5 V, V_{CC1} = 5 V
High Level Supply Current	I_{CC1L}			2	mA	Vin = 0 V, V_{CC1} = 5 V
High Level Supply Current	I_{CC2H}		3	7	mA	output open
Low Level Supply Current	I_{CC2L}		3	7	mA	output open
Blanking Capacitor Charging Current	I_{CHG}	0.2	0.32	0.45	mA	Vdesat = 0 V
Blanking Capacitor Discharge Current	I_{DSCHG}		60		mA	Vdesat = 7 V
UVLO Threshold	V_{UVLO+}		13.0 (10.9)	13.4 (12.5)	V	V_{CC2} = 1.0 ms ramp, V_O > 5 V
	V_{UVLO-}	11.2 (8.7)	11.6 (9.5)		V	V_{CC2} = 1.0 ms ramp, V_O > 5 V
UVLO Hysteresis	V_{UVLO+} - V_{UVLO-}		1.4		V	
Desaturation Trip Voltage	V_{DESAT}	6.0	7.0	8.0	V	

*All typical values at T_A = 25°C and V_{CC2} - V_{EE} = 30 V, unless otherwise noted.

[1)] V_{UVLO+} and V_{UVLO-} are specified as the V_{CC2} at which V_O exceeds 5 V. The approximate output voltage just prior/after the UVLO transition is given in parenthesis.

Preliminary Switching Specifications (AC)

Over recommended operating conditions (T_A = -40 to 100°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%
Propagation Delay Time to Low Output Level	t_{PHL}	0.10		0.50	µs	
Pulse Width Distortion	pwd	-0.1		0.1	µs	
Propagation Delay Difference Between Any Two Parts	t_{PHL} - t_{PLH}	-0.4		0.4	µs	
Rise Time	t_r		0.1		µs	
Fall Time	t_f		0.1		µs	
Propagation Delay Time from Desat to Low Level Output	$t_{P(DS)}$			1.5	µs	Rg = 10 Ω, CG = 10 nF
Propagation Delay Time from Desat to Low Level FAULT Signal	$t_{PF(DS)}$			10	µs	RG = 10 Ω, CG = 10 nF
Minimum FAULT Signal Pulse Width	Δt_{FAULT}		2.0		µs	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6		µs	
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, INPUT = 5 V, V_{CM} = 1500 V, V_{CC} = 30 V
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, INPUT = 0 V, V_{CC2} = 30 V

*All typical values at T_A = 25°C and V_{CC2} - V_{EE} = 30 V, unless otherwise noted.