MICRF007

QwikRadio™ Low-Power UHF Receiver

Preliminary Information

General Description

The MICRF007 is a single chip ASK/OOK (ON-OFF Keyed) Receiver IC for remote wireless applications, employing Micrel's latest QwikRadio[tm] technology. This device is a true "antenna-in to data-out" monolithic device. All RF and IF tuning is accomplished automatically within the IC which eliminates manual tuning, and reduces production costs. The result is a highly reliable yet extremely low cost solution. The MICRF007 is an enhanced version of the MICRF002 and MICRF011.

The MICRF007 is a conventional superhetrodyne receiver, with an (internal) Local oscillator fixed at a single frequency based on an external reference crystal or clock. As with any conventional superhetrodyne reciever, the *transmit* frequency must be accurately controlled, generally with a crystal or SAW (Surface Acoustic Wave) resonator.

The MICRF007 provides two feature enhancements over the MICRF001/011, (1) a Shutdown Mode, which may be used for duty-cycle operation. (2) Reduced current consumption. The MICRF007 requires a mere 1.7mA at 315MHz (3.0mA at 433.92MHz).These features make the MICRF007 ideal for low and ultra-low power applications, such as RKE and RFID.

All post-detection (demodulator) data filtering is provided on the MICRF007, so no external baseband filters are required. The demodulator filter bandwidth is set to 2.1kHz. Data rates up to 2kbps may be used

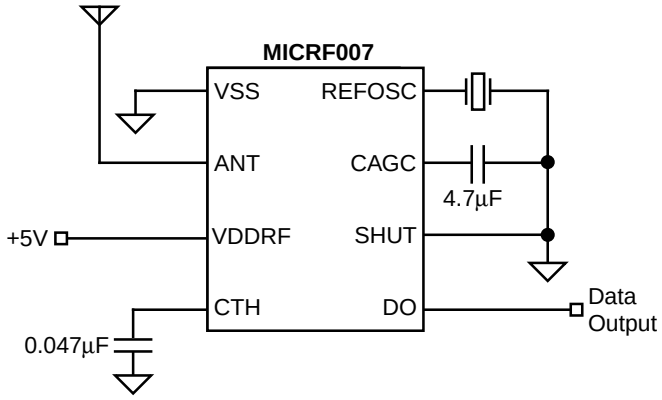
Features

- Complete UHF receiver on a monolithic chip
- 300MHz
- Data Rates up to 2.1kbps
- Automatic tuning, no manual adjustment
- Low Power Consumption
  - 315MHz:
  - 1.7 mA fully operational
  - 0.5µA shutdown
  - 170µA polled
  - 433.92MHz:
  - 3.0mA fully operational
  - 0.5µA shutdown
  - 300µA in 10:1 polled operation
- Very low RF re-radiation at the antenna
- CMOS logic interface to standard decoder and micro-processor ICs
- Extremely low external part count
- No filters or inductors required

Applications

- Automotive Remote Keyless Entry (RKE)
- Long Range RF Identification
- Remote fan and light control
- Garage door and gate openers

Typical Application



315MHz 1200b/s On-Off Keyed Receiver

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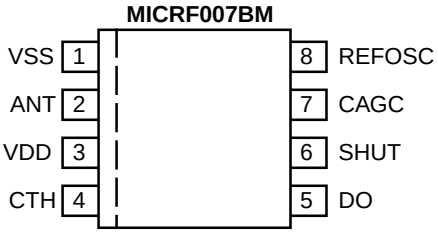
Ordering Information

Part Number	Demodulator Bandwidth	Package
MICRF007BM	2100Hz	8-Pin SOIC

Other voltages available. Contact Micrel for details.

Pin Configuration



8-Pin SOP (M) Package

Pin Description

Pin Number	Pin Name	Pin Function
1	VSS	Ground Return (Input): Ground return to the power supply. See “Application Information” for bypass capacitor details.
2	ANT	Antenna (Input): High-impedance, internally ac coupled receiver input. Connect this pin to the receive antenna. This FET gate input has approximately 2pF of shunt (parasitic) capacitance. See “Applications Information” for optional band-pass filter information.
3	VDD	Power Supply (Input): Positive supply input for the RF IC. Connect a low ESL, low ESR decoupling capacitor from this pin to VSS, lead lengths should be as short as possible.
4	CTH	[Data Slicing] Threshold Capacitor (External Component): Capacitor extracts the dc average value from the demodulated waveform which becomes the reference for the internal data slicing comparator. See “Applications Information” for selection.
5	DO	Digital Output (Output): CMOS-level compatible data output signal.
6	SHUT	Shutdown (Input): Shutdown-mode logic-level control input. Pull low to enable the receiver. This input has an internal pulled-up to VDD.
7	CAGC	AGC Capacitor (External Component): Integrating capacitor for on-chip AGC (automatic gain control). The decay/attack time-constant (t) ratio is nominally 10:1. See “Applications Information” for capacitor selection.
8	REFOSC	Reference Oscillator (External Component or Input): Timing reference for on-chip tuning and alignment. Connect a crystal between this pin and VSS, or drive the input with an ac-coupled 0.5Vpp input clock.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{DDRF}, V_{DDBB}) ..... +7V
Input/Output Voltage ($V_{I/O}$) ..... V_{SS}–0.3 to V_{DD}+0.3
Junction Temperature (T_J) ..... +150°C
Storage Temperature Range (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +260°C
ESD Rating, **Note 3**

Operating Ratings (Note 2)

Supply Voltage (V_{DD}, V_{DDBB}) ..... +4.75V to +5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance (θ_{JA})
16-pin DIP (θ_{JA}) ..... 90°C/W
16-pin SOIC (θ_{JA}) ..... 120°C/W

Electrical Characteristics

$V_{DDRF} = V_{DDBB} = V_{DD}$ where +4.75V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V; C_{AGC} = 4.7µF, C_{TH} = 0.047µF; f_{REFOSC} = 4.90MHz; T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; current flow into device pins is positive; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OP}	Operating Current	continuous operation		3	**5.5**	mA
		10:1 duty cycle		300		µA
I_{STBY}	Standby Current	$V_{SHUT} = V_{DD}$		0.5		µA
RF Section, IF Section						
	Receiver Sensitivity	**Notes 4, 6**		–96	–90	dBm
f_{IF}	IF Center Frequency	**Note 7**		0.86		MHz
f_{BW}	IF 3dB Bandwidth	**Notes 6, 7**	**400**	0.43		kHz
f_{ANT}	RF Input Range		**300**		**440**	MHz
	Receive Modulation Duty-Cycle		**20**		**80**	%
	Maximum Receiver Input	R_{SC} = 50Ω			**–20**	dBm
	Spurious Reverse Isolation	ANT pin, R_{SC} = 50Ω, **Note 5**		1		µVrms
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$		0.1		
	AGC Leakage Current	T_A = +85°C		100		nA
Reference Oscillator						
	Reference Oscillator Stabilization Time	to 1% of final value		2.5	3.1	ms
Z_{REFOSC}	Reference Oscillator Input Impedance			290		kΩ
	Reference Oscillator Input Range		0.1		1.5	V_{P-P}
	Reference Oscillator Source Current		4.5 **2.8**	5.2		µA
Demodulator						
Z_{CTH}	CTH Source Impedance	**Note 8**		110		kΩ
ΔZ_{CTH}	CTH Source Impedance Variation		**–15**		**+15**	%
$I_{ZCTH(leak)}$	CTH Leakage Current	T_A = +85°C		±100		nA
	Demodulator Filter Bandwidth	$V_{SEL0} = V_{SEL1} = V_{SWEN} = V_{DD}$, **Notes 7, 9**		4160		Hz
	Demodulator Filter Bandwidth	$V_{SEL0} = V_{SEL1} = V_{DD}$, $V_{SWEN} = V_{SS}$, **Notes 5, 7, 9**		8320		Hz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital/Control Section						
$I_{IN(pu)}$	Input Pull-Up Current	SEL0, SEL1, SWEN, $V_{SHUT} = V_{SS}$		8		µA
$V_{IN(high)}$	Input-High Voltage	SEL0, SEL1, SWEN			**$0.8V_{DD}$**	V
$V_{IN(low)}$	Input-Low Voltage	SEL0, SEL1, SWEN	**$0.2V_{DD}$**			V
I_{OUT}	Output Current	DO, WAKEB pins, push-pull		10		µA
$V_{OUT(high)}$	Output High Voltage	DO, WAKEB pins, I_{OUT} = –1µA	**$0.9V_{DD}$**			V
$V_{OUT(low)}$	Output Low Voltage	DO, WAKEB pins, I_{OUT} = +1µA			**$0.1V_{DD}$**	V
t_R, t_F	Output Rise and Fall Times	DO, WAKEB pins, C_{LOAD} = 15pF			**10**	µs

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Use appropriate ESD precautions. Meets class 1 ESD test requirements, (human body model HBM), in accordance with MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.

Note 4: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10^{-2} BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded data) at a data rate of 300b/s. The RF input is assumed to be matched into 50Ω.

Note 5: Spurious reverse isolation represents the spurious components which appear on the RF input pin (ANT) measured into 50Ω with an input RF matching network.

Note 6: Sensitivity, a commonly specified receiver parameter, provides an indication of the receiver's input referred noise, generally input thermal noise. However, it is possible for a more sensitive receiver to exhibit range performance no better than that of a less sensitive receiver if the background noise is appreciably higher than the thermal noise. Background noise refers to other interfering signals, such as FM radio stations, pagers, etc.

A better indicator of achievable receiver range performance is usually given by its selectivity, often stated as intermediate frequency (IF) or radio frequency (RF) bandwidth, depending on receiver topology. Selectivity is a measure of the rejection by the receiver of "ether" noise. More selective receivers will almost invariably provide better range. Only when the receiver selectivity is so high that most of the noise on the receiver input is actually thermal will the receiver demonstrate sensitivity-limited performance.

Note 7: Parameter scales linearly with reference oscillator frequency f_T. For any reference oscillator frequency other than 4.90MHz, compute new parameter value as the ratio:

$$\frac{f_{REFOSC}\text{MHz}}{4.90} \times (\text{parameter value at 4.90MHz})$$

Example: For reference oscillator freqency f_T = 6.00MHz:

$$(\text{parameter value at 6.00MHz}) = \frac{6.00}{4.90} \times (\text{paramter value at 4.90MHz})$$

Note 8: Parameter scales inversely with reference oscillator frequency f_T. For any reference oscillator frequency other than 4.90MHz, compute new parameter value as the ratio:

$$\frac{4.90}{f_{REFOSC}\text{MHz}} \times (\text{parmeter value at 4.90MHz})$$

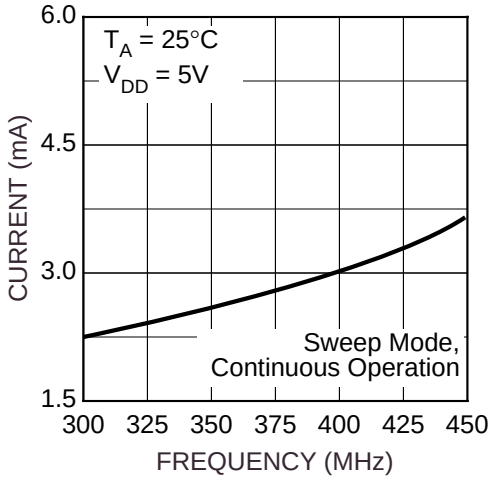
Example: For reference oscillator frequency f_T = 6.00MHz:

$$(\text{parmeter value at 6.00MHz}) = \frac{4.90}{6.00} \times (\text{parmeter value at 4.90MHz})$$

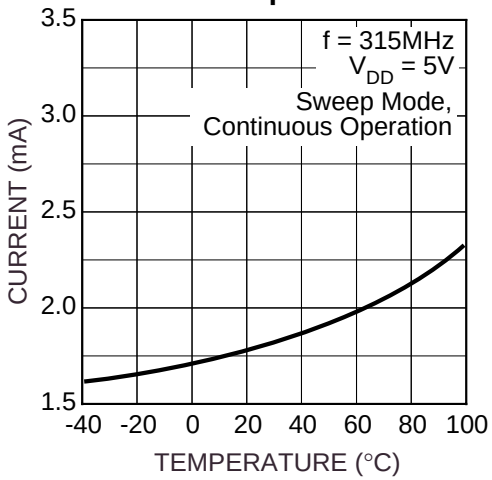
Note 9: Demodulator filter bandwidths are related in a binary manner, so any of the (lower) nominal filter values may be derived simply by dividing this parameter value by 2, 4, or 8 as desired.

Typical Characteristics

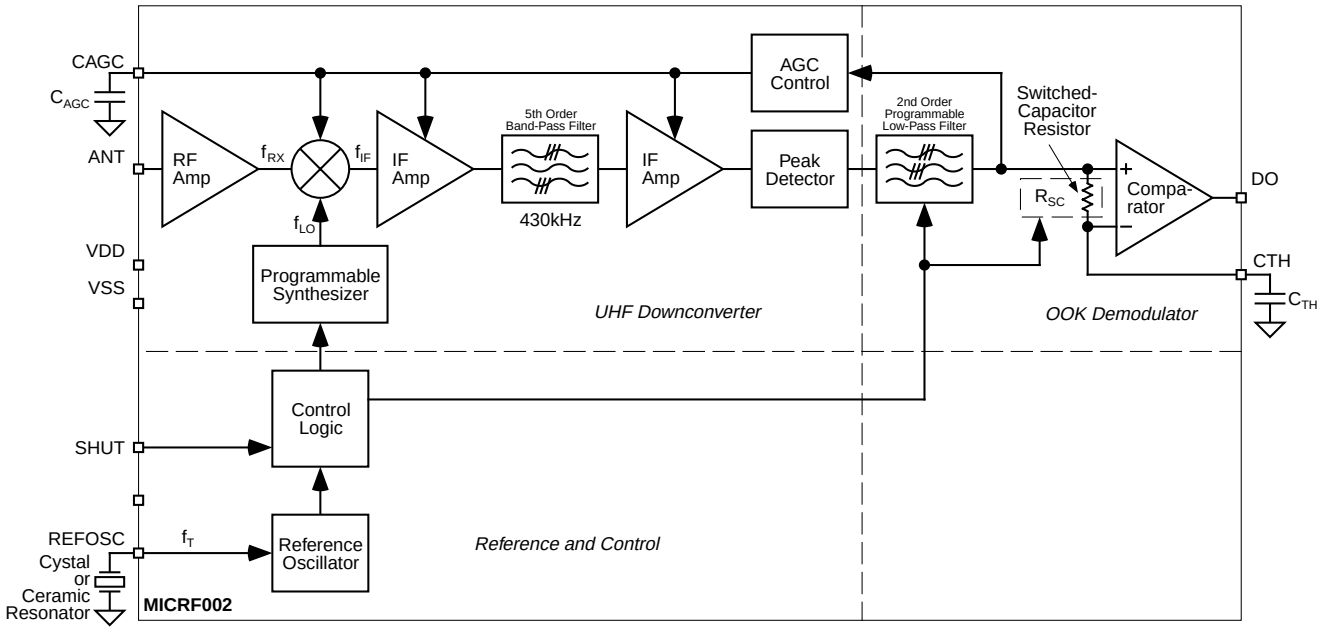
Supply Current vs. Frequency



Supply Current vs. Temperature



Functional Diagram



MICRF007 Block Diagram

Functional Description

Refer to "MICRF007 Block Diagram". Identified in the block diagram are the three sections of the IC: UHF Downconverter, OOK Demodulator and Reference and Control, and Wakeup. Also shown in the figure are two capacitors (C_{TH}, C_{AGC}) and one timing component (Y1), usually a crystal. With the exception of a supply decoupling capacitor, these are the only external components needed by the MICRF007 to assemble a complete UHF receiver. There is one control input, the SHUT pin. The SHUT function is used to enable the reciever. These inputs are CMOS compatible, and are pulled-up on the IC.

Receiver Operation

The MICRF007 is a standard superheterodyne receiver with a narrow RF bandwidth IF. The narrow bandwidth receiver is less susceptible to interfering RF signals. The MICRF007 is capable of data rates up to 2.1kbps. Typically a crystal is used for the reference oscillator frequency. The MICRF007 RF center frequency is controlled by a completely integrated PLL / VCO frequency synthesizer which is referenced to the crystal frequency.

Since the MICRF007 bandwidth is 430kHz, a tight tolerance transmitter must be used for the system. Typically SAW or crystal based transmitters are used in application designs.

IF Bandpass Filter

Rolloff response of the IF Filter is 5th order, while the demodulator data filter exhibits a 2nd order response.

Baseband Demodulator Filter Bandwidth

The MICRF007 has a fully intergrated baseband demodulator filter. The filter has a fixed 2.1kHz bandwidth. This filter limits the reciever raw data rate to 2kbps.

Data Slicing Level

Extraction of the dc value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip switched-capacitor "resistor" R_{SC}, shown in the block diagram. The effective resistance of R_{SC} is 118kΩ.

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms. Optimization of the value of C_{TH} is required to maximize range.

Automatic Gain Control

The signal path has AGC (automatic gain control) to increase input dynamic range. An external capacitor, C_{AGC}, must be connected to the CAGC pin of the device. The ratio of decay-to-attack time-constant is fixed at 10:1 (that is, the attack time constant is 1/10th of the decay time constant), and this ratio cannot be changed by the user. However, the attack time constant is set externally by choosing a value for C_{AGC}.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF007 in excess of 100:1. When the device is placed into shutdown mode (SHUT pin pulled high), the AGC capacitor floats, to retain the voltage. When operation is resumed, only the voltage droop on the capacitor due to leakage must be replenished, therefore a relatively low-leakage capacitor is recommended for duty-cycled operation. The actual tolerable leakage will be application dependent. Clearly, leakage performance is less critical when the device off-time is low (milliseconds) and more critical when the off-time is high (seconds).

To further enhance duty-cycled operation of the IC, the AGC push and pull currents are increased for a fixed time immediately after the device is taken out of shutdown mode (turned-on). This compensates for AGC capacitor voltage droop while the IC is in shutdown mode, reduces the time to restore the correct AGC voltage, and therefore extends maximum

achievable duty ratios. Push-pull currents are increased by 45 times their nominal values. The fixed time period is based on the reference oscillator frequency f_T, 10.9ms for f_T = 6.00MHz, and varies inversely as f_T varies.

Reference Oscillator

All timing and tuning operations on the MICRF007 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of two ways:

1. Connect a crystal
2. Drive this pin with an external timing signal

The multiplication factor between the reference oscillator frequency f_T and the internal local oscillator (LO) is 64.5×. For $f_T = f_{LO}$ = 6.00MHz × 64.5 = 387MHz.

The second approach is attractive for lowering system cost further if an accurate reference signal exists elsewhere in the system, for example, a reference clock from a crystal-controlled microprocessor. An externally applied signal should be ac-coupled and resistively-attenuated, or otherwise limited, to approximately 0.5Vpp. The specific reference frequency required is related to the system transmit frequency.

Shutdown Function

The shutdown function is controlled by a logic state applied to the SHUT pin. When V_{SHUT} is high, the device goes into low-power standby mode, consuming less than 1µA. This pin is pulled high internally. It must be externally pulled low to enable the receiver.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF007 are diagrammed in Figures 1 through 6. The ESD protection diodes at all input and output pins are not shown.

ANT Pin

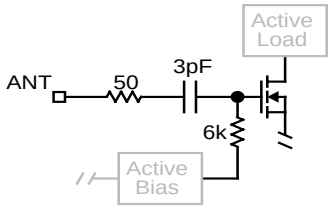


Figure 1a. ANT Pin

The ANT pin is internally AC-coupled via a 3pF capacitor, to an RF N-channel MOSFET, as shown in Figure 1. Impedance on this pin to VSS is quite high at low frequencies, and decreases as frequency increases. In the UHF frequency range, the device input can be modeled as 6.3kΩ in parallel with 2pF (pin capacitance) shunt to VSS0RF.

CTH Pin

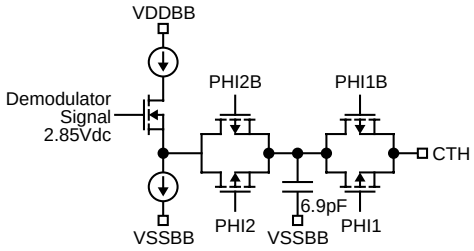


Figure 2. CTH Pin

Figure 2 illustrates the CTH-pin interface circuit. The CTH pin is driven from a P-channel MOSFET source-follower with approximately 10µA of bias. Transmission gates TG1 and TG2 isolate the 6.9pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a “resistance” of approximately 100kΩ. The dc potential at the CTH pin is approximately 1.6V

CAGC Pin

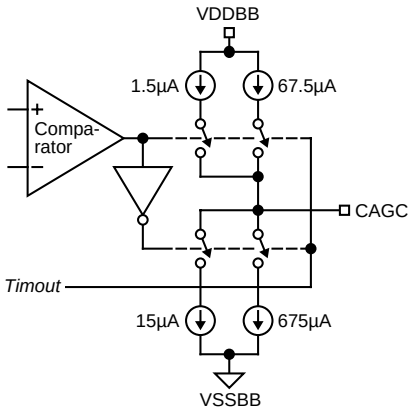


Figure 3. CAGC Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor C_{AGC}. The attack current is nominally 15µA, while the decay current is a 1/10th scaling of this, nominally 1.5µA, making the attack/decay timeconstant ratio a fixed 10:1. Signal gain of the RF/IF strip inside the IC diminishes as the voltage at CAGC decreases. Modification of the attack/decay ratio is possible by adding resistance from the CAGC pin to V_{DD}.

Both the push and pull current sources are disabled during shutdown, which maintains the voltage across C_{AGC}, and improves recovery time in duty-cycled applications. To further improve duty-cycle recovery, both push and pull currents are increased by 45 times for approximately 10ms after release of the SHUT pin. This allows rapid recovery of any voltage droop on C_{AGC} while in shutdown.

DO Pin

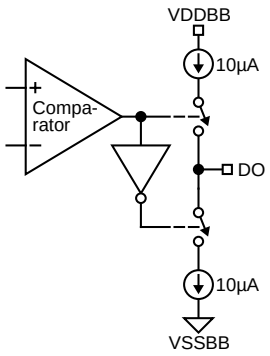


Figure 4. DO Pin

The output stage for DO (digital output) is shown in Figure 4. The output is a 10µA push and 10µA pull switched-current stage. This output stage is capable of driving CMOS loads. An external buffer-driver is recommended for driving high-capacitance loads.

REFOSC Pin

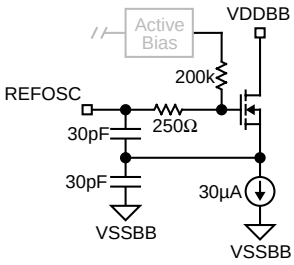


Figure 5. REFOSC Pin

The REFOSC input circuit is shown in Figure 5. Input impedance is high (200kΩ). This is a Colpitts oscillator with internal 30pF capacitors. This input is intended to work with standard ceramic resonators connected from this pin to the VSS pin, although a crystal may be used when greater frequency accuracy is required. The nominal dc bias voltage on this pin is 1.4V.

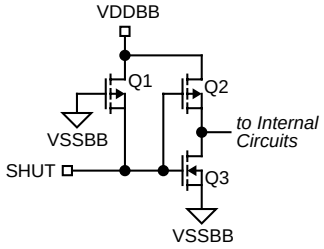


Figure 6. SHUT

Control input circuitry is shown in Figure 6. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-channel MOSFET Q1 is a large channel length device which functions essentially as a “weak” pullup to VDD. Typical pullup current is 5μA, leading to an impedance to the VDD supply of typically 1MΩ.

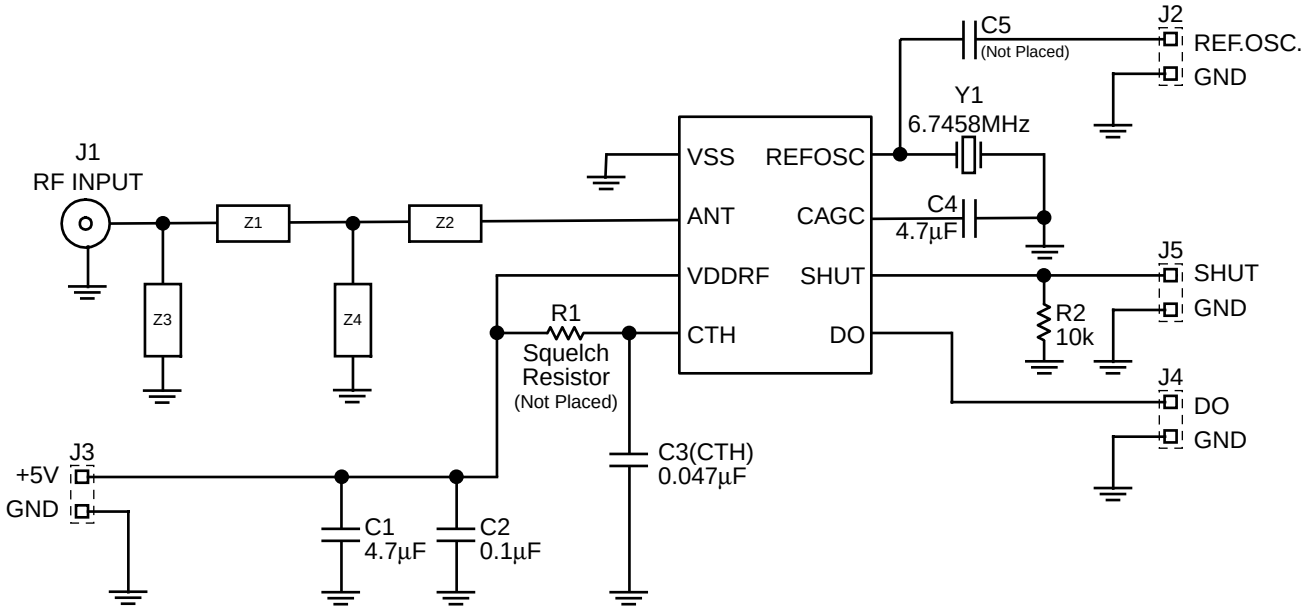
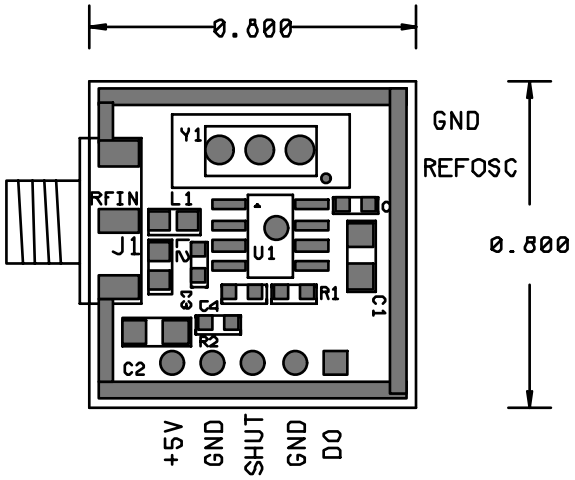


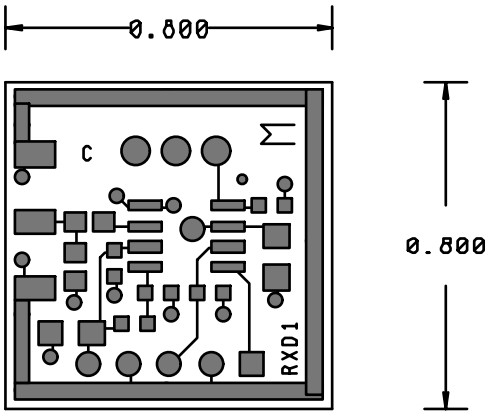
Figure 1. Test Circuit

PCB Layout Information

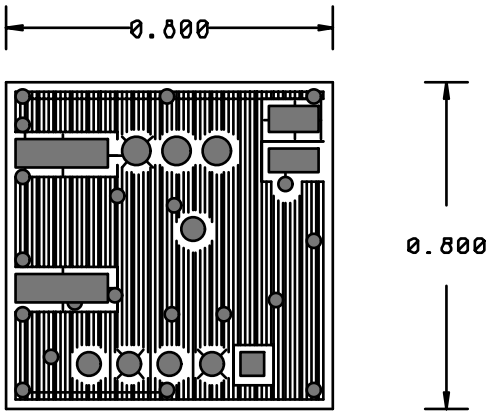
The MICRF007 evaluation board was designed and characterized using two sided 0.031 inch thick FR4 material with 1 ounce copper clad. If another type of printed circuit board material were to be substituted, impedance matching and characterization data stated in this document may not be valid.



PCB Silk Screen



PCB Component Side Layout



PCB Solder Side Layout

Application Information

Transmitter Compatibility

Generally, best performance and range will be realized when the MICRF007 is operated in a system using a SAW or crystal based transmitter. The receiver reference oscillator requires the use of a crystal.

Bypass Capacitors

The power supply bypass capacitors connected to VDD should have the shortest possible lead lengths. For best performance, connect directly to VSS

Optional BandPass Filter

For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and VSS to provide additional receive selectivity and input overload protection. A typical filter is included in Figure 7a.

Data Squelching

During quiet periods (no signal) the data output (DO pin) transitions randomly with noise, presenting problems for some decoders. A simple solution is to introduce a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal comparator. Usually 20mV to 30mV is sufficient, and may be introduced by connecting a several-megohm resistor from the CTH pin to either V_{SS} or V_{DD}, depending on the desired offset polarity. Since the MICRF007 has receiver AGC, noise at the internal comparator input is always the same, set by the AGC. The squelch offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce range modestly. Only introduce an amount of offset sufficient to quiet the output.

AGC Configuration

By adding resistance from the CAGC pin to VDDBB or VSSBB in parallel with the AGC capacitor, the ratio of decay-to-attack time constant may be varied, although the value of such adjustments must be studied on a per-application basis. Generally the design value of 10:1 is adequate for the vast majority of applications.

To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under 10mVpp once the control voltage has attained its quiescent value. For this reason capacitor values of at least 0.47µF are recommended.

Crystal Selection

Selecting Reference Oscillator Frequency f_T

As with any superheterodyne receiver, the difference between the internal LO (local oscillator) frequency f_{LO} and the incoming transmit frequency f_{TX} ideally must equal the IF center frequency. Equation 1 may be used to compute the appropriate f_{LO} for a given f_{TX}:

$$(1) \quad f_{LO} = f_{TX} \pm \left(1.064 \frac{f_{TX}}{390}\right)$$

Frequencies f_{TX} and f_{LO} are in MHz. Note that two values of f_{LO} exist for any given f_{TX}, distinguished as "high-side mixing" and "low-side mixing," and there is generally no preference of one over the other.

After choosing one of the two acceptable values of f_{LO}, use Equation 2 to compute the reference oscillator frequency f_T:

$$(2) \quad f_T = \frac{f_{LO}}{64.5}$$

Frequency f_T is in MHz. Connect a crystal of frequency f_T to REFOSC on the MICRF007. Four-decimal-place accuracy on the frequency is generally adequate. The following table identifies f_T for some common transmit frequencies.

Transmit Frequency f_{TX}	Reference Oscillator Frequency f_T
315MHz	4.8970MHz
390MHz	6.0630MHz
418MHz	6.4983MHz
433.92MHz	6.7458MHz

Table 2. Common Transmitter Frequencies

External Timing Signals

Externally applied signals should be ac-coupled and the amplitude must be limited to approximately 0.5Vpp.

Frequency and Capacitor Selection

Selection of the slicing level capacitor (C_{TH}), and AGC capacitor (C_{AGC}) are briefly summarized in this section.

Selecting Capacitor C_{TH}

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure (that is, existence of data preamble, etc.). This issue is covered in more detail in Application Note 22.

Source impedance of the CTH pin is given by equation (4), where f_T is in MHz:

$$(4) \quad R_{SC} = 118k\Omega \frac{4.90}{f_T}$$

Assuming that a slicing level time constant τ has been established, capacitor C_{TH} may be computed using equation

$$(5) \quad C_{TH} = \frac{\tau}{R_{SC}}$$

A standard ±20% X7R ceramic capacitor is generally sufficient.

Selecting C_{AGC} Capacitor in Continuous Mode

Selection of C_{AGC} is dictated by minimizing the ripple on the AGC control voltage by using a sufficiently large capacitor. Factory experience suggests that C_{AGC} should be in the vicinity of 0.47µF to 4.7µF. Large capacitor values should be carefully considered as this determines the time required for the AGC control voltage to settle from a completely discharged condition. AGC settling time from a completely discharged (zero-volt) state is given approximately by Equation 6:

(6) $\Delta t = 1.333 C_{AGC} - 0.44$

where:

C_{AGC} is in µF, and Δt is in seconds.

Selecting C_{AGC} Capacitor in Duty-Cycle Mode

Generally, droop of the AGC control voltage during shutdown should be replenished as quickly as possible after the IC is "turned-on". As described in the functional description, for about 10ms after the IC is turned on, the AGC push-pull currents are increased to 45 times their normal values. Consideration should be given to selecting a value for C_{AGC} and a shutdown time period such that the droop can be replenished within this 10ms period.

Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. Worst-case from a recovery standpoint is downward droop, since the AGC pullup current is 1/10th magnitude of the pulldown current. The downward droop is replenished according to the Equation 7:

(7) $$\frac{I}{C_{AGC}} = \frac{\Delta V}{\Delta t}$$

where:

I = AGC pullup current for the initial 10ms (67.5µA)

C_{AGC} = AGC capacitor value

Δt = droop recovery time

ΔV = droop voltage

For example, if user desires Δt = 10ms and chooses a 4.7µF C_{AGC}, then the allowable droop is about 144mV. Using the same equation with 200nA worst case pin leakage and assuming 1µA of capacitor leakage in the same direction, the maximum allowable Δt (shutdown time) is about 0.56s for droop recovery in 10ms.

315.0MHz Receiver/Decoder Application

Figure 7a illustrates a typical application for the MICRF007 UHF Receiver IC. This receiver operates continuously (not duty cycled), and features 6-bit address decoding and two output code bits.

Operation in this example is at 315.5MHz, and may be customized by selection of the appropriate frequency reference (Y1), and adjustment of the antenna length. The value of C4 would also change if the optional input filter is used. Changes from the 1kb/s data rate may require a change in the value of R1. A bill of materials accompanies the schematic.

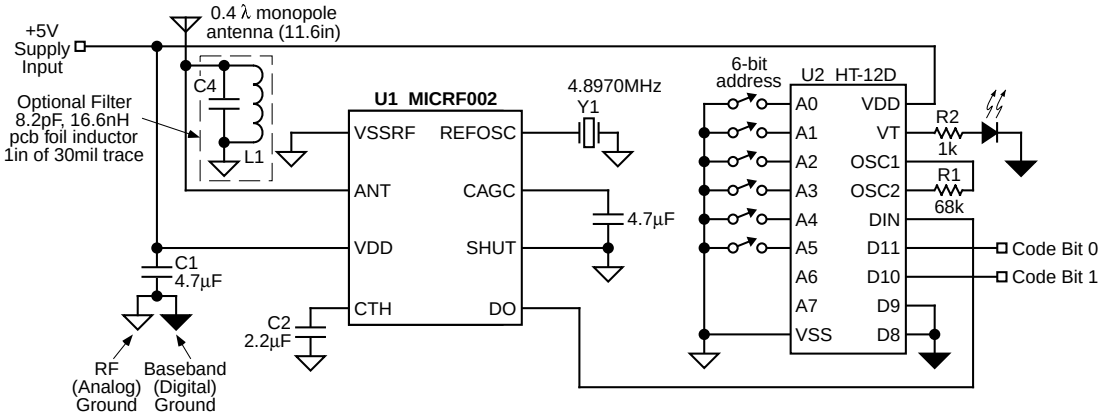


Figure 7a. 315MHz, 1kb/s On-Off Keyed Receiver/Decoder

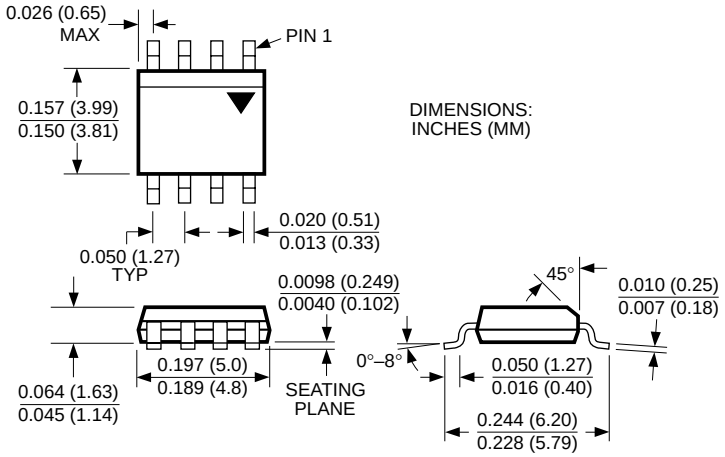
Item	Part Number	Manufacturer	Description
U1	MICRF002	Micrel	UHF receiver
U2	HT-12D	Holtek	logic decoder
CR1	CSA6.00MG	Murata	6.00MHz ceramic resonator
D1	SSF-LX100LID	Lumex	red LED
R1			68k 1/4W 5%
R2		Vishay	1k 1/4W 5%
C1		Vishay	4.7µF dipped tantalum capacitor
C3		Vishay	4.7µF dipped tantalum capacitor
C2		Vishay	2.2µF dipped tantalum capacitor
C4		Vishay	8.2pF COG ceramic capacitor

Figure 7b. Bill of Material

Vendor	Telephone	FAX
Vishay	(203) 268-6261	—
Holtek	(408) 894-9046	(408) 894-0838
Lumex	(800) 278-5666	(847) 359-8904
Murata	(800) 241-6574	(770) 436-3030

Figure 7c. Component Vendors

Package Information



8-Lead SOP (M)

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