

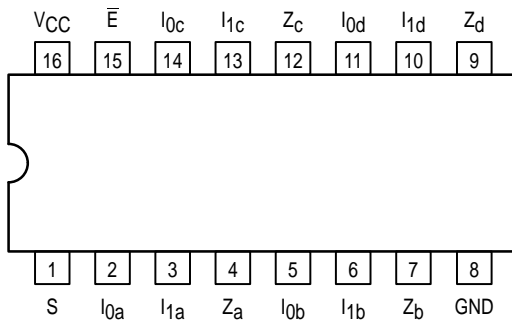


# QUAD 2-INPUT MULTIPLEXER

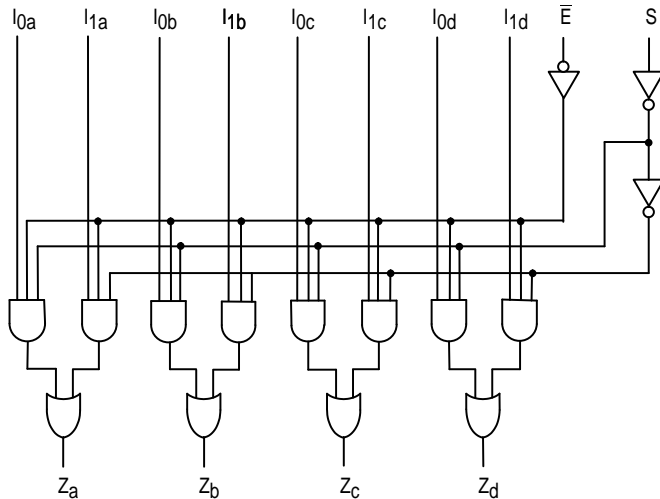
The MC74F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The F157A can also be used to generate any four of the 16 different functions to two variables.

- AC Enhanced Version of the F157

### CONNECTION DIAGRAM DIP (TOP VIEW)



### LOGIC DIAGRAM



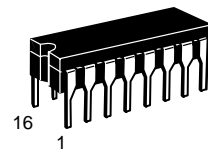
### FUNCTION TABLE

Inputs				Output
$\bar{E}$	S	$I_0$	$I_1$	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

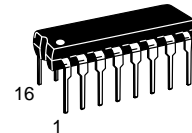
H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

## MC74F157A

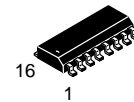
### QUAD 2-INPUT MULTIPLEXER FAST™ SHOTTKY TTL



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

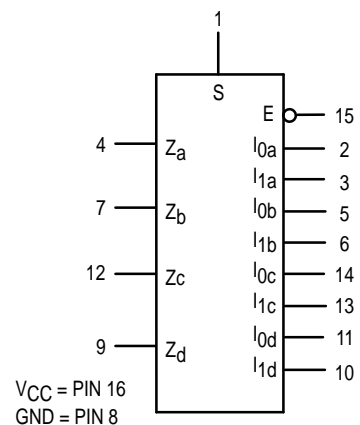


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

MC74FXXXJ Ceramic  
MC74FXXXN Plastic  
MC74FXXXD SOIC

### LOGIC SYMBOL



# MC74F157A

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	74	4.5	5.0	5.5	V
T <sub>A</sub>	Operating Ambient Temperature Range	74	0	25	70	°C
I <sub>OH</sub>	Output Current — High	74			-1.0	mA
I <sub>OL</sub>	Output Current — Low	74			20	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V <sub>IK</sub>	Input Clamp Diode Voltage			-1.2	V	I <sub>IN</sub> = -18 mA	V <sub>CC</sub> = MIN
V <sub>OH</sub>	Output HIGH Voltage	74	2.7	3.4	V	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.75 V
		74	2.5				V <sub>CC</sub> = 4.50 V
V <sub>OL</sub>	Output LOW Voltage		0.35	0.5	V	I <sub>OL</sub> = 20 mA	V <sub>CC</sub> = MIN
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>IN</sub> = 2.7 V	V <sub>CC</sub> = MAX
				100	μA	V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.6	mA	V <sub>IN</sub> = 0.5 V	V <sub>CC</sub> = MAX
I <sub>OS</sub>	Output Short Circuit Current (Note 2)	-60		-150	mA	V <sub>OUT</sub> = 0 V	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current		15	23	mA	All Inputs = 4.5 V	V <sub>CC</sub> = MAX

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to 70°C V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF		
		Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.5	10	3.5	11	ns
t <sub>PHL</sub>	S to Z <sub>n</sub>	3.0	7.0	3.0	8.0	
t <sub>PLH</sub>	Propagation Delay	3.5	9.5	3.5	11	ns
t <sub>PHL</sub>	$\bar{E}$ to Z <sub>n</sub>	2.5	6.5	2.5	7.0	
t <sub>PLH</sub>	Propagation Delay	2.0	6.0	2.0	6.5	ns
t <sub>PHL</sub>	I <sub>n</sub> to Z <sub>n</sub>	2.5	5.5	2.0	7.0	

## FUNCTIONAL DESCRIPTION

The F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

A common use of the F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$