

SANYO

No. 5115

LC89915, 89915M**NTSC 1 H Delay Line**

Overview

The LC89915 and LC89915M are delay lines that produce a 1 H delayed signal for NTSC format with an external low-pass filter. It can also provide 1 H delayed signal for PAL format by changing the number of its CCD shift register.

Functions

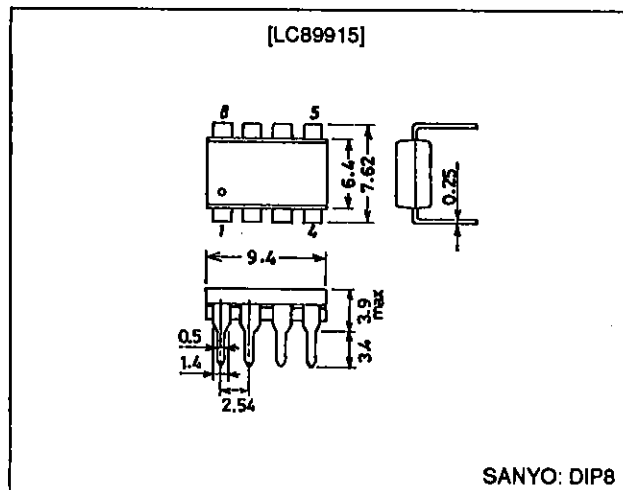
- 453.5 bits (switchable to 456.5 bits) CCD shift register
- Auto-bias circuit
- Sync tip clamping circuit
- Sample-and-hold circuit
- Delay time switching circuit

Features

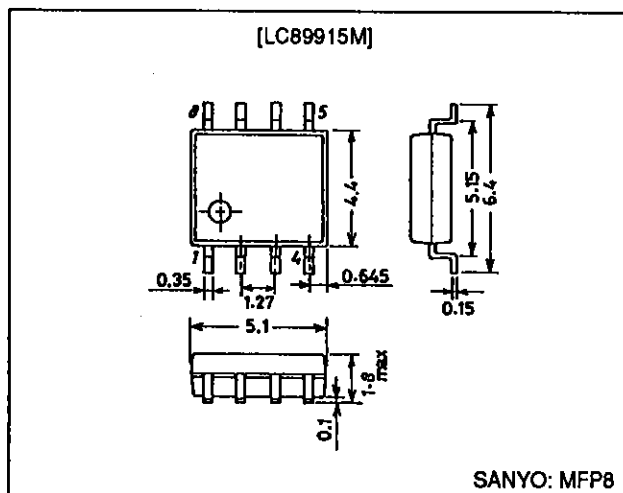
- Single 5 V power supply
- Operates on a low-amplitude clock input.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output
- Control pin switchable to provide a PAL 1 H delayed signal.

Package Dimensions

unit: mm

3001B-DIP8

unit: mm

3032B-MFP8

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------|------------|--------------|------------------|
| Maximum supply voltage | $V_{DD\ max}$ | | -0.3 to +6.0 | V |
| Allowable power dissipation | $P_d\ max$ | LC89915 | 400 | mW |
| | | LC89915M | 140 | mW |
| Operating temperature | T_{opr} | | -10 to +60 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

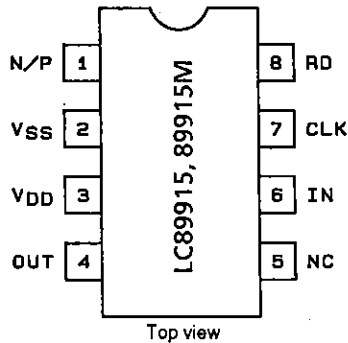
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Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------|------------------|------------|------|-----------|------|-------|
| Supply voltage | V _{DD} | | 4.75 | 5.00 | 5.25 | V |
| Clock input amplitude | V _{CLK} | Sine wave | 100 | 300 | 1000 | mVp-p |
| Clock frequency | F _{CLK} | | — | 7.1590909 | — | MHz |
| Signal input amplitude | V _{IN} | * | — | 500 | — | mVp-p |

Note: * Connect the input signal with a low impedance to assure correct sync tip clamping.

Pin Assignment

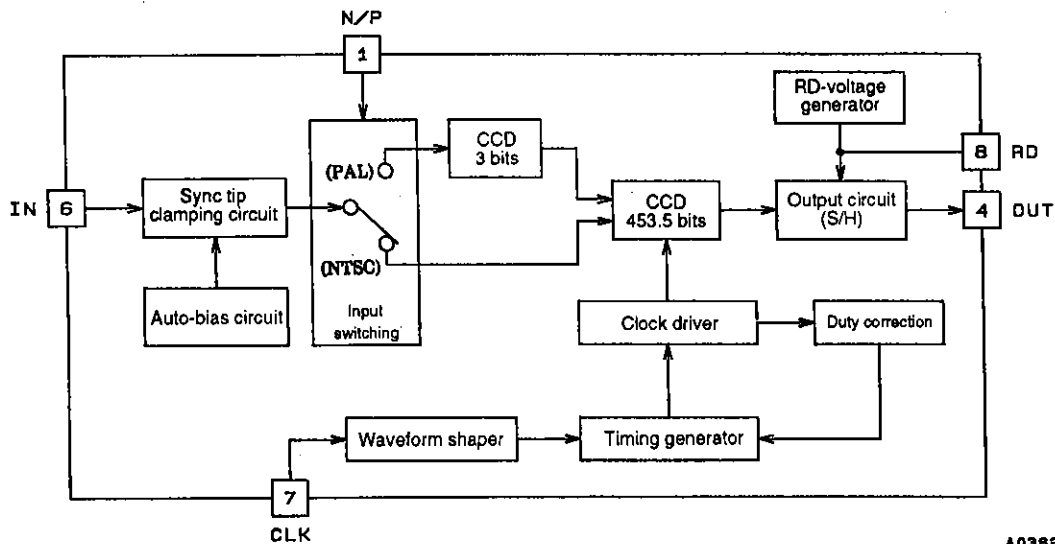


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Pin Functions

| Pin No. | Symbol | Function |
|---------|-----------------|-----------------------------|
| 1 | N/P | Delay time switching |
| 2 | V _{SS} | GND |
| 3 | V _{DD} | Power supply |
| 4 | OUT | Delayed signal output |
| 5 | NC | |
| 6 | IN | Signal input |
| 7 | CLK | Clock input |
| 8 | RD | RD-voltage generator output |

Block Diagram



Functional Description

The delay time can be switched with the N/P control pin (pin 1).

0 V — NTSC mode

The CCD has a length of 453.5 bits and the delay time corresponds to 1 H (63.5 μs) in the NTSC format.

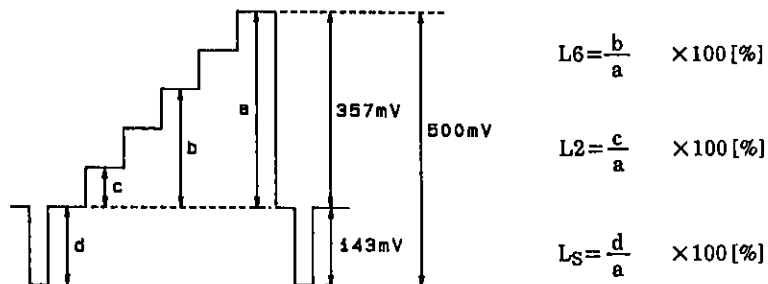
5 V — PAL mode

The CCD has a length of 456.5 bits and the delay time corresponds to 1 H (64.0 μs) in the PAL format.

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Electrical Characteristics at Ta = 25°C, VDD = 5.0 V, CLK = 7.1590909 MHz; 300 mVp-p; sine wave

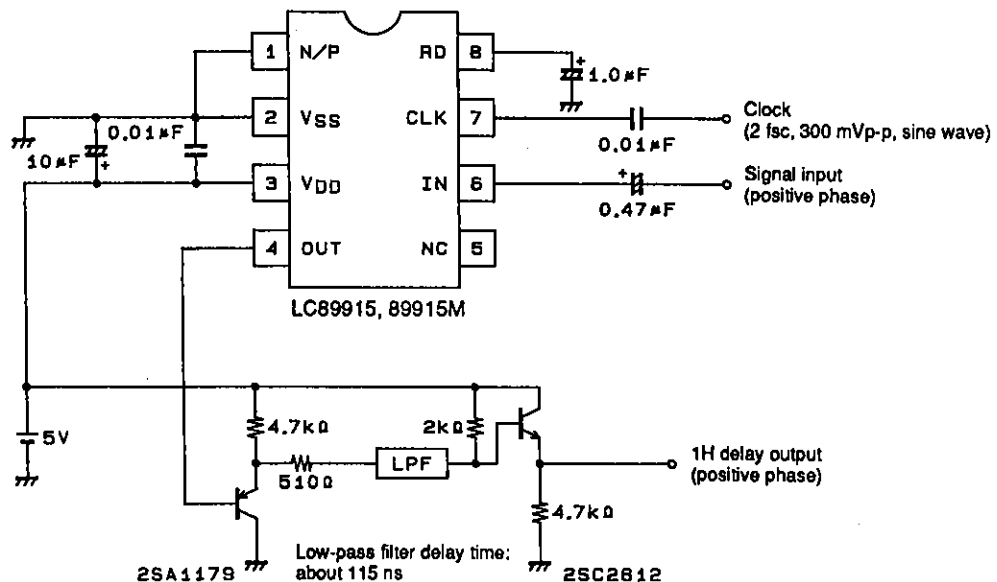
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|------------------|--------------------------------------|------|-------|-----|-------|
| Current drain | I _{DD} | No signal input | 4 | 8 | 12 | mA |
| Voltage gain | G _V | With a 200 kHz 0.5 Vp-p input | 2.5 | 4.5 | 6.5 | dB |
| Frequency characteristics | G _f | 2.0 MHz, 0.2 Vp-p/200 kHz, 0.2 Vp-p | -3.0 | -1.5 | | dB |
| Linearity | L6 | * | 56 | 60 | 64 | % |
| | L2 | * | 18 | 20 | 22 | % |
| | L _S | * | 37 | 40 | 43 | % |
| Clock leakage | L _{CLK} | No signal input, the 2 fsc component | | 10 | 30 | mVrms |
| Noise | N _O | No signal input, 4.2 MHz bandwidth | | 1.0 | 2.0 | mVrms |
| Output impedance | Z _O | | 200 | 300 | 400 | Ω |
| Delay time | T _{D-N} | | | 63.44 | | μs |
| | T _{D-P} | | | 63.88 | | μs |



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Note: * Input signal/output signal

Sample Application Circuit



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