DATA SHEET

~~74F175~~*, 74F175A
Quad D flip-flop

** Discontinued part. Please see the Discontinued Product List in Section 1, page 21.*

Product specification

1996 Mar 12

IC15 Data Handbook

Philips
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Quad D flip-flop 74F175A

FEATURES

- Four edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- True and complementary outputs
- Industrial temperature range available (–40°C to +85°C)
- PNP light loading inputs

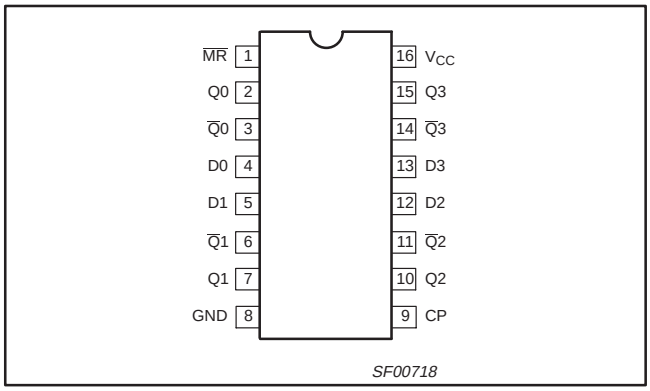
DESCRIPTION

The 74F175A is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of clock or data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required, and the CP and $\overline{MR}$ are common to all storage elements.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175A	160MHz	22mA

ORDERING INFORMATION

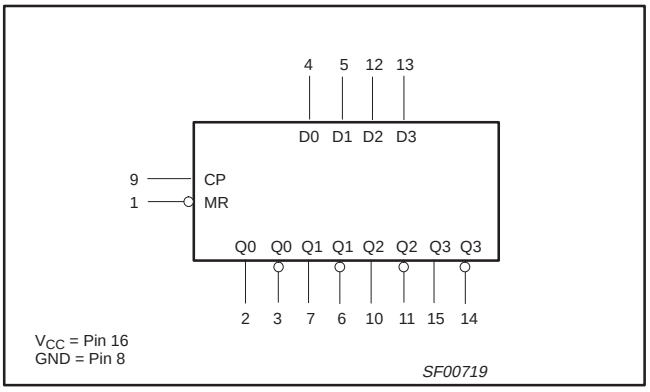
DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74F175AN	SOT38-4
16-pin plastic SO	74F175AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

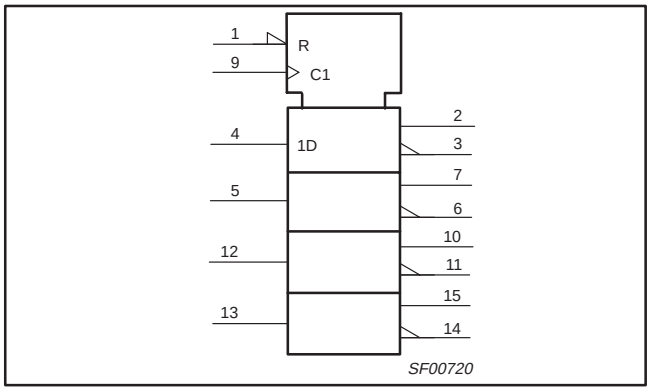
PINS	DESCRIPTION		74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	74F175A	1.0/0.033	20µA/20µA
$\overline{MR}$	Master reset input (active–Low)	74F175A	1.0/0.033	20µA/20µA
CP	Clock input (active rising edge)	74F175A	1.0/0.033	20µA/20µA
Q0–Q3	True outputs		50/33	1.0mA/20mA
$\overline{Q}$0–$\overline{Q}$3	Complementary outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

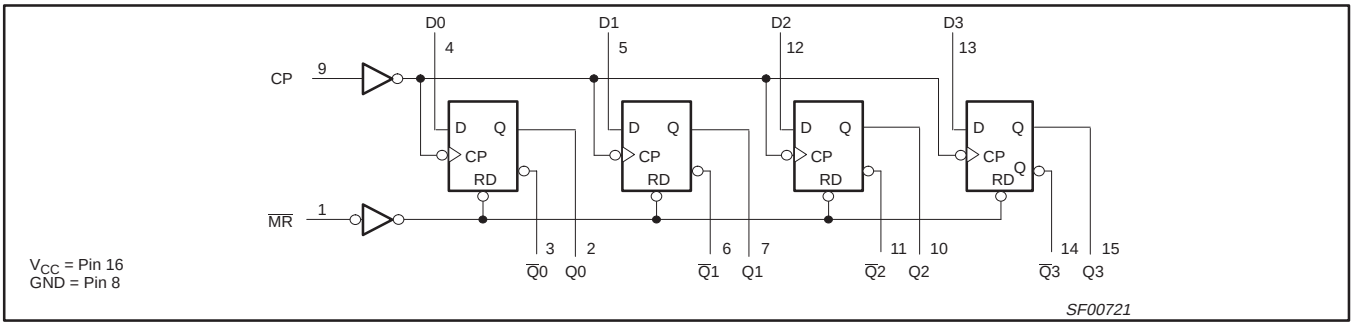
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	Dn	Q_n	$\overline{Q}_n$	
L	X	X	L	H	Reset (clear)
H	↑	h	H	L	Load “1”
H	↑	l	L	H	Load “0”

H = High voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don’t care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}= MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.5	V
			±5%V_{CC}		0.30	0.5	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	74F175A			–20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	74F175A		22	31	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F175A

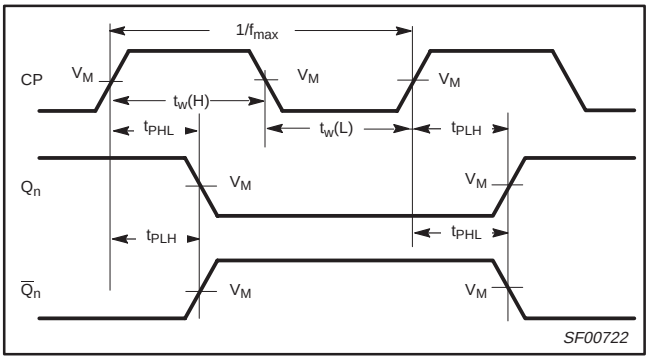
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = 25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	140	160		125		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	Waveform 1	3.0 4.5	4.0 6.0	6.5 8.5	2.5 4.0	7.5 9.0	2.5 4.0	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 3	4.5	6.5	9.0	4.5	10.0	4.5	11.0	ns
t_{PHL} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}$n	Waveform 3	4.5	6.0	8.0	4.0	9.0	4.0	10.0	ns

AC SETUP REQUIREMENTS FOR 74F175A

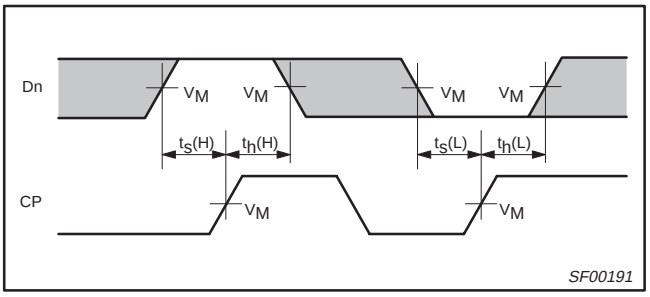
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = 25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	3.0 4.0			3.5 5.0		4.0 5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	3.5			3.5		4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	4.0			4.5		5.0		ns

AC WAVEFORMS

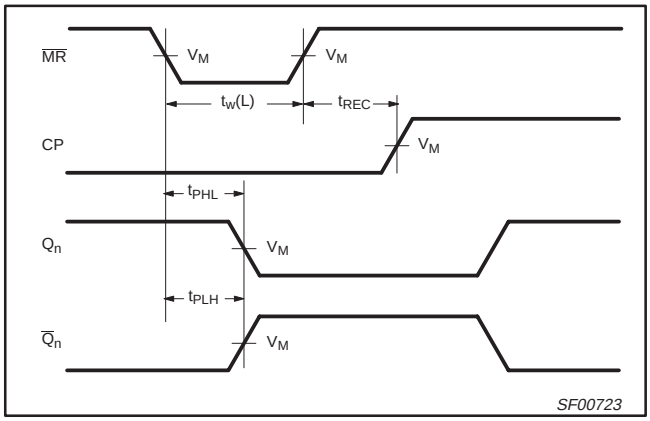
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency

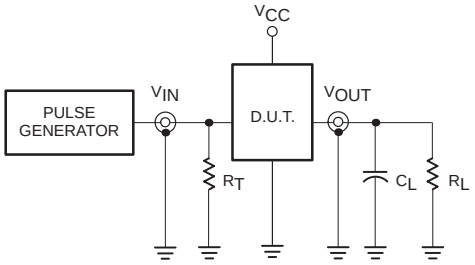


Waveform 2. Data setup time and hold times

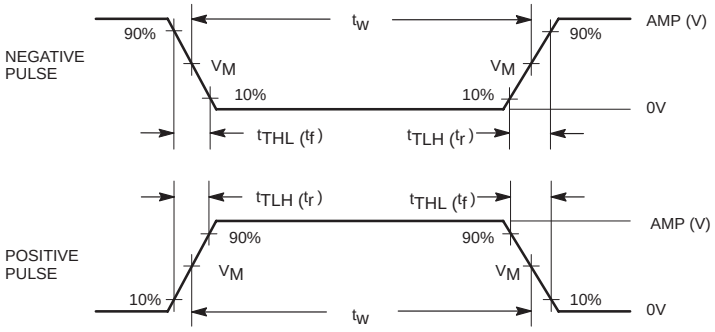


Waveform 3. Master Reset pulse width, Master Reset to output delay and Master Reset to Clock recovery time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

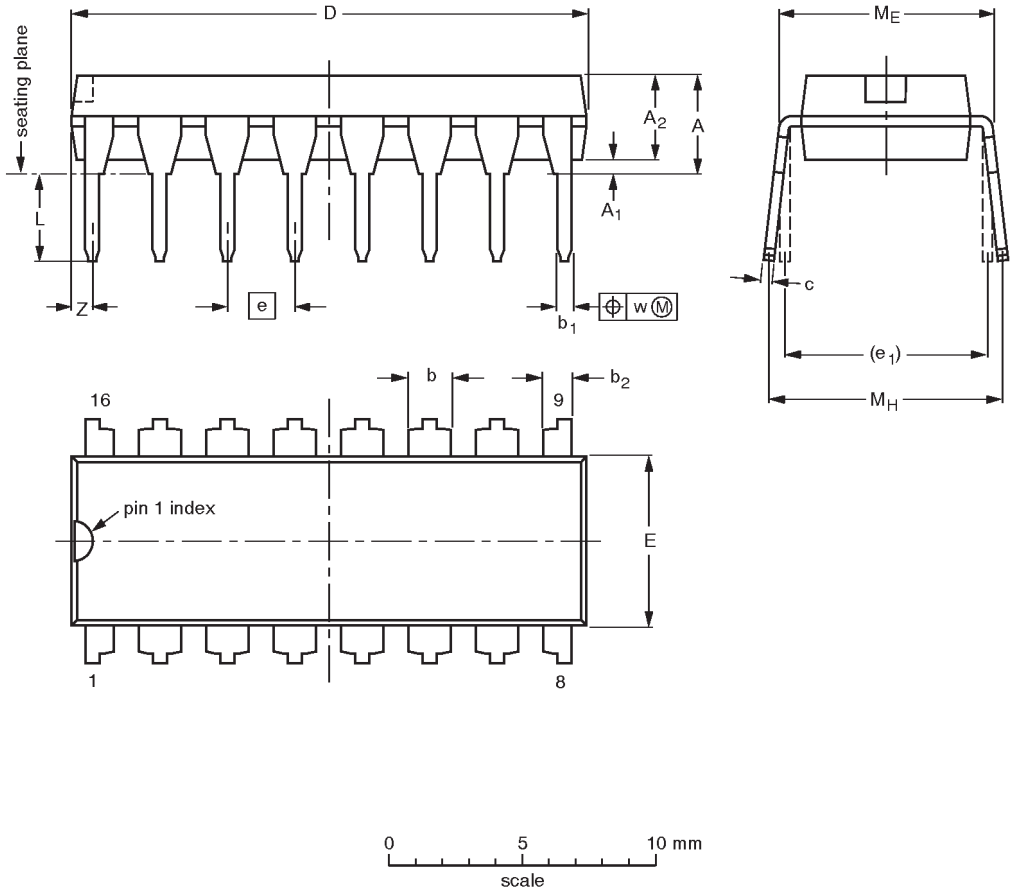
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

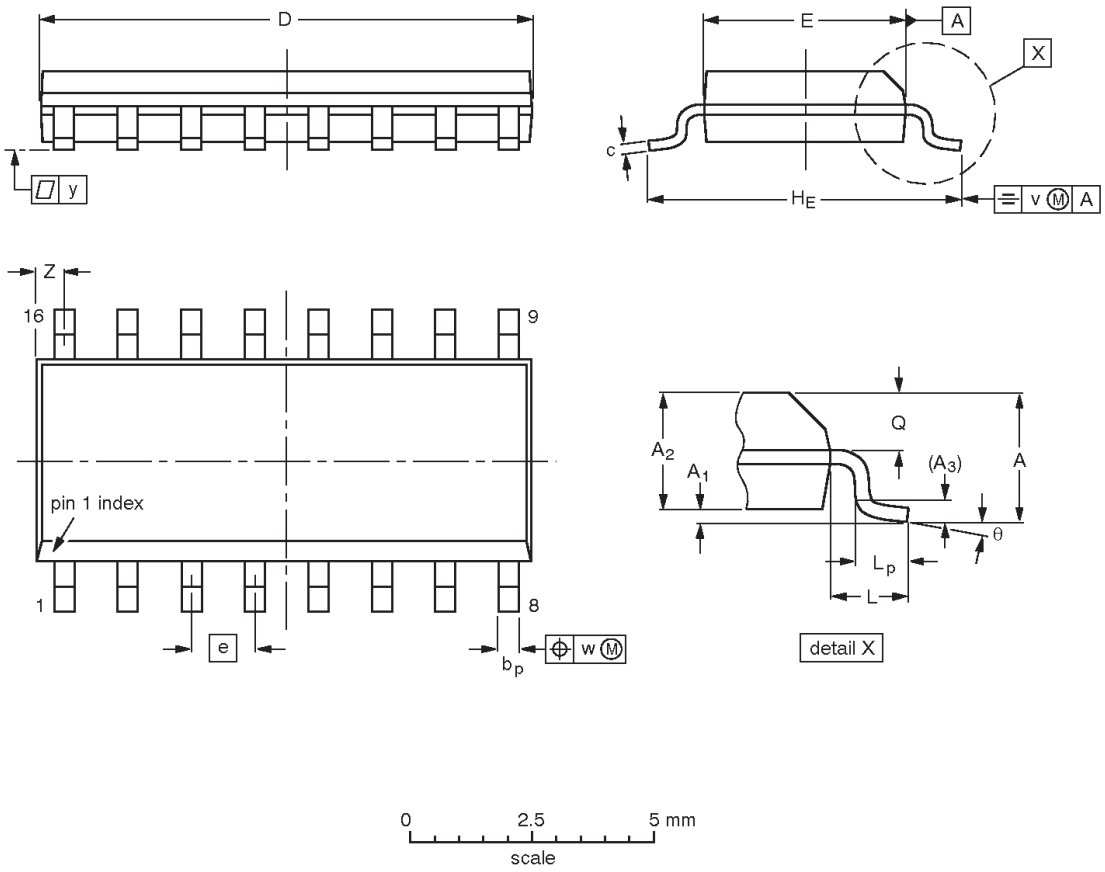
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

** Discontinued part. Please see the Discontinued Product List.*

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

** Discontinued part. Please see the Discontinued Product List.*

NOTES

** Discontinued part. Please see the Discontinued Product List.*

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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