MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate

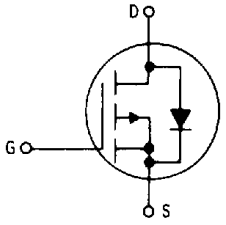
MTP5P25

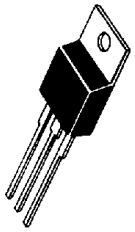
TMOS POWER FET
5 AMPERES
$R_{DS(on)}$ = 3 OHMS
250 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and motor drives.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$, and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS®





CASE 221A-06
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	5 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67		°C/W
Junction to Ambient	$R_{\theta JA}$	30	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	0.2 1	mAdc

This document contains information on a new product. Specifications and information herein are subject to change without notice.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$R_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 16 15	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	1600	pF
Output Capacitance	C_{oss}	—	400	
Reverse Transfer Capacitance	C_{rss}	—	250	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time	$t_{d(on)}$	—	40	ns
Rise Time	t_r	—	70	
Turn-Off Delay Time	$t_{d(off)}$	—	90	
Fall Time	t_f	—	60	
Total Gate Charge	Q_g	15 (Typ)	30	nC
Gate-Source Charge	Q_{gs}	5 (Typ)	—	
Gate-Drain Charge	Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage	V_{SD}	3 (Typ)	5	Vdc
Forward Turn-On Time	t_{on}	180 (Typ)	—	ns
Reverse Recovery Time	t_{rr}	200 (Typ)	—	ns

	Test Conditions
Input Capacitance, Output Capacitance, Reverse Transfer Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 14
Turn-On Delay Time, Rise Time, Turn-Off Delay Time, Fall Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 11, 12 and 13
Total Gate Charge, Gate-Source Charge, Gate-Drain Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 10
Forward On-Voltage, Forward Turn-On Time, Reverse Recovery Time	(I_S = Rated I_D V_{GS} = 0)

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

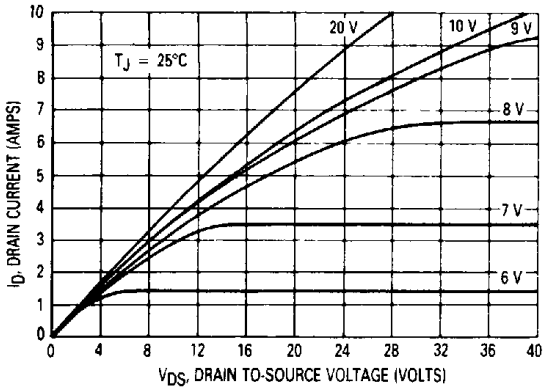


Figure 1. On-Region Characteristics

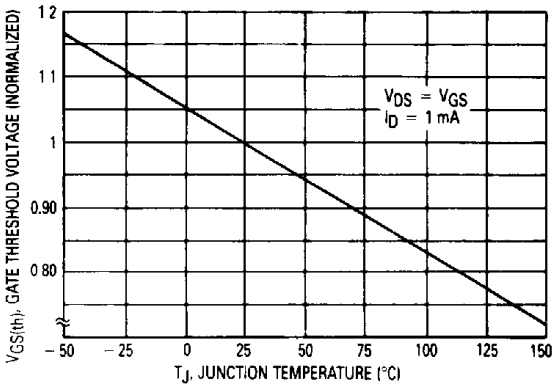


Figure 2. Gate-Threshold Voltage Variation With Temperature

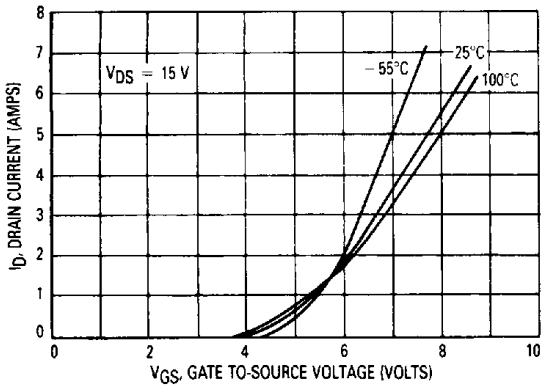


Figure 3. Transfer Characteristics

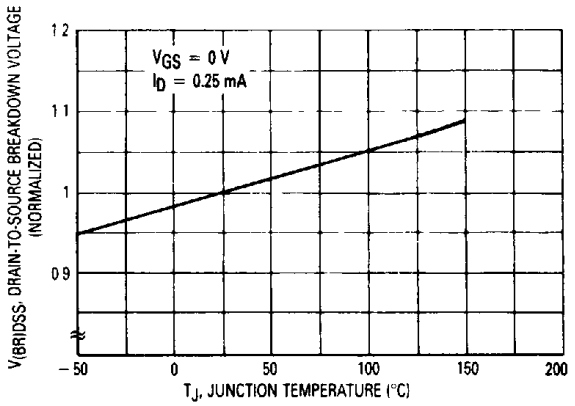


Figure 4. Drain-To-Source Breakdown Voltage Variation With Temperature

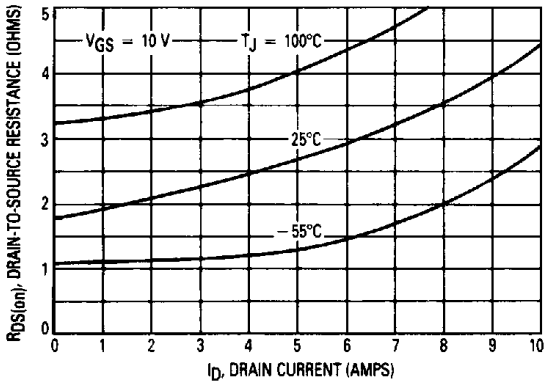


Figure 5. On-Resistance versus Drain Current

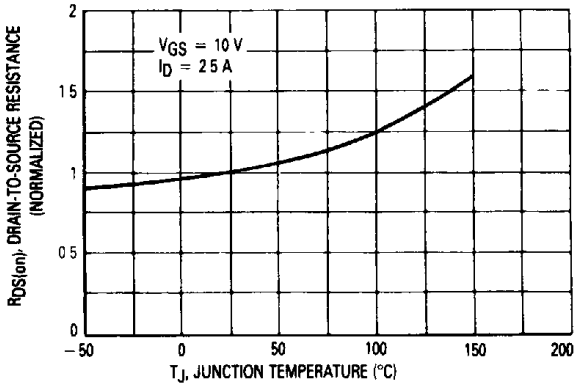


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

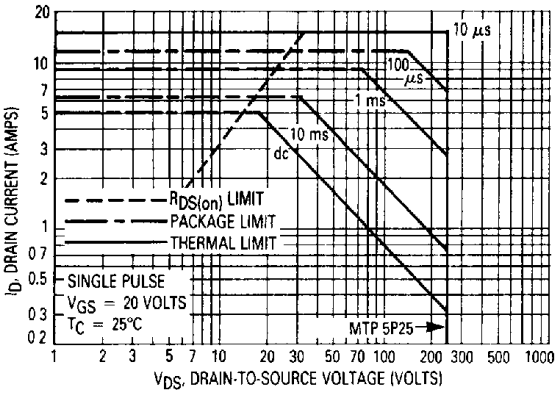


Figure 7. Maximum Rated Forward Bias Safe Operating Area

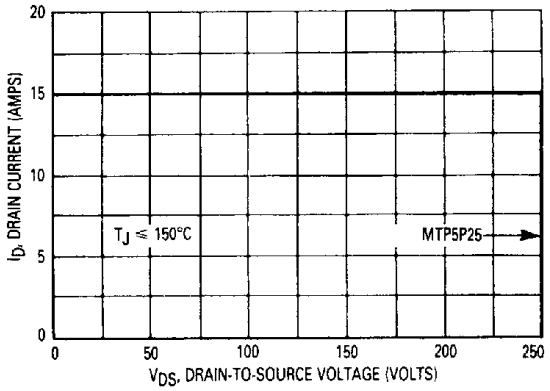


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

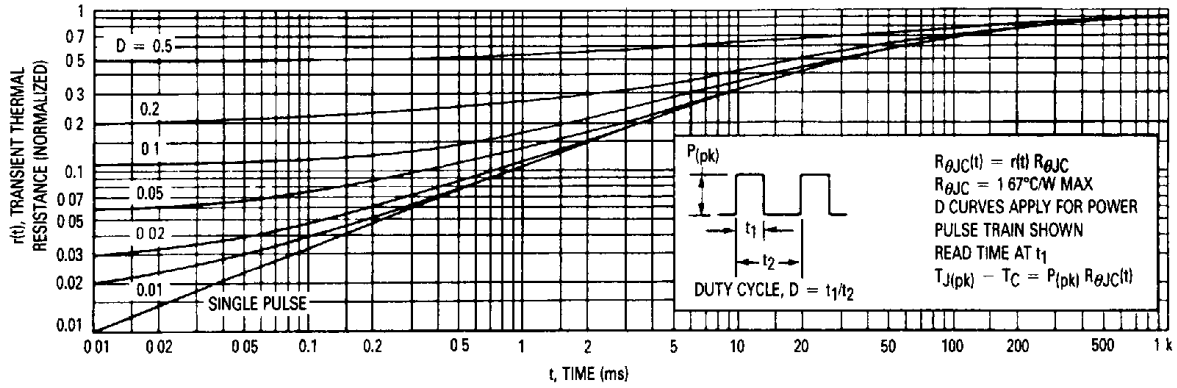


Figure 9. Thermal Response

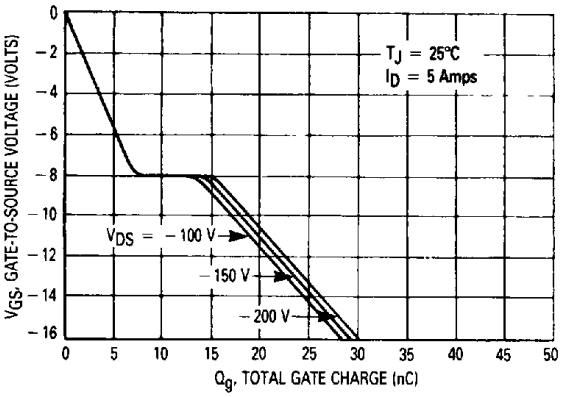


Figure 10. Gate Charge versus Gate-To-Source Voltage

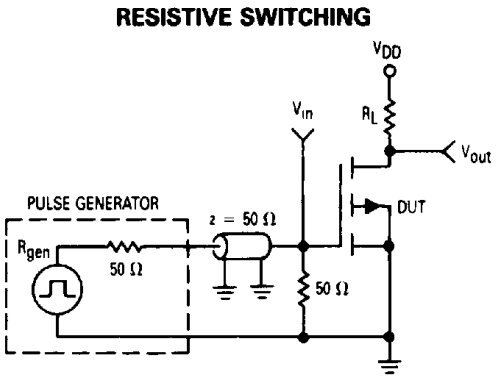


Figure 11. Switching Test Circuit

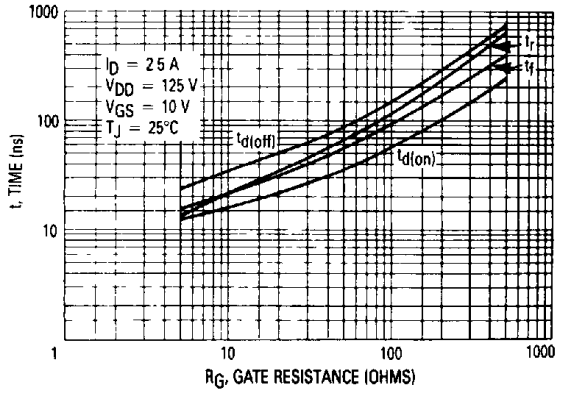


Figure 12. Resistive Switching versus Gate Resistance

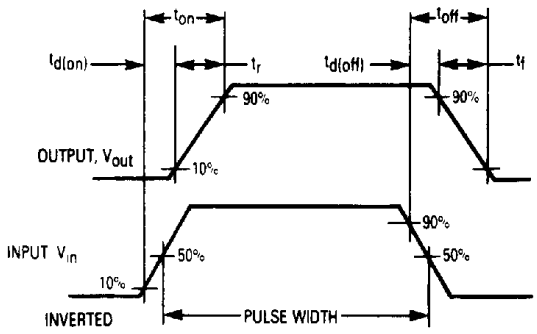


Figure 13. Switching Waveforms

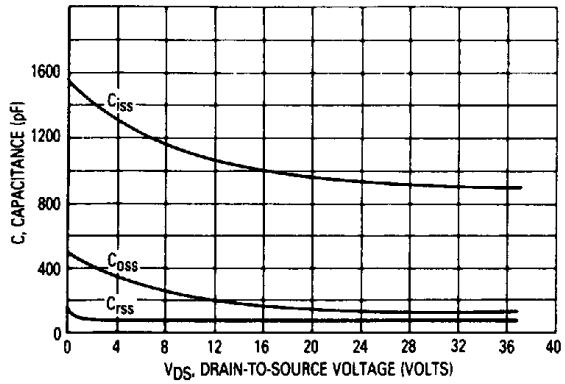


Figure 14. Capacitance Variation