



Frequency Timing Generator for PENTIUM II Systems

General Description

The ICS9250-09 is a main clock synthesizer chip for Pentium II based systems using Rambus Interface DRAMs. This chip provides all the clocks required for such a system when used with a Direct Rambus Clock Generator(DRCG) chip such as the ICS9211-01.

Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-09 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

The CPU/2 clocks are inputs to the DRCG.

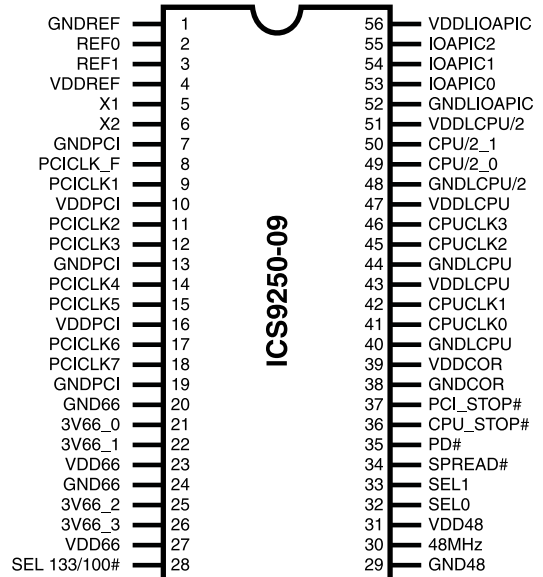
Key Specification

- CPU Output Jitter: <250ps
- CPU/2 Output Jitter: <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- Ref Output Jitter: <1000ps
- CPU Output Skew: <175ps
- CPU/2 Output Skew: <175ps
- IOAPIC Output Skew <250ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <250ps
- CPU to 3V66 Output Offset: 0.0 - 1.5ns (CPU leads)
- 3V66 to PCI Output Offset: 1.5 - 4.0ns (3V66 leads)
- CPU to IOAPIC Output Offset 1.5 - 4.0ns (CPU leads)

Features

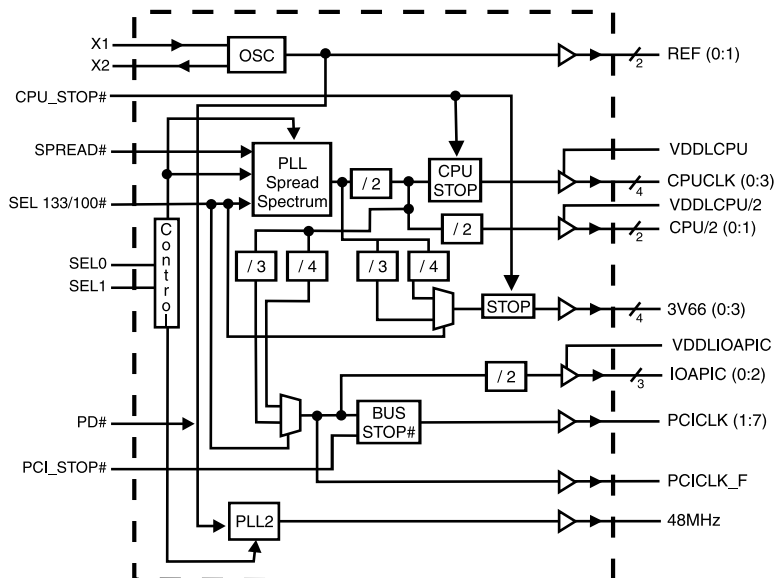
- Generates the following system clocks:
 - 4 CPU clocks (2.5V, 100/133MHz)
 - 8 PCI clocks, including 1 free-running (3.3V, 33MHz)
 - 2 CPU/2 clocks (2.5V, 50/66MHz)
 - 3 IOAPIC clocks (2.5V, 16.67MHz)
 - 4 Fixed frequency 66MHz clocks(3.3V, 66MHz)
 - 2 REF clocks(3.3V, 14.318MHz)
 - 1 USB clock (3.3V, 48MHz)
- Efficient power management through PD#, CPU_STOP# and PCI_STOP#.
- 0.5% typical down spread modulation on CPU, PCI, IOAPIC, 3V66 and CPU/2 output clocks.
- Uses external 14.318MHz crystal.

Pin Configuration



56-pin SSOP

Block Diagram





Pin Descriptions

| Pin number | Pin name | Type | Description |
|---------------------------|--------------|------|---|
| 1 | GNDREF | PWR | Gnd pin for REF clocks |
| 2, 3 | REF(0:1) | OUT | 14.318MHz reference clock outputs at 3.3V |
| 4 | VDDREF | PWR | Power pin for REF clocks |
| 5 | X1 | IN | XTAL_IN 14.318MHz crystal input |
| 6 | X2 | OUT | XTAL_OUT Crystal output |
| 7, 13, 19 | GNDPCI | PWR | Gnd pin for PCICLKs |
| 8 | PCICLK_F | OUT | Free running PCI clock at 3.3V. Synchronous to CPU clocks. Not affected by the PCI_STOP# input. |
| 9, 11, 12, 14, 15, 17, 18 | PCICLK[1:7] | OUT | PCI clock outputs at 3.3V. Synchronous to CPU clocks. |
| 10, 16 | VDDPCI | PWR | 3.3Volts power pin for PCICLKs |
| 20, 24 | GND66 | PWR | Gnd pin for 3V66 outputs |
| 21, 22, 25, 26 | 3V66[0:3] | OUT | 66MHz outputs at 3.3V. These outputs are stopped when CPU_STOP# is driven active.. |
| 23, 27 | VDD66 | PWR | power pin for the 3V66 clocks. |
| 28 | SEL 133/100# | IN | This selects the frequency for the CPU and CPU/2 outputs. High = 133MHz, Low=100MHz |
| 29 | GND48 | PWR | Ground pin for the 48MHz output |
| 30 | 48MHz | OUT | Fixed 48MHz clock output. 3.3V |
| 31 | VDD48 | PWR | Power pin for the 48MHz output. |
| 32, 33 | SEL[0:1] | IN | Function select pins. See truth table for details. |
| 34 | SPREAD# | IN | Enables spread spectrum when active(Low). modulates all the CPU, PCI, IOAPIC, 3V66 and CPU/2 clocks. Does not affect the REF and 48MHz clocks. 0.5% down spread modulation. |
| 35 | PD# | IN | This asynchronous input powers down the chip when drive active(Low). The internal PLLs are disabled and all the output clocks are held at a Low state. |
| 36 | CPU_STOP# | IN | This asynchronous input halts the CPUCLK[0:3] and the 3V66[0:3] clocks at logic "0" when driven active(Low). Does not affect the CPU/2 clocks. |
| 37 | PCI_STOP# | IN | This asynchronous input halts the PCICLK[1:7] at logic"0" when driven active(Low). PCICLK_F is not affected by this input. |
| 38 | GNDCOR | PWR | Ground pin for the PLL core |
| 39 | VDDCOR | PWR | Power pin for the PLL core. 3.3V |
| 43, 47 | VDDLCPU | PWR | Power pin for the CPUCLKs. 2.5V |
| 40, 44 | GNDLCPU | PWR | Ground pin for the CPUCLKs |
| 41, 42, 45, 46 | CPUCLK[0:3] | OUT | Host bus clock output at 2.5V. 133MHz or 100MHz depending on the state of the SEL 133/100MHz. |
| 48 | GNDLCPU/2 | PWR | Ground pin for the CPU/2 clocks. |
| 49, 50 | CPU/2[0:1] | OUT | 2.5V clock outputs at 1/2 CPU frequency. 66MHz or 50MHz depending on the state of the SEL 133/100# input pin. |
| 51 | VDDLCPU/2 | PWR | Power pin for the CPU/2 clocks. 2.5V |
| 52 | GNDLIOAPIC | PWR | Ground pin for the IOAPIC outputs. |
| 53, 54, 55 | IOAPIC[0:2] | OUT | IOAPIC clocks at 2.5V. Synchronous with CPUCLKs but fixed at 16.67MHz. |
| 56 | VDDLIOAPIC | PWR | Power pin for the IOAPIC outputs. 2.5V. |



Frequency Select:

| SEL 133/100-# | SEL1 | SEL0 | CPU MHz | CPU/2 MHz | 3V66 MHz | PCI MHz | 48 MHz | REF MHz | IOAPIC MHz | Comments |
|---------------|------|------|---------|-----------|----------|---------|--------|---------|------------|--------------------|
| 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Tri-state |
| 0 | 0 | 1 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Reserved |
| 0 | 1 | 0 | 100.00 | 50.00 | 66.67 | 33.33 | Hi-Z | 14.318 | 16.67 | 48MHz PLL disabled |
| 0 | 1 | 1 | 100.00 | 50.00 | 66.67 | 33.33 | 48 | 14.318 | 16.67 | |
| 1 | 0 | 0 | TCLK/2 | TCLK/4 | TCLK/4 | TCLK/8 | TCLK/2 | TCLK | TCLK/16 | Test mode (1) |
| 1 | 0 | 1 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | Reserved |
| 1 | 1 | 0 | 133.32 | 66.67 | 66.67 | 33.33 | Hi-Z | 14.318 | 16.67 | |
| 1 | 1 | 1 | 133.32 | 66.67 | 66.67 | 33.33 | 48 | 14.318 | 16.67 | |

Note:

1. TCLK is a test clock driven on the x1 input during test mode.

Power Management Features:

| CPU_STOP# | PD# | PCI_STOP# | CPUCLK | CPU/2 | IOAPIC | 3V66 | PCI | PCI_F | REF 48MHz | Osc | VCOs |
|-----------|-----|-----------|--------|-------|--------|------|-----|-------|-----------|-----|------|
| X | 0 | X | LOW | LOW | LOW | LOW | LOW | LOW | LOW | OFF | OFF |
| 0 | 1 | 0 | LOW | ON | ON | LOW | LOW | ON | ON | ON | ON |
| 0 | 1 | 1 | LOW | ON | ON | LOW | ON | ON | ON | ON | ON |
| 1 | 1 | 0 | ON | ON | ON | ON | LOW | ON | ON | ON | ON |
| 1 | 1 | 1 | ON | ON | ON | ON | ON | ON | ON | ON | ON |

Note:

1. LOW means outputs held static LOW as per latency requirement next page.
2. On means active.
3. PD# pulled Low, impacts all outputs including REF and 48 MHz outputs.
4. All 3V66 as well as all CPU clocks should stop cleanly when CPU_STOP# is pulled LOW.
5. CPU/2, IOAPIC, REF, 48 MHz signals are not controlled by the CPU_STOP# functionality and are enabled all in all conditions except PD# = LOW



Power Management Requirements:

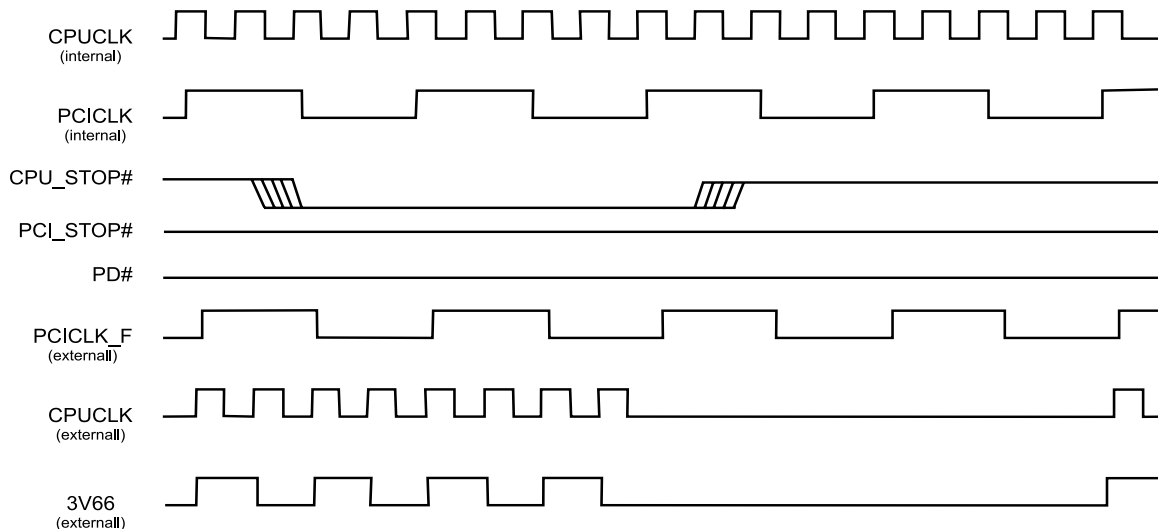
| Signal | Signal State | Latency |
|-----------|----------------------|-------------------------------|
| | | No. of rising edges of PCICLK |
| CPU_STOP | 0 (disabled) | 1 |
| | 1 (enabled) | 1 |
| PCI_STOP# | 0 (disabled) | 1 |
| | 1 (enabled) | 1 |
| PD# | 1 (normal operation) | 3mS |
| | 0 (power down) | 2max. |

Note:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high to when the first valid clocks are driven from the device).

CPU_STOP# Timing Diagram

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU and 3V66 clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU clock) and must be internally synchronized to the external output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. **ONLY one rising edge of PCICLK_F is allowed** after the clock control logic switched for both the CPU and 3V66 outputs to become enabled/disabled.



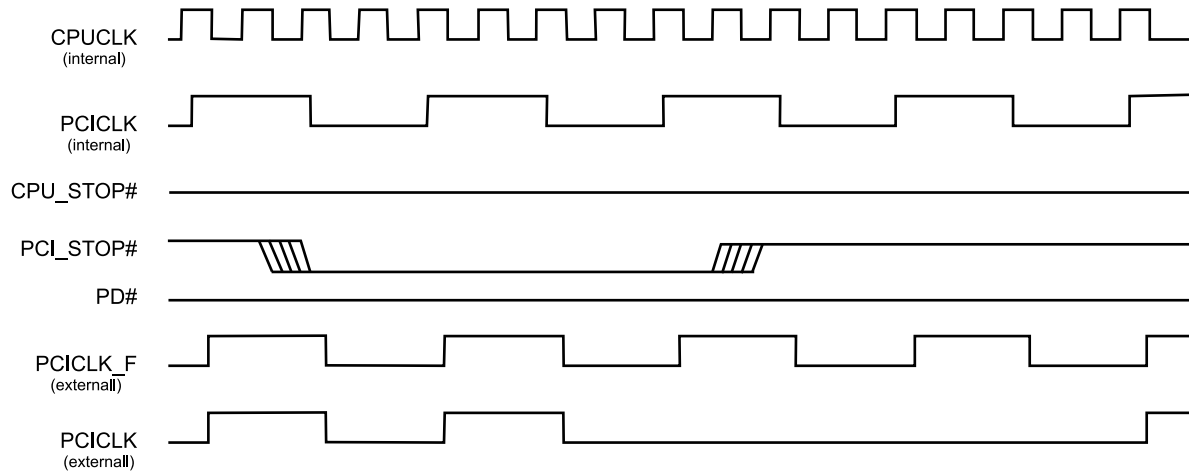
Notes:

1. All timing is referenced to the internal CPUCLK.
2. The internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. CPU_STOP# signal is an input signal that must be made synchronous to free running PCICLK_F
4. 3V66 clocks also stop/start before
5. PD# and PCI_STOP# are shown in a high state.
6. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz



PCI_STOP# Timing Diagram

PCI_STOP# is an input to the clock synthesizer and must be made synchronous to the clock driver PCICLK_F output. It is used to turn off the PCI clocks for low power operation. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. **ONLY one rising edge of PCICLK_F is allowed** after the clock control logic switched for the PCI outputs to become enabled/disabled.



Notes:

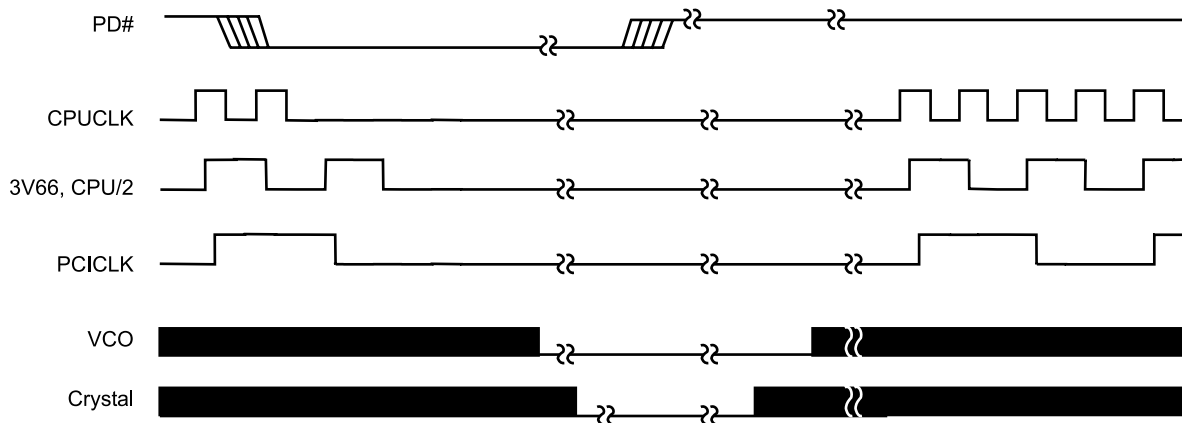
1. All timing is referenced to CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCICLK_F output.
3. Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PD# and CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9250 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



Absolute Maximum Ratings

- Supply Voltage 7.0 V
- Logic Inputs GND–0.5 V to V_{DD}+0.5 V
- Ambient Operating Temperature 0°C to +70°C
- Storage Temperature –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Offset

| Group | Offset | Measurement Loads | Measure Points |
|---------------|----------------------|---------------------------|----------------------------|
| CPU to 3V66 | 0.0-1.5ns CPU leads | CPU @ 20pF, 3V66 @ 30pF | CPU @ 1.25V, 3V66 @ 1.5V |
| 3V66 to PCI | 1.5-4.0ns 3V66 leads | 3V66 @ 30pF, PCI @ 30pF | 3V66 @ 1.5V, PCI @ 1.5V |
| CPU to IOAPIC | 1.5-4.0ns CPU leads | CPU @ 20pF, IOAPIC @ 20pF | CPU @ 1.25V, IOAPIC @ 1.5V |

Note: 1. All offsets are to be measured at rising edges.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70° C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | µA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | µA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | µA |
| Operating Supply Current | I _{DD3.3OP100} | Select @ 100MHz; Max discrete cap loads | | 68 | 180 | mA |
| | I _{DD3.3OP133} | Select @ 133MHz; Max discrete cap loads | | 80 | | |
| Power Down Supply Current | I _{DD3.3PD} | C _L = 0 pF; PWRDWN# = 0 | | 62 | 200 | uA |
| Input frequency | F _i | V _{DD} = 3.3 V | 12 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T _{Trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Settling Time ¹ | T _S | From 1st crossing to 1% target Freq. | | 1 | | ms |
| Clk Stabilization ¹ | T _{Stab} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70° C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|---|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.5OP66} | Select @ 100MHz; Max discrete cap loads | | 19 | 25 | mA |
| | I _{DD2.5OP100} | Select @ 133MHz; Max discrete cap loads | | 22 | | |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|---------------------------|---|------|------|------|-------|
| Output High Voltage | V_{OH2B} | $I_{OH} = -12.0\text{ mA}$ | 2 | 2.2 | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 12\text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH} = 1.7\text{ V}$ | | -35 | -19 | mA |
| Output Low Current | I_{OL2B} | $V_{OL} = 0.7\text{ V}$ | 19 | 27 | | mA |
| Rise Time | t_{r2B}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$ | 0.4 | 1.2 | 1.6 | ns |
| Fall Time | t_{f2B}^1 | $V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.4 | 1.25 | 1.6 | ns |
| Duty Cycle | d_{t2B}^1 | $V_T = 1.25\text{ V}$ | 45 | 48 | 55 | % |
| Skew | t_{sk2B}^1 | $V_T = 1.25\text{ V}$ | | 80 | 175 | ps |
| Jitter, One Sigma | $t_{j1\sigma2B}^1$ | $V_T = 1.25\text{ V}$ | | 20 | 150 | ps |
| Jitter, Absolute | t_{jabs2B}^1 | $V_T = 1.25\text{ V}$ | -250 | 61 | +250 | ps |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc}2B}^1$ | $V_T = 1.25\text{ V}$ | | 150 | 250 | ps |

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Electrical Characteristics - CPU/2

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|---------------------------|---|------|-----|------|-------|
| Output High Voltage | V_{OH2B} | $I_{OH} = -12.0\text{ mA}$ | 2 | 2.3 | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 12\text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH} = 1.7\text{ V}$ | | -35 | -19 | mA |
| Output Low Current | I_{OL2B} | $V_{OL} = 0.7\text{ V}$ | 19 | 27 | | mA |
| Rise Time | t_{r2B}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$ | 0.4 | 1.1 | 1.6 | ns |
| Fall Time | t_{f2B}^1 | $V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.4 | 1 | 1.6 | ns |
| Duty Cycle | d_{t2B}^1 | $V_T = 1.25\text{ V}$ | 45 | 48 | 55 | % |
| Jitter, One Sigma | $t_{j1\sigma2B}^1$ | $V_T = 1.25\text{ V}$ | | 20 | 150 | ps |
| Jitter, Absolute | t_{jabs2B}^1 | $V_T = 1.25\text{ V}$ | -250 | 70 | +250 | ps |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc}2B}^1$ | $V_T = 1.25\text{ V}$ | | 100 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------|---|------|------|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -11\text{ mA}$ | 2.4 | 3.1 | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 9.4\text{ mA}$ | | 0.25 | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0\text{ V}$ | | -60 | -22 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8\text{ V}$ | 25 | 44 | | mA |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 0.5 | 1.6 | 2 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.5 | 1.3 | 2 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 48 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V}$ | | 120 | 175 | ps |
| Jitter, One Sigma ¹ | $t_{j1\sigma1}$ | $V_T = 1.5\text{ V}$ | | 43 | 150 | ps |
| Jitter, Absolute ¹ | t_{jabs1} | $V_T = 1.5\text{ V}$ | -250 | 100 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jeyc-cycl1}$ | $V_T = 1.5\text{ V}$ | | 150 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 60\text{ pF}$ for PCI0 & PCI1, $C_L = 30\text{ pF}$ for other PCIs

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------|---|------|-----|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -11\text{ mA}$ | 2.4 | 3.1 | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 9.4\text{ mA}$ | | 0.2 | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0\text{ V}$ | | -60 | -22 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8\text{ V}$ | 25 | 45 | | mA |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 0.5 | 1.7 | 2 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.5 | 1.6 | 2 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 50 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V}$ | | 360 | 500 | ps |
| Jitter, One Sigma ¹ | $t_{j1\sigma1}$ | $V_T = 1.5\text{ V}$ | | 18 | 150 | ps |
| Jitter, Absolute ¹ | t_{jabs1} | $V_T = 1.5\text{ V}$ | -250 | 80 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jeyc-cycl1}$ | $V_T = 1.5\text{ V}$ | | 155 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 48MHz, REF

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------------|---|-----|-----|------|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -12\text{ mA}$ | 2.6 | 2.9 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9\text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0\text{ V}$ | | -35 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8\text{ V}$ | 17 | 23 | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$, 48MHz | | 2 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$, 48MHz | | 2 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{ V}$, 48MHz | 45 | 50 | 55 | % |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$, REF | | 2.2 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$, REF | | 1.9 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{ V}$, REF | 45 | 52 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $t_{j\text{cyc-cyc}5}$ | $V_T = 1.5\text{ V}$, 48MHz | | 200 | 500 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{j\text{cyc-cyc}5}$ | $V_T = 1.5\text{ V}$, REF | | 800 | 1000 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-------------------------|---|------|------|-----|-------|
| Output High Voltage | V_{OH4B} | $I_{OH} = -12\text{ mA}$ | 2 | 2.23 | | V |
| Output Low Voltage | V_{OL4B} | $I_{OL} = 12\text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH4B} | $V_{OH} = 1.7\text{ V}$ | | -36 | -16 | mA |
| Output Low Current | I_{OL4B} | $V_{OL} = 0.7\text{ V}$ | 19 | 26 | | mA |
| Rise Time ¹ | T_{r4B} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$ | 0.4 | 1.3 | 1.6 | ns |
| Fall Time ¹ | T_{f4B} | $V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.4 | 1.25 | 1.6 | ns |
| Duty Cycle ¹ | D_{t4B} | $V_T = 1.25\text{ V}$ | 45 | 49 | 55 | % |
| Jitter, One Sigma ¹ | $T_{j1\sigma 4B}$ | $V_T = 1.25\text{ V}$ | | 14 | 150 | ps |
| Jitter, Absolute ¹ | $T_{j\text{abs}4B}$ | $V_T = 1.25\text{ V}$ | -250 | 65 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{j\text{cyc-cyc}4B}$ | $V_T = 1.25\text{ V}$ | | 87 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



General Layout Precautions:

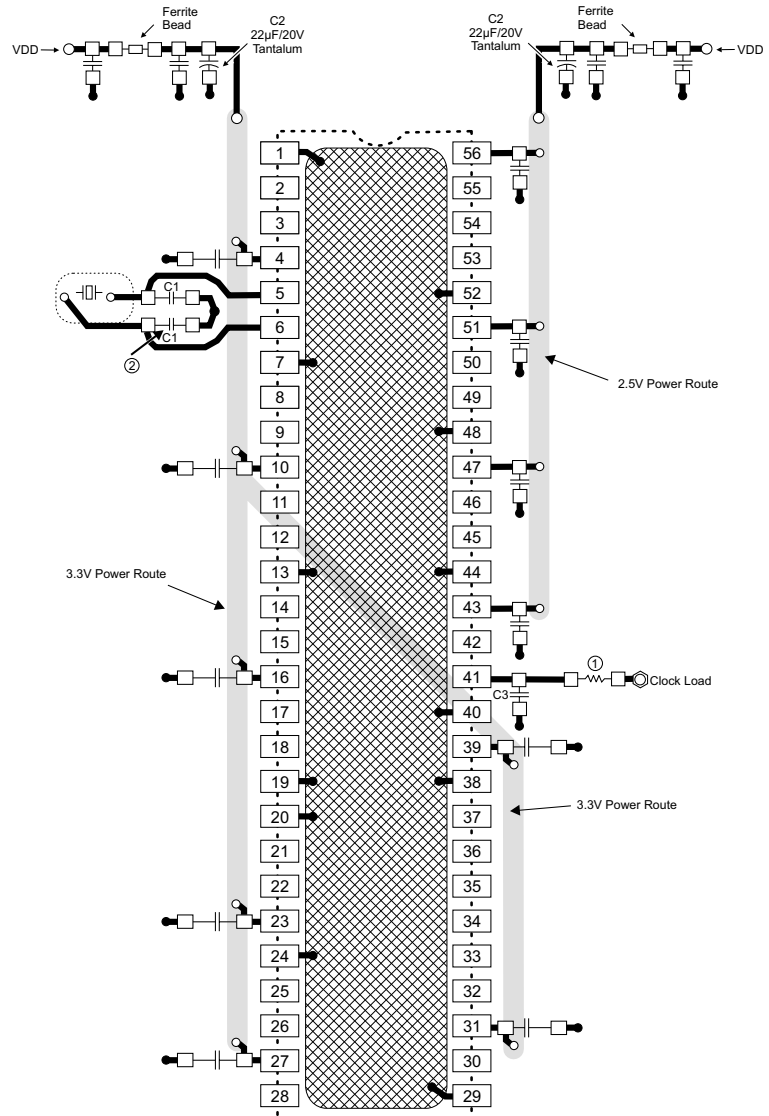
- 1) Use a ground plane on the top routing layer of the PCB in all areas not used by traces.
- 2) Make all power traces and ground traces as wide as the via pad for lower inductance.

Notes:

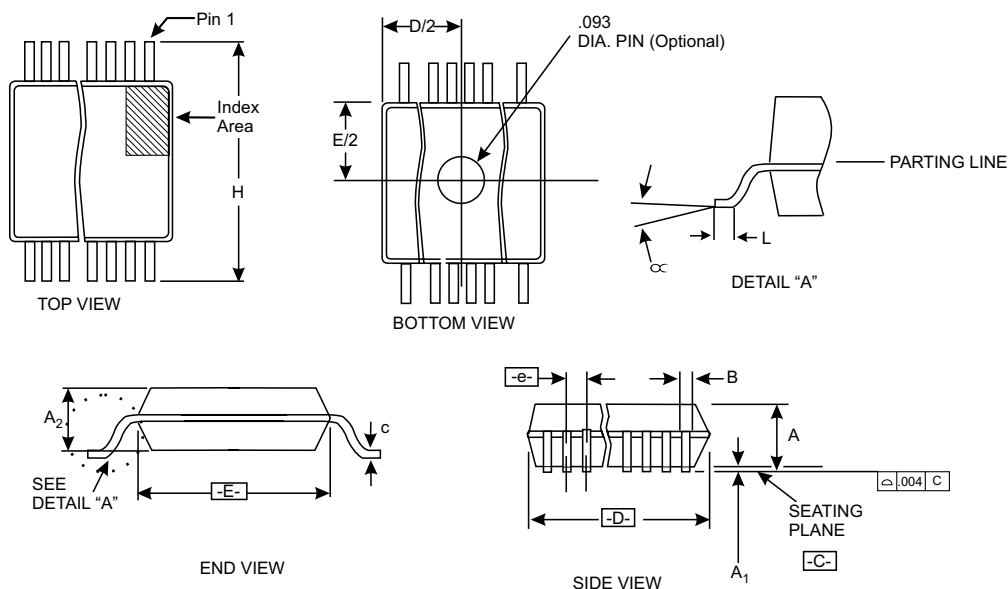
- ① All clock outputs should have provisions for a 15pf capacitor between the clock output and series terminating resistor. Not shown in all places to improve readability of diagram.
- ② Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.

Connections to VDD:

- Best
- Okay
- Avoid
- Avoid



- = Routed Power
- = Ground Connection Key (component side copper)
- = Ground Plane Connection
- = Power Route Connection
- = Solder Pads
- = Clock Load



| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | N |
|--------|-------------------|------|-------|---|------|------|------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .102 | .110 | AD | .720 | .725 | .730 | 56 |
| A1 | .008 | .012 | .016 | "For current dimensional specifications, see JEDEC 95." Dimensions in inches | | | | |
| A2 | .087 | .090 | .094 | | | | | |
| B | .008 | - | .0135 | | | | | |
| c | .005 | - | .010 | | | | | |
| D | See Variations | | | | | | | |
| E | .291 | .295 | .299 | | | | | |
| e | 0.025 BSC | | | | | | | |
| H | .395 | - | .420 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .020 | - | .040 | | | | | |
| N | See Variations | | | | | | | |
| ∞ | 0° | - | 8° | | | | | |

56 Pin 300 mil SSOP Package

Ordering Information

ICS9250yF-09-T

Example:

ICS XXXX y F - PPP - T

- Prefix
ICS, AV = Standard Device
- Device Type (consists of 3 or 4 digit numbers)
- Revision Designator (will not correlate with datasheet revision)
- Package Type
F=SSOP
- Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- Designation for tape and reel packaging