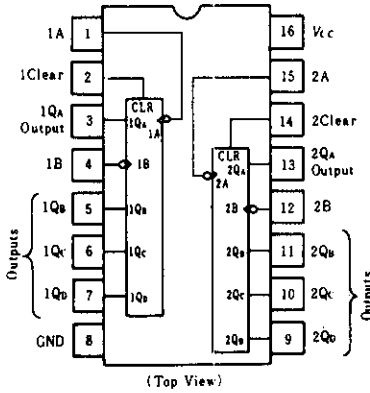


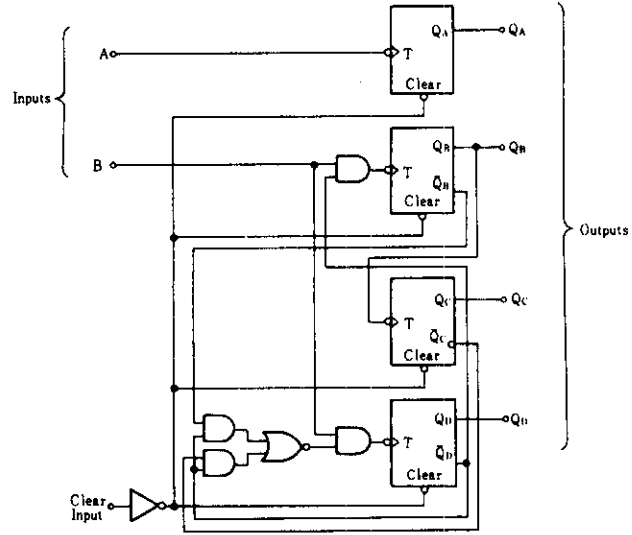
# HD74LS390 • Dual Decade Counters

This circuit contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters. The HD74LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage.

## ■ PIN ARRANGEMENT



## ■ BLOCK DIAGRAM (1/2)



## ■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	
Output current	$I_{OH}$	—	—	-400	$\mu A$	
Output current	$I_{OL}$	—	—	8	mA	
Count frequency	Input A	$f_{count}$	0	—	25	MHz
	Input B		0	—	20	
Pulse width	Input A	$t_w$	20	—	—	ns
	Input B		25	—	—	
	Clear		20	—	—	
Setup time	$t_{su}$	25	—	—	ns	

†; The arrow indicates that the falling edge of the clock pulse is used for reference.

## ■ FUNCTION TABLE

### ● BCD Count Sequence (Notes 1)

Count	Outputs			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

### ● Bi-Quinary (Notes 2)

Count	Outputs			
	$Q_A$	$Q_D$	$Q_C$	$Q_B$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

### Notes)

1. Output  $Q_A$  is connected to input B for BCD count.
2. Output  $Q_D$  is connected to input A for bi-quinary count.
3. H; high level, L; low level, X; irrelevant

## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	Clear	7	V
	A, B	5.5	V
Operating temperature range	$T_{op}$	-20 ~ +75	$^{\circ}C$
Storage temperature range	$T_{stg}$	-65 ~ +150	$^{\circ}C$

# HD74LS390

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$		—	—	0.8	V	
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.7	—	—	V	
	$V_{OL}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$				V	
Input current	Clear				0.1	mA	
	Input A	$V_{CC} = 5.25\text{V}$			0.2		
	Input B				0.4		
	Clear				20	$\mu\text{A}$	
	Input A	$V_{CC} = 5.25\text{V}$ , $V_I = 2.7\text{V}$			100		
	Input B				200		
	Clear				-0.4	mA	
	Input A	$V_{CC} = 5.25\text{V}$ , $V_I = 0.4\text{V}$			-1.6		
	Input B				-2.4		
	Short-circuit output current	$I_{OS}$	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA
	Supply current	$I_{CC}^{**}$	$V_{CC} = 5.25\text{V}$	—	15	26	mA
	Input clamp voltage	$V_{IA}$	$V_{CC} = 4.75\text{V}$ , $I_{IN} = -18\text{mA}$	—	—	-1.5	V

\*  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

\*\*  $I_{CC}$  is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## ■ SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{V}$ , $T_a = 25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	$f_{max}$	A	$Q_A$	$C_L = 15\text{pF}$ , $R_L = 2\text{k}\Omega$	25	35	—	MHz
		B	$Q_B$		20	30	—	
Propagation delay time	$t_{PLH}$	A	$Q_A$		—	12	20	ns
	$t_{PHL}$				—	13	20	
	$t_{PLH}$	A	$Q_C$		—	37	60	
	$t_{PHL}$				—	39	60	
	$t_{PLH}$	B	$Q_B$		—	13	21	
	$t_{PHL}$				—	14	21	
	$t_{PLH}$	B	$Q_C$		—	24	39	
	$t_{PHL}$				—	26	39	
	$t_{PLH}$	B	$Q_D$		—	13	21	
	$t_{PHL}$				—	14	21	
	$t_{PHL}$	Clear	Any	—	24	39		



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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