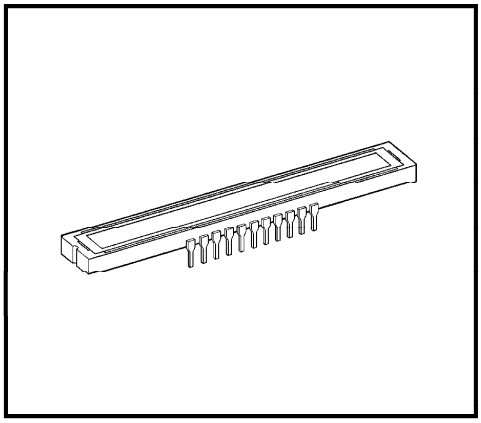
**TENTATIVE** TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

# TCD1702C

The TCD1702C is a high sensitive and low dark current 7500 elements CCD image sensor.
The sensor is designed for facsimile, imagescanner and OCR.
The device contains a row of 7500 elements photodiodes which provide a 24 lines / mm (600DPI) across a A3 size paper. The device is operated by 5V (pulse), and 12V power supply.



Weight : 6.6g (Typ.)

## FEATURES

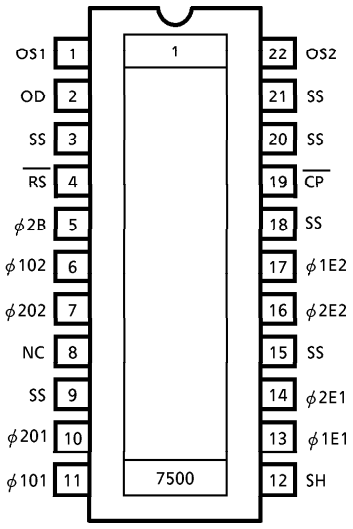
- Number of Image Sensing Elements : 7500 elements
- Image Sensing Element Size
  : 7$\mu$m by 7$\mu$m on 7$\mu$m centers
- Photo Sensing Region : High sensitive and low voltage dark signal pn photodiode
- Clock : 2 phase (5V)
- Package : 22pin DIP

## MAXIMUM RATINGS (Note 1)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Clock Pulse Voltage | $V_\phi$ | −0.3~8 | V |
| Shift Pulse Voltage | $V_{SH}$ | | |
| Reset Pulse Voltage | $V_{\overline{RS}}$ | | |
| Clamp Pulse Voltage | $V_{\overline{CP}}$ | | |
| Power Supply Voltage | $V_{OD}$ | −0.3~15 | |
| Operating Temperature | $T_{opr}$ | −25~60 | °C |
| Storage Temperature | $T_{stg}$ | −40~100 | °C |

(Note 1) All voltage are with respect to SS terminals (Ground).

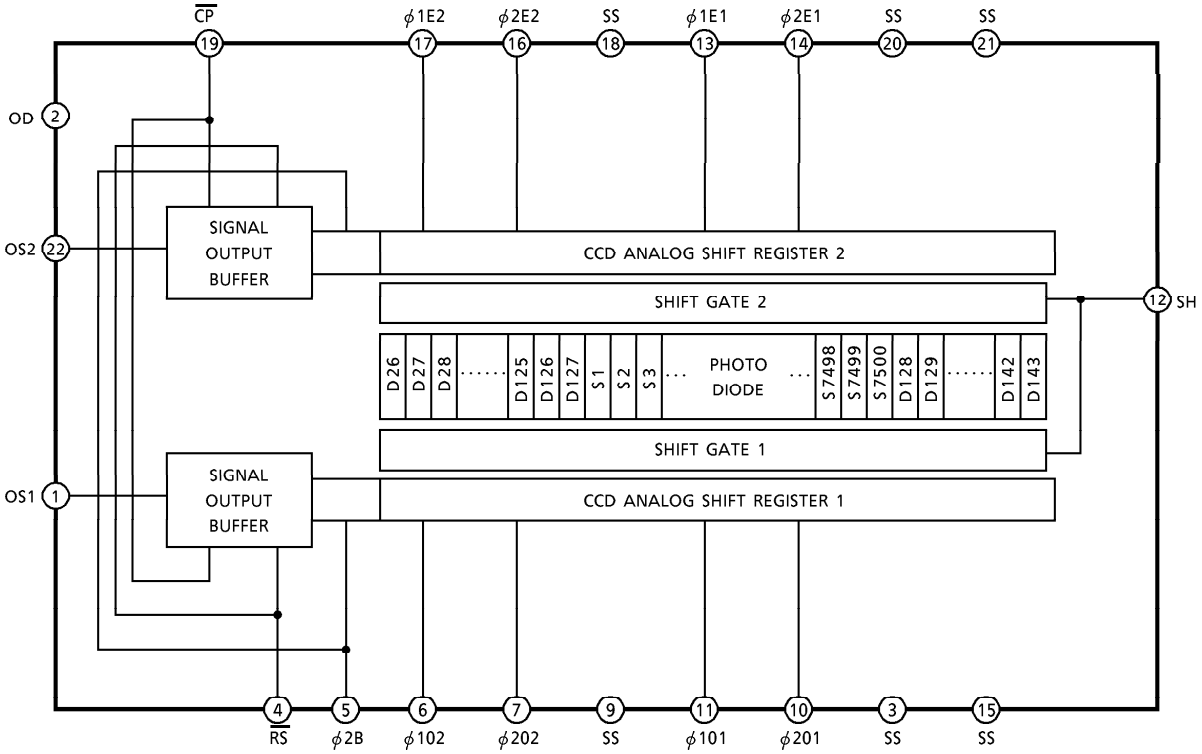
PIN CONNECTIONS




(TOP VIEW)

961001EBA2

## CIRCUIT DIAGRAM




## PIN NAME

| | |
|---|---|
| $\phi$1E, O | Clock (Phase 1) |
| $\phi$2E, O | Clock (Phase 2) |
| $\phi$2B | Final Stage Clock (Phase 2) |
| SH | Shift Gate |
| $\overline{RS}$ | Reset Gate |
| $\overline{CP}$ | Clamp Gate |
| OS1 | Signal Output 1 |
| OS2 | Signal Output 2 |
| OD | Power |
| SS | Ground |
| NC | Non Connection |

**OPTICAL / ELECTRICAL CHARACTERISTICS**

(Ta = 25°C, $V_{OD}$ = 12V, $V_\phi = V_{SH} = V_{\overline{RS}} = V_{\overline{CP}}$ = 5V, $f_\phi$ = 1MHz,
$t_{INT}$ (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP
LOAD RESISTANCE = 100kΩ)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Sensitivity | R | 7.2 | 9 | 10.8 | V / lx·s | |
| Photo Response Non Uniformity | PRNU | — | — | 10 | % | (Note 2) |
| | PRNU (3) | — | 4 | 8 | mV | (Note 8) |
| Saturation Output Voltage | $V_{SAT}$ | 1.5 | 2 | — | V | (Note 3) |
| Saturation Exposure | SE | 0.14 | 0.22 | — | lx·s | (Note 4) |
| Dark Signal Voltage | $V_{DRK}$ | — | 1 | 2.5 | mV | (Note 5) |
| Dark Signal Non Uniformity | DSNU | — | 1 | 2.5 | mV | (Note 5) |
| DC Power Dissipation | $P_D$ | — | 300 | 364 | mW | |
| Total Transfer Efficiency | TTE | 92 | — | — | % | |
| Output Impedance | $Z_o$ | — | 0.5 | 1 | kΩ | |
| Dynamic Range | DR | — | 2000 | — | — | (Note 6) |
| DC Signal Output Voltage | $V_{OS1}$ | 3.5 | 4.5 | 6 | V | (Note 7) |
| | $V_{OS2}$ | 3.5 | 4.5 | 6 | V | (Note 7) |
| DC Differential Error Voltage | $\lvert V_{OS1}-V_{OS2}\rvert$ | — | — | 300 | mV | |

(Note 2) Measured at 50% of SE (Typ.)

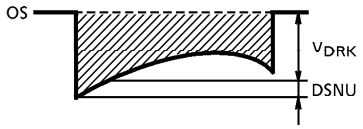
Definition of PRNU : PRNU = $\frac{\Delta\chi}{\overline{\chi}} \times 100\,(\%)$

Where $\overline{\chi}$ is average of total signal outputs and $\Delta\chi$ is maximum deviation from $\overline{\chi}$ under uniform illumination. (Channel 1)
In the case of 3750 elements (Channel 2), the condition is the same as above too.

(Note 3) $V_{SAT}$ is defined as minimum saturation output voltage of all effective pixels.

(Note 4) Definition of SE : SE = $\frac{V_{SAT}}{R}$ (lx·s)

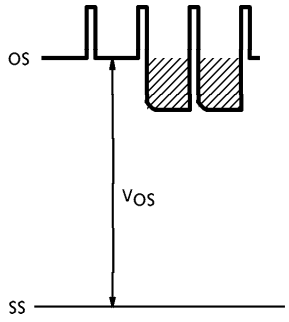
(Note 5) $V_{DRK}$ is defined as average dark signal voltage of all effective pixels.
DSNU is defined as different voltage between $V_{DRK}$ and $V_{MDK}$ when $V_{MDK}$ is maximum dark signal voltage.




(Note 6) Definition of DR : $DR = \frac{V_{SAT}}{V_{DRK}}$

$V_{DRK}$ is proportional to $t_{INT}$ (Integration Time).
So the shorter $t_{INT}$ condition makes wider DR values.

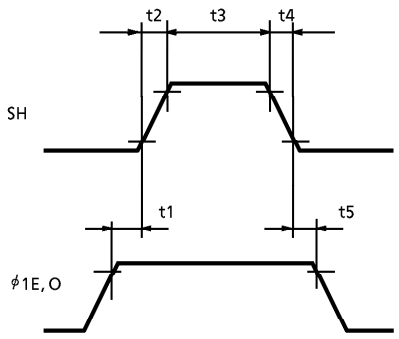
(Note 7) DC signal output voltage and DC compensation output voltage are defined as follows:



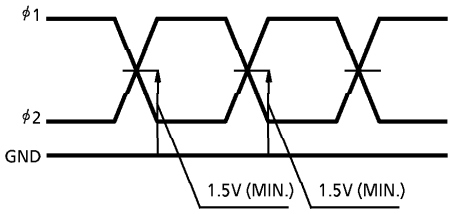

(Note 8) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.)

TIMING REQUIREMENTS

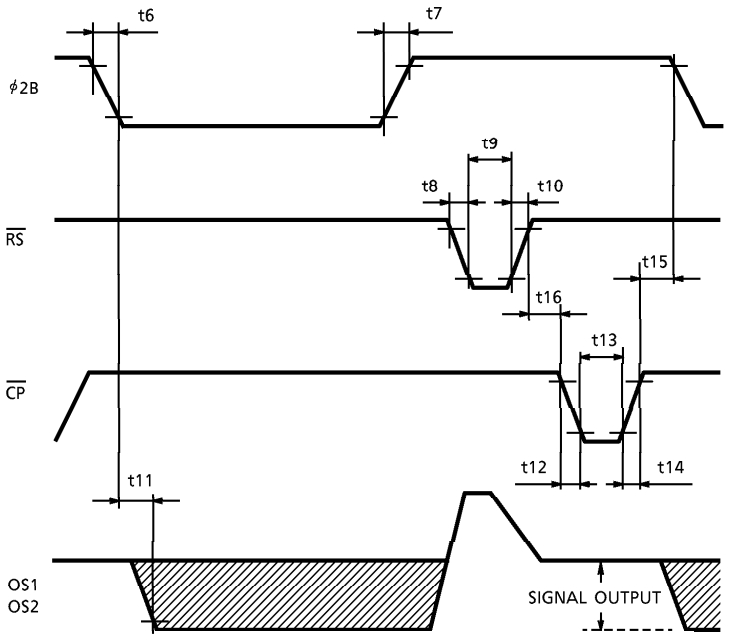
SH, $\phi$1 Timing




$\phi$1, $\phi$2 Cross Point




$\phi$2, $\overline{RS}$, $\overline{CP}$, OS Timing




| CHARACTERISTIC | SYMBOL | MIN. | TYP. (Note 9) | MAX. | UNIT |
|---|---|---|---|---|---|
| Pulse Timing of SH and $\phi$10, E | t1, t5 | 150 | 300 | — | ns |
| SH Pulse Rise Time, Fall Time | t2, t4 | 0 | 50 | — | ns |
| SH Pulse Width | t3 | 500 | 1000 | — | ns |
| $\phi$2 Pulse Rise Time, Fall Time | t6, t7 | 0 | 100 | — | ns |
| $\overline{RS}$ Pulse Rise Time, Fall Time | t8, t10 | 0 | 20 | — | ns |
| $\overline{RS}$ Pulse Width | t9 | 20 | 250 | — | ns |
| Video Data Delay Time (Note 10) | t11 | — | 20 | — | ns |
| $\overline{CP}$ Pulse Rise Time, Fall Time | t12, t14 | 0 | 20 | — | ns |
| $\overline{CP}$ Pulse Width | t13 | 20 | — | — | ns |
| Pulse Timing of $\phi$2B and $\overline{CP}$ | t15 | 0 | — | — | ns |
| Pulse Timing of $\overline{RS}$ and $\overline{CP}$ | t16 | 0 | — | — | ns |

(Note 9) TYP. is the case of $f_{RS}$ = 1.0MHz
(Note 10) Load Resistance is 100kΩ

**OPERATING CONDITION**

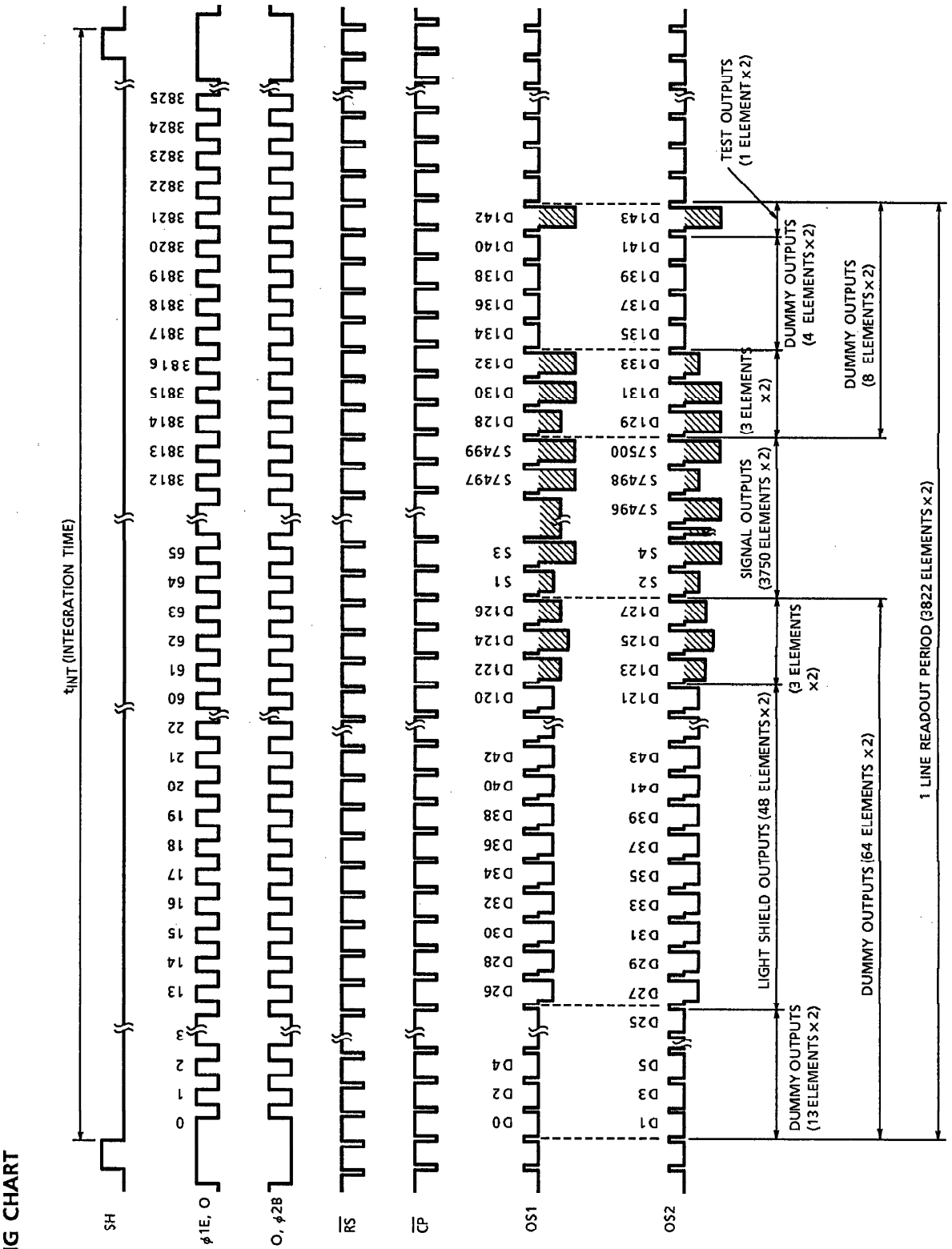
| CHARACTERISTIC | | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Clock Pulse Voltage | "H" Level | $V_{\phi}1E, O$ | 4.5 | 5 | 5.5 | V |
| | "L" Level | $V_{\phi}2E, O$ | 0 | — | 0.5 | |
| Final Stage Clock Voltage | "H" Level | $V_{\phi}2B$ | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Shift Pulse Voltage | "H" Level | (Note) | $V_{\phi}E, 0"H" - 0.5$ | $V_{\phi}E, 0"H"$ | $V_{\phi}E, 0"H"$ | V |
| | "L" Level | $V_{SH}$ | 0 | — | 0.5 | |
| Reset Pulse Voltage | "H" Level | $V_{\overline{RS}}$ | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Clamp Pulse Voltage | "H" Level | $V_{\overline{CP}}$ | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Power Supply Voltage | | $V_{OD}$ | 11.4 | 12 | 13 | V |

(Note) $V_{\phi}E, 0"H"$ means the value of high level voltage at $V_{\phi}E, 0$, when SH pulse is high level.

**CLOCK CHARACTERISTICS** (Ta = 25°C)

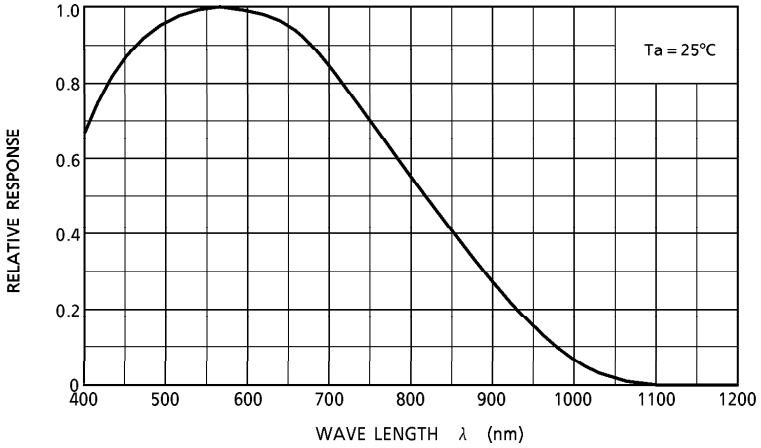
| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Clock Pulse Frequency | $f_{\phi}$ | — | 1 | 10 | MHz |
| Reset Pulse Frequency | $f_{\overline{RS}}$ | — | 1 | 10 | MHz |
| Clock Capacitance | $C_{\phi}E$ | — | 350 | 450 | pF |
| | $C_{\phi}O$ | — | 350 | 450 | pF |
| Final Stage Clock Capacitance | $C_{\phi}B$ | — | 10 | 20 | pF |
| Shift Gate Capacitance | $C_{SH}$ | — | 350 | 450 | pF |
| Reset Gate Capacitance | $C_{\overline{RS}}$ | — | 10 | 20 | pF |
| Clamp Gate Capacitance | $C_{\overline{CP}}$ | — | 10 | 20 | pF |

## TIMING CHART



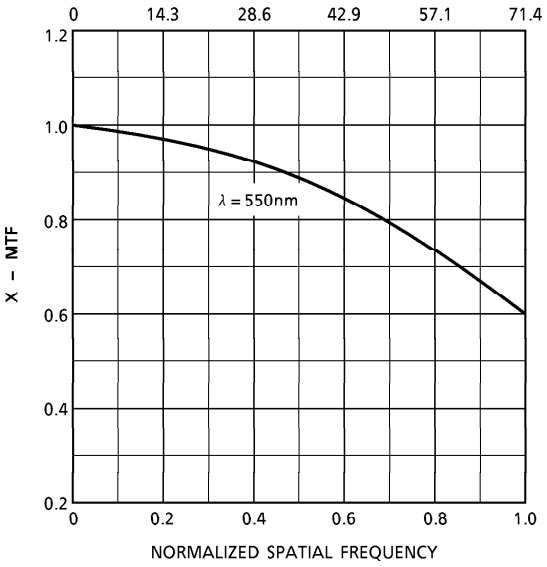
## TYPICAL PERFORMANCE CURVES

SPECTRAL RESPONSE



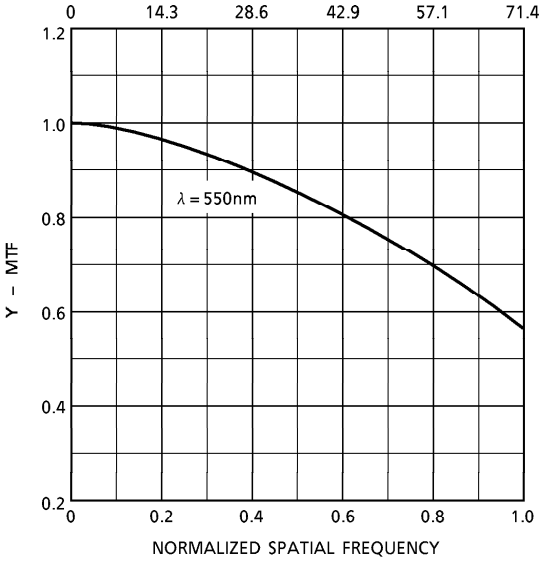

MODULATION TRANSFER FUNCTION OF X-DIRECTION

SPATIAL FREQUENCY (Cycles / mm)



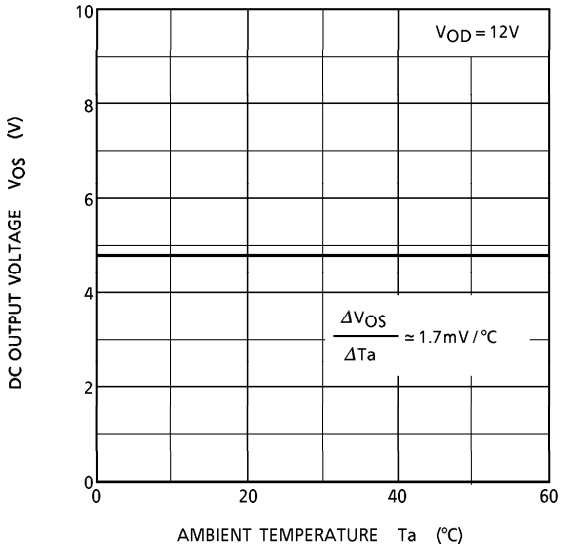

MODULATION TRANSFER FUNCTION OF Y-DIRECTION

SPATIAL FREQUENCY (Cycles / mm)

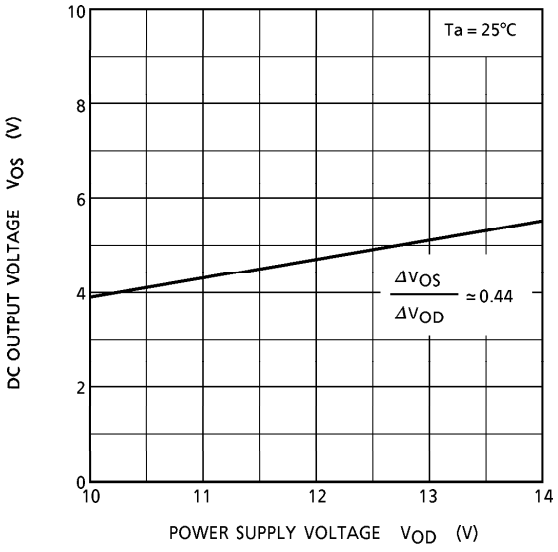


**TYPICAL PERFORMANCE CURVES (Cont'd)**

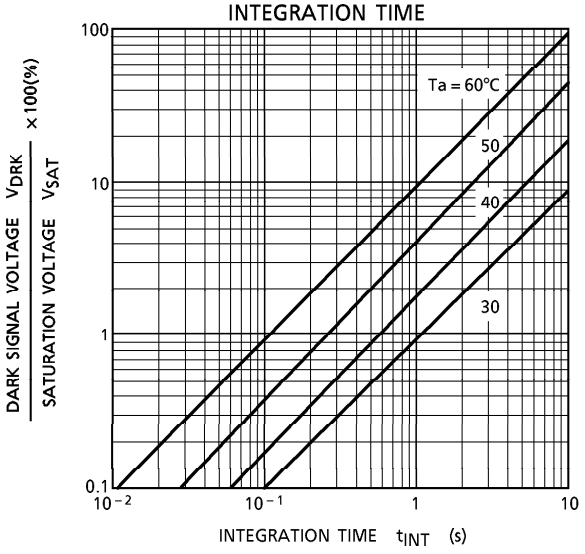
DC OUTPUT VOLTAGE vs
AMBIENT TEMPERATUER




DC OUTPUT VOLTAGE vs
POWER SUPPLY VOLTAGE




DARK SIGNAL VOLTAGE vs
INTEGRATION TIME



**CAUTION**

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry by blowing with filtered dry $N_2$.

   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

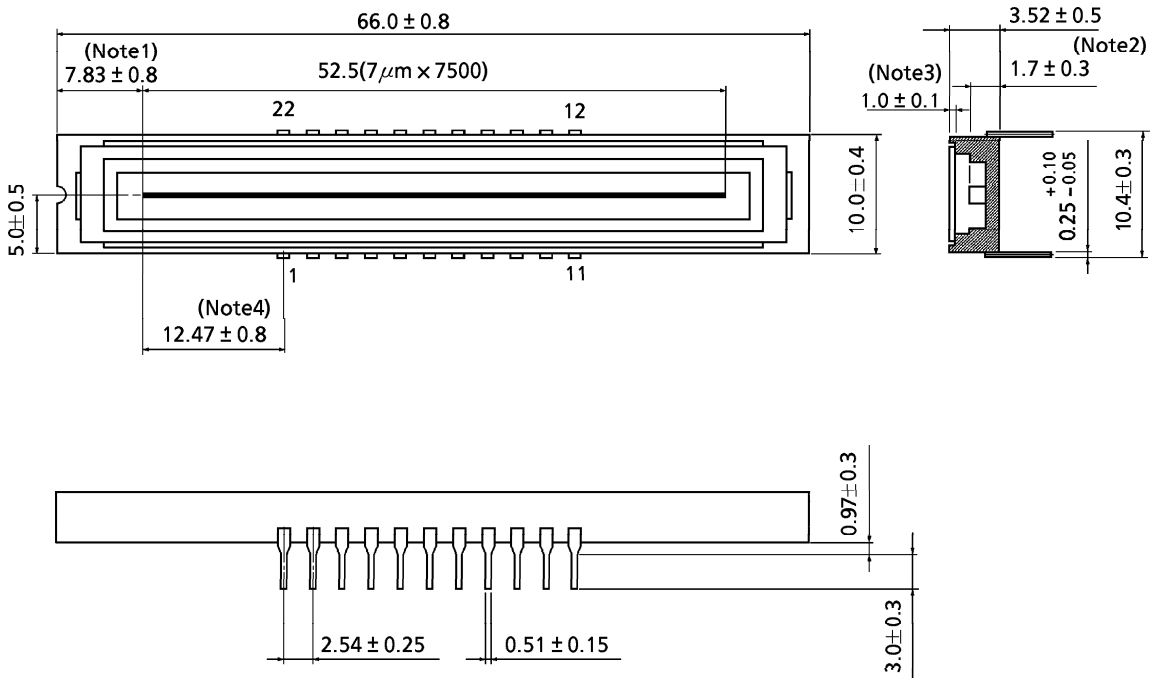
3. Incident Light

   CCD sensor is sensitive to infrared light.

   Note that infrared light component degrades resolution and PRNU of CCD sensor.

**OUTLINE DRAWING**

Unit in mm




(Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 3) GLASS THICKNES (n = 1.5)
(Note 4) No. 1 SENSOR ELEMENT (S1) TO CENTER OF No. 1 PIN.

Weight : 6.6g (Typ.)