

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

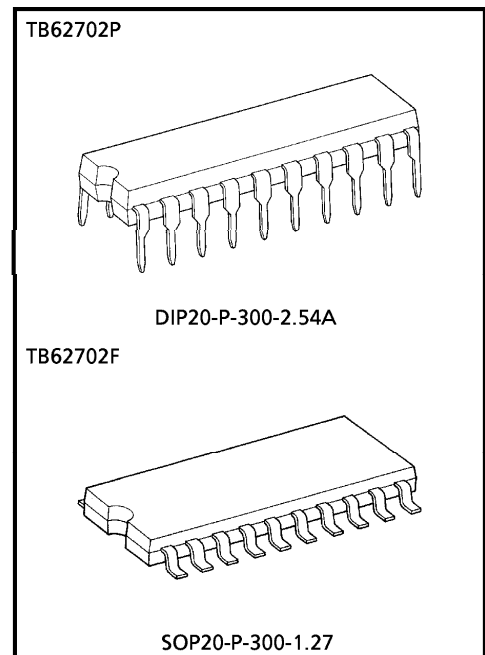
TB62702P, TB62702F

10BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH / 10SEGMENT LED DRIVERS

The TB62702P, TB62702F are specifically designed for 10-Segment LED Drivers and LED display. And these are monolithic integrated circuits designed to be used together with Bi-CMOS (DMOS) integrated circuit. The devices consist of a 10bit shift Register and 10bit Latches, and 10bit DMOS structures.

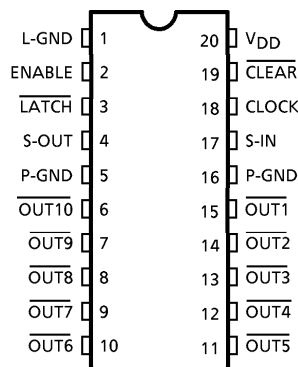
FEATURES

- 10bit serial-in parallel-out shift register / latch / 10segment LED driver (Bi-CMOS process)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Serial data output for cascade operation
- Package ; P-type DIP-20-P-300A
F-type SOP-20-P-300



Weight
 DIP20-P-300-2.54A : 2.25g (Typ.)
 SOP20-P-300-1.27 : 0.48g (Typ.)

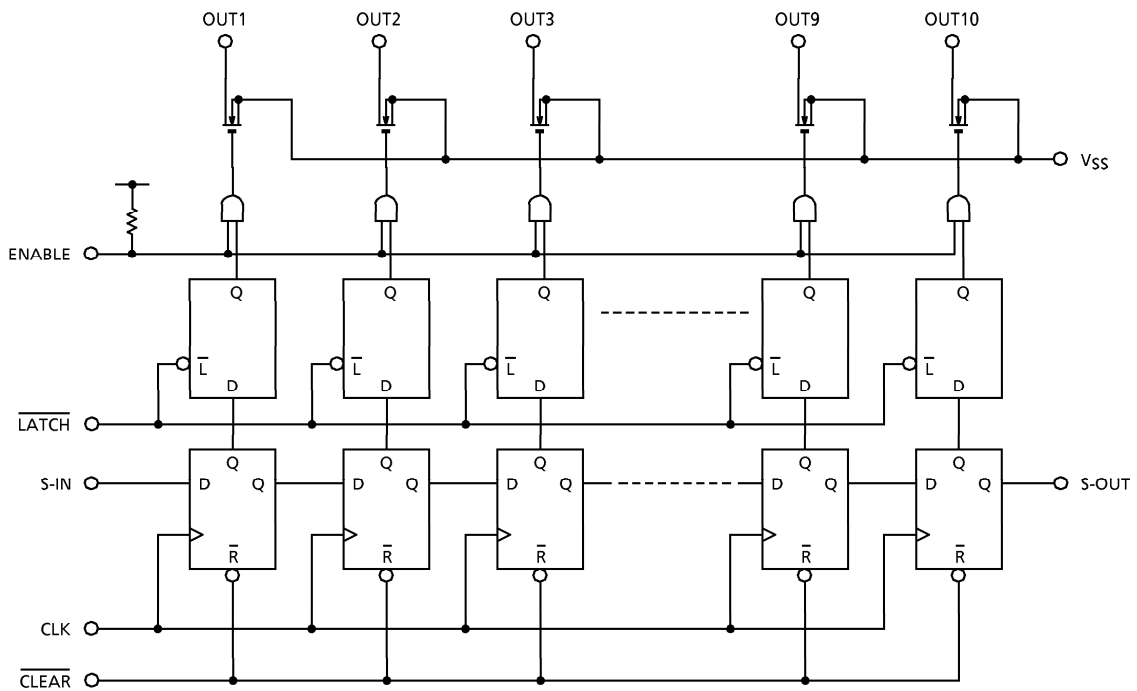
PIN CONNECTION (TOP VIEW)



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BLOCK DIAGRAM



MAXIMUM RATINGS (Ta = 25°C, VSS = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Output Drain-Source Voltage	V _{OUT}	-0.4~30	V
Input Current	I _{OUT}	30	mA / bit
Power Dissipation	P	P _D	1.47
	F	(Note 1)	0.96 (Note 2)
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

(Note 1) Delated above 25°C in the proportion of 11.7mW/°C (P-type), 7.7mW/°C (F-type).

(Note 2) On Glass Epoxy (50 × 50 × 1.6mm Cu 40%)

RECOMMENDED OPERATING CONDITIONS ($T_a = -40\sim 85^\circ\text{C}$, $V_{SS} = 0\text{V}$)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	—	4.5	5	5.5	V
Input Current	"H" Level	V_{IH}	—	$0.7 V_{DD}$	—	V_{DD}	V
	"L" Level	V_{IL}	—	0	—	$0.3 V_{DD}$	
Output Drain-Source Voltage		V_{OUT}	—	—	—	30	V
Output Current		I_{OUT}	Duty = 100%, All output "L" level	—	—	24	mA / ch
Power Dissipation	P	P_D	—	—	—	760	mW
	F		(Note 1)	—	—	470	

(Note 1) On Glass Epoxy (50×50×1.6mm Cu 40%)

ELECTRICAL CHARACTERISTICS ($T_a = -40\sim 85^\circ\text{C}$, $V_{DD} = 4.5\sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	"L" Level	V_{DS1}	—	$I_{OUT} = 15\text{mA}$, $T_a = 25^\circ\text{C}$	—	—	0.18	V
	"L" Level	V_{DS1}	—	$I_{OUT} = 15\text{mA}$	—	—	0.27	
	"L" Level	V_{DS2}	—	$I_{OUT} = 26\text{mA}$, $T_a = 25^\circ\text{C}$	—	—	0.31	
	"L" Level	V_{DS2}	—	$I_{OUT} = 26\text{mA}$	—	—	0.47	
Output Resistor		R_{ON}	—	$T_a = 25^\circ\text{C}$, $I_{OUT} = 26\text{mA}$	—	—	12	Ω
Output Current		I_{OZ1}	—	$V_{OUT} = 30\text{V}$, EN = "L" 1bit	—	—	10	μA
		I_{OZ2}	—	$V_{OUT} = 30\text{V}$, EN = "L" 10bit	—	—	± 1	
Input Current		I_{IN}	—	$V_{IN} = V_{DD}$ or V_{SS}	—	—	± 1	μA
		I_{IL}	—	ENABLE, $V_{IN} = V_{SS}$	-27.5	-55.0	-110.0	
Output Current	"H" Level	I_{OH}	—	S-OUT $V_{DS} = 4.6\text{V}$, $V_{DD} = 5.0\text{V}$	-400	-600	—	μA
	"L" Level	I_{OL}	—	S-OUT $V_{DS} = 0.4\text{V}$, $V_{DD} = 5.0\text{V}$	400	600	—	
Input Voltage	"H" Level	V_{IH}	—	—	$0.7 V_{DD}$	—	V_{DD}	V
	"L" Level	V_{IL}	—	—	0	—	$0.3 V_{DD}$	
Operating Supply Current		I_{DD1}	—	$f_{CLK} = 5\text{MHz}$ NO loads, 1bit	—	—	1500	μA
Supply Current		I_{DD2}	—	—	—	—	500	

SWITCHING CHARACTERISTICS

(Ta = 25°C, VDD = 5V, VOUT = 30V, RL = 1150Ω, CL = 15pF, "H" = VIH, "L" = VIL)

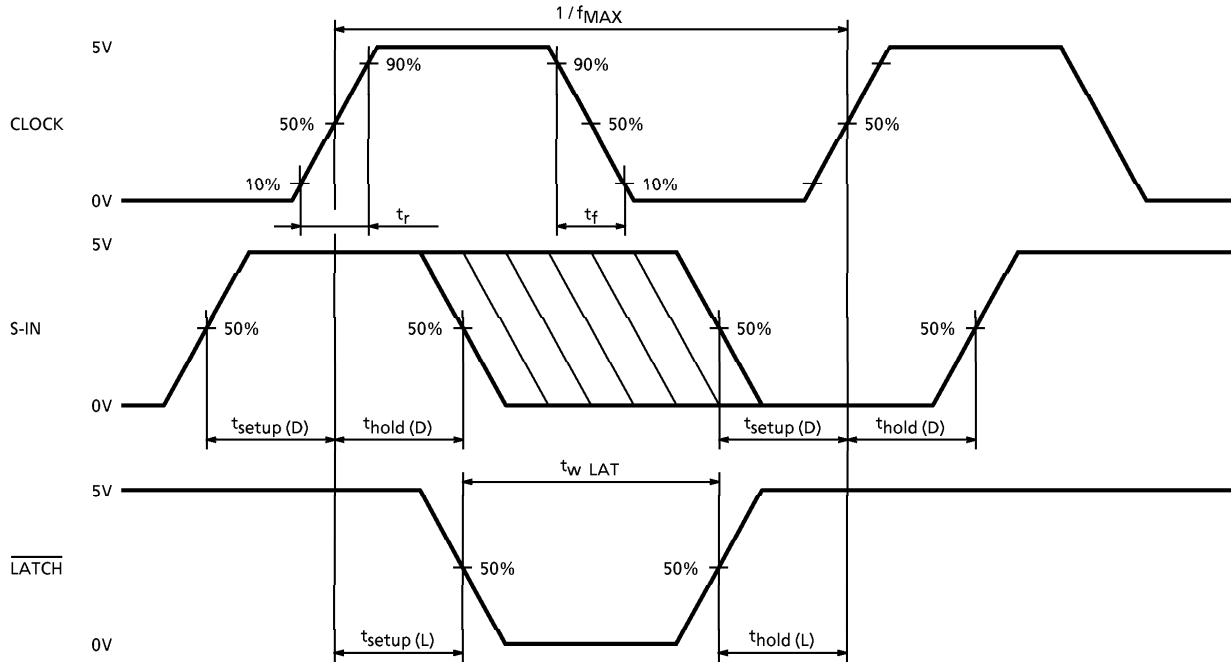
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Propagation Delay Time (Low-to-High)	CLK-OUTn	t _{pLH}	LAT = "H", CLR = "H", EN = "H"	—	—	250	ns
	CLK-OUTn		LAT = "H", EN = "H"	—	—	250	
	LAT-OUTn		CLR = "H", EN = "H"	—	—	200	
	EN-OUTn		LAT = "H", CLR = "H"	—	—	150	
Propagation Delay Time (High-to-Low)	CLK-OUTn	t _{pHL}	LAT = "H", CLR = "H", EN = "H"	—	—	250	ns
	LAT-OUTn		CLR = "H", EN = "H"	—	—	200	
	EN-OUTn		LAT = "H", CLR = "H"	—	—	150	
Set Up Time	CLK-LAT	t _{setup} (L)	—	—	50	ns	
	CLK-S-IN	t _{setup} (D)	—	—	35		
Hold Time	CLK-LAT	t _{hold} (L)	—	—	105		
	CLK-S-IN	t _{hold} (D)	—	—	50		
Clock Pulse Width	t _w CLK	—	—	—	100	ns	
Latch Pulse Width	t _w LATn	—	—	—	50		
Clear Pulse Width	t _w CLR	—	—	—	50		
Enable Pulse Width	t _w EN	—	—	—	400		
Output Rise Time	t _{or}	OUTn	—	—	1000	ns	
	t _r	S-OUT, VSS = 0V	—	—	50		
Output Fall Time	t _{of}	OUTn	—	—	150		
	t _f	S-OUT, VSS = 0V	—	—	50		
Maximum Clock Frequency	f _{MAX1}	Duty = 50% Cascade connected	5	8	—	MHz	
	f _{MAX2}	Duty = 50%	6	12	—		

RECOMMENDED TIMING CONDITIONS (Ta = -40~85°C, VDD = 4.5~5.5V, VSS = 0)

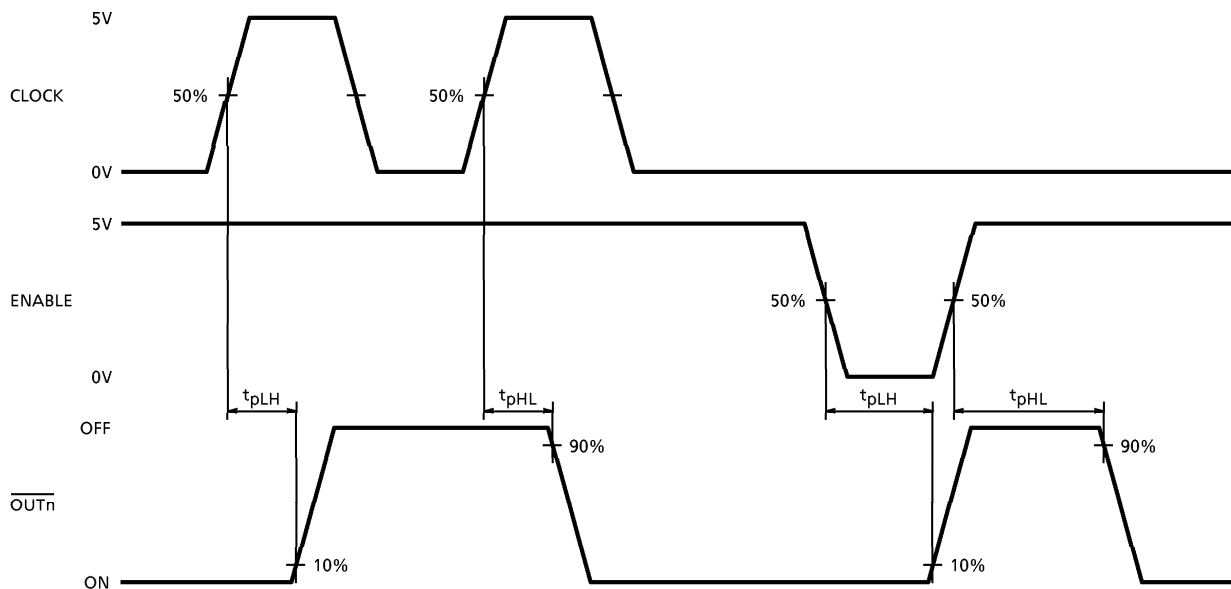
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	t _w CLK	—	100	—	—	ns
Enable Pulse Width	t _w EN	—	400	—	—	μs
Latch Pulse Width	t _w LAT	—	100	—	—	ns
Clear Pulse Width	t _w CLR	—	100	—	—	ns
Data Set Up Time	t _{setup}	—	100	—	—	ns
Data Hold Time	t _{hold}	—	150	—	—	ns

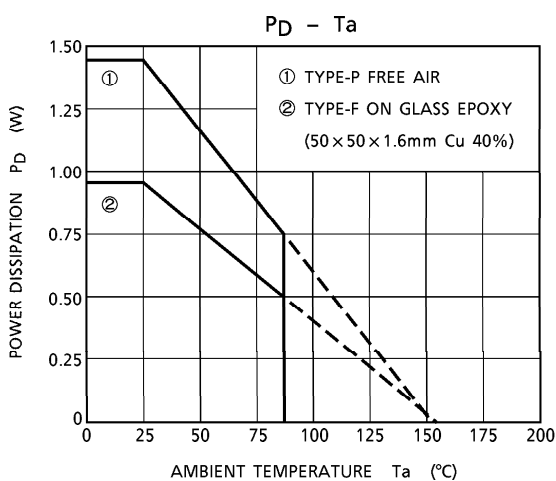
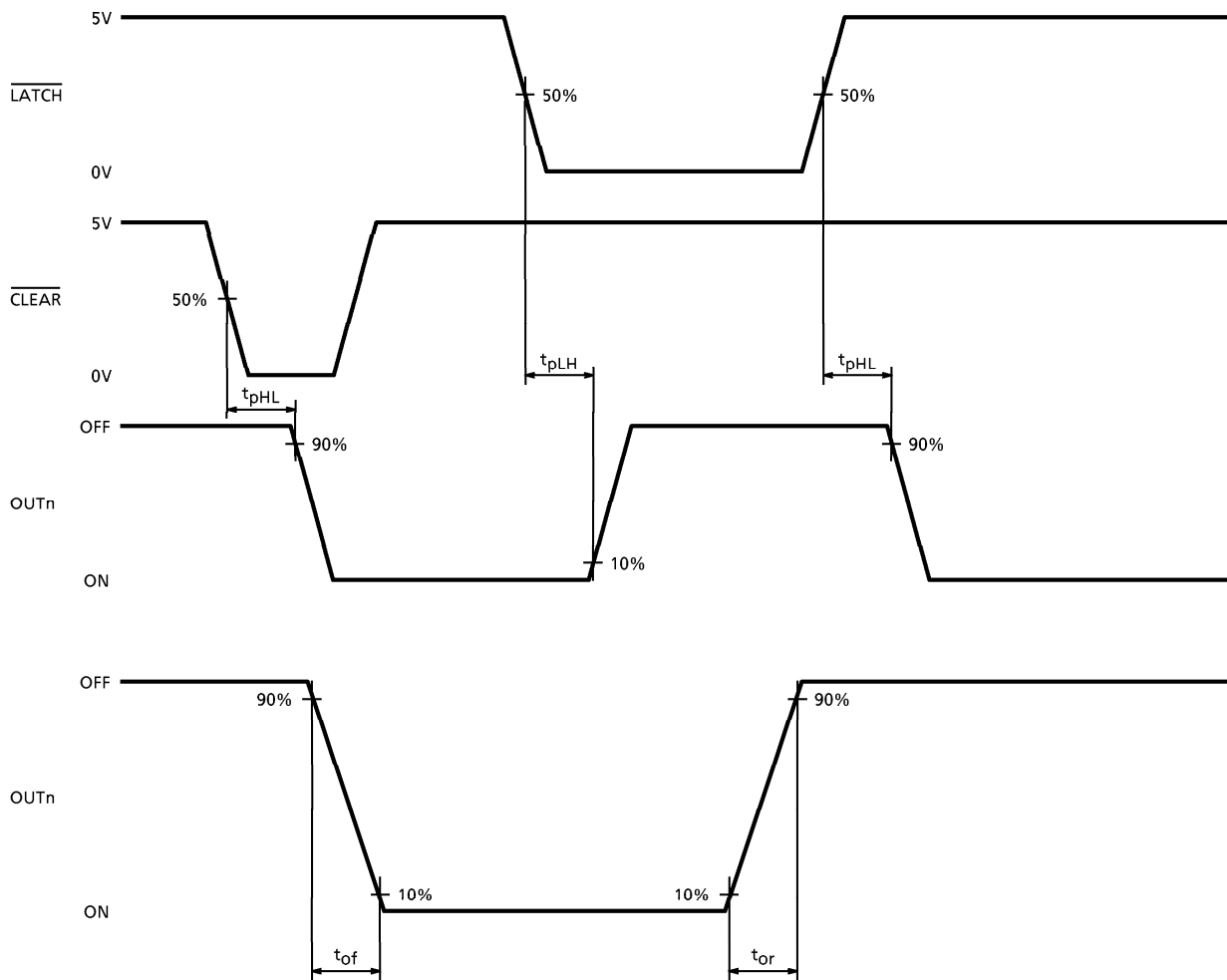
TIMING DIAGRAM

1. Input timing diagram



2. Propagation delay time



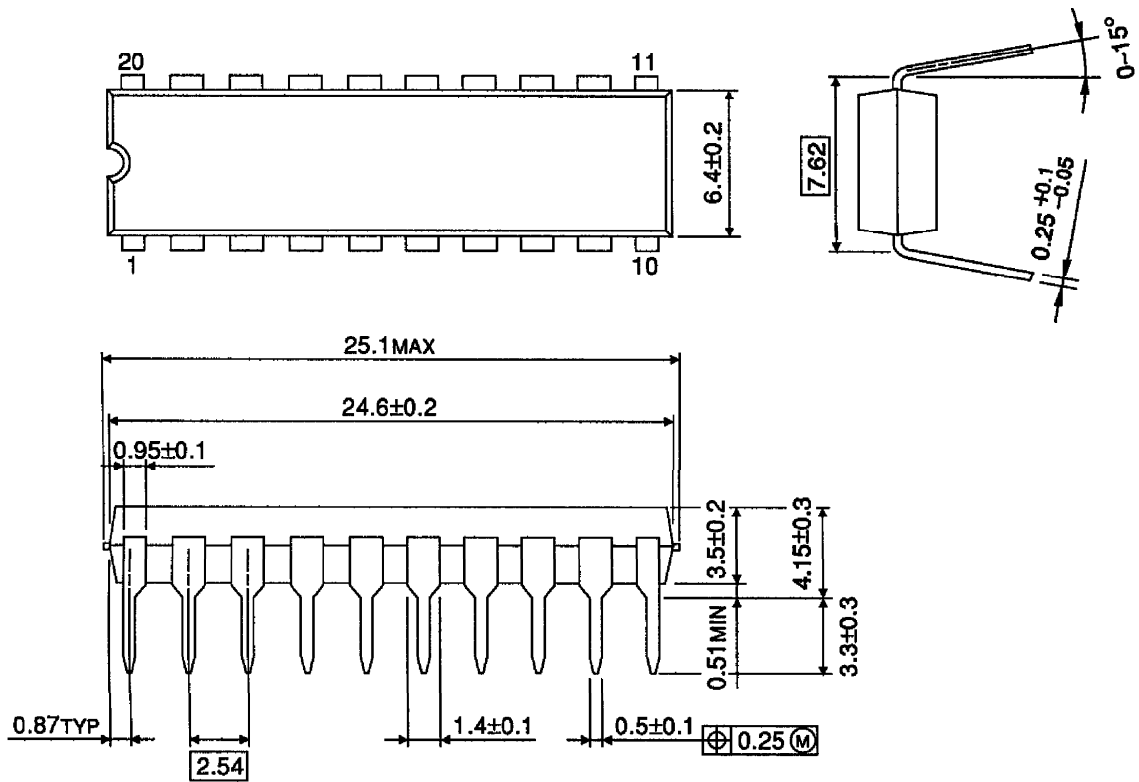


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING
DIP20-P-300-2.54A

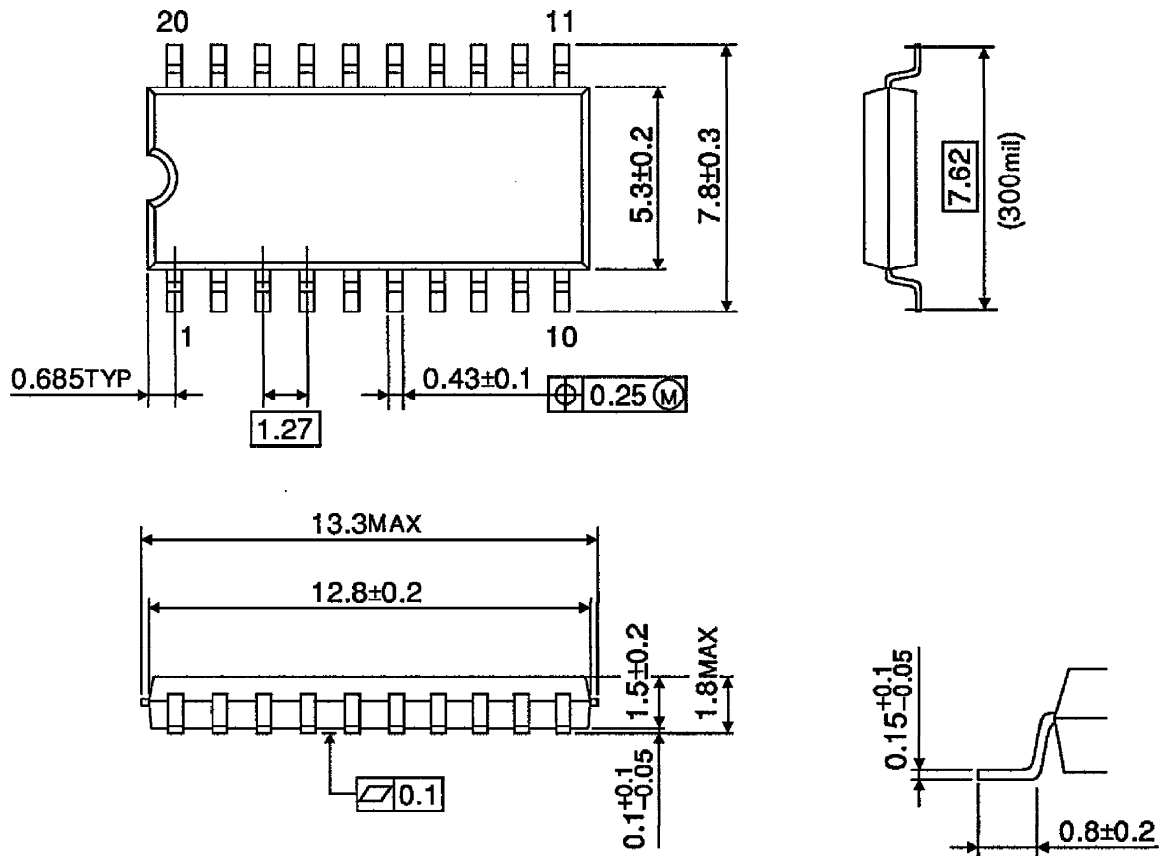
Unit : mm



Weight : 2.25g (Typ.)

OUTLINE DRAWING
SOP20-P-300-1.27

Unit : mm



Weight : 0.48g (Typ.)