TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

T6M74A, JT6M74A-AS

T6M74A, JT6M74A-AS, CMOS 1 CHIP LSI FOR LCD ELECTRONIC CALCULATOR

The T6M74A, JT6M74A-AS is a CMOS 1 chip microcomputer for 16-digits capacity 1-memory electronic calculation.
T6M74A, JT6M74A-AS is the complete single chip CMOS LSI for electronic calculator with single power supply operation.
Wide operating voltage range and low power consumption make it suitable for 1.5V solar battery operated.
Besides T6M74A, JT6M74A-AS can selectable with a pin-programmable to function of Power timer and Memory hold. With the following features.

QFP80-P-1420-0.80A
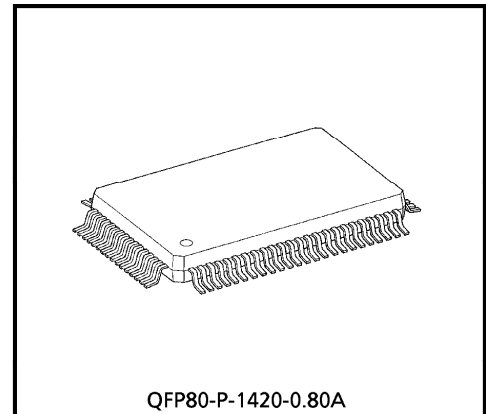
Weight : 1.52g (Typ.)

FEATURES

● Display : 16-digits of data, 1-digits of sign, error symbol, memory load symbol.

● Algebraic mode.

● Standard 4 functions (+ , − , × , ÷)

● Automatic percentage operation with add-on, discount.

● Automatic delta percentage, mark-up and markdown operations.

● Square root.

● Constant calculation.

● Chain calculation.

● Change sign.

● Floating point or momentary mode (selectable with a switch).

● Fixed point ("0", "1", "2", "3", "4" or "6" places) or floating point (selectable with a switch).

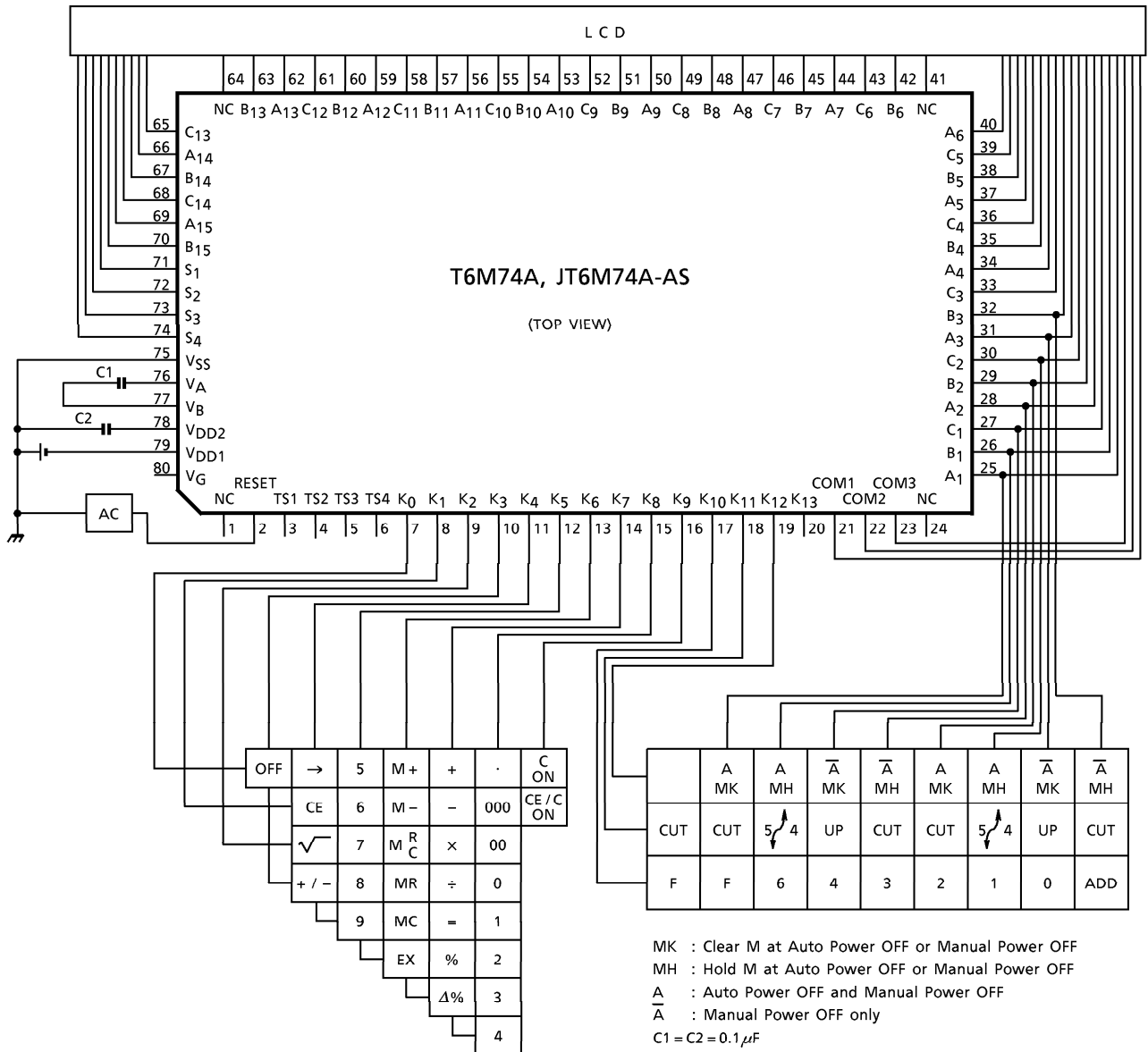● Adding point mode (selectable with a switch).

- Rounding switches (rounding up, down and off).

- Leading zero suppression.

- Trailing zero suppression.

- Punctuation on display, commas for thousands.

- Memory contents indicator, turned on with non-zero in the memory.

- Registration overflow, indicating that too many digits are entered (the most significant digit are protected).

- Result overflow, indicating during calculation (most function key are locked as it happened).

- Memory overflow indicating to flashing of memory load mark.

- Key roll over function.

- Floating minus.

SYSTEM BLOCK DIAGRAM

Battery Type

L C D

T6M74A, JT6M74A-AS

(TOP VIEW)

	A	A	$\overline{A}$	$\overline{A}$	A	A	$\overline{A}$	$\overline{A}$
	MK	MH	MK	MH	MK	MH	MK	MH
	CUT	CUT	5/4	UP	CUT	CUT	5/4	UP
								CUT
	F	F	6	4	3	2	1	0
								ADD

OFF	→	5	M+	+	·	C ON
CE	6	M−	−	000	CE/C ON
√	7	M R C	×	00
+/−	8	MR	÷	0
9	MC	=	1
EX	%	2
Δ%	3
4

MK : Clear M at Auto Power OFF or Manual Power OFF
MH : Hold M at Auto Power OFF or Manual Power OFF
A : Auto Power OFF and Manual Power OFF
$\overline{A}$: Manual Power OFF only
C1 = C2 = 0.1 μF

Dual Type

MK : Clear M at Auto Power OFF or Manual Power OFF
MH : Hold M at Auto Power OFF or Manual Power OFF
A : Auto Power OFF and Manual Power OFF
$\overline{A}$: Manual Power OFF only
$C1 = C2 = 0.1\mu F$
$C3 = 10\mu F$

Solar Type

L C D

T6M74A, JT6M74A-AS

(TOP VIEW)

Pins (top row): 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41

Top labels: NC B_{13} A_{13} C_{12} B_{12} A_{12} C_{11} B_{11} A_{11} C_{10} B_{10} A_{10} C_9 B_9 A_9 C_8 B_8 A_8 C_7 B_7 A_7 C_6 B_6 NC

Left labels:
65 C_{13}
66 A_{14}
67 B_{14}
68 C_{14}
69 A_{15}
70 B_{15}
71 S_1
72 S_2
73 S_3
74 S_4
75 V_{SS}
76 V_A
77 V_B
78 V_{DD2}
79 V_{DD1}
80 V_G

Right labels:
40 A_6
39 C_5
38 B_5
37 A_5
36 C_4
35 B_4
34 A_4
33 C_3
32 B_3
31 A_3
30 C_2
29 B_2
28 A_2
27 C_1
26 B_1
25 A_1

Bottom labels:
RESET
NC TS1 TS2 TS3 TS4 K_0 K_1 K_2 K_3 K_4 K_5 K_6 K_7 K_8 K_9 K_{10} K_{11} K_{12} K_{13} COM1 COM3 NC
COM2

Bottom pins: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

C3 C2 C1 AC

Keypad matrix:

OFF	→	5	M+	+	·	C ON
CE	6	M−	−	000	CE / C ON
√	7	M RC	×	00
+/−	8	MR	÷	0
	9	MC	=	1
		EX	%	2
			Δ%	3
				4

	A MK	A MH	$\overline{A}$ MK	$\overline{A}$ MH	A MK	A MH	$\overline{A}$ MK	$\overline{A}$ MH
CUT	CUT	5/4	UP	CUT	CUT	5/4	UP	CUT
F	F	6	4	3	2	1	0	ADD

MK : Clear M at Auto Power OFF or Manual Power OFF
MH : Hold M at Auto Power OFF or Manual Power OFF
A   : Auto Power OFF and Manual Power OFF
$\overline{A}$: Manual Power OFF only
C1 = C2 = 0.1 μF
C3 = 10 μF

CONNECTION OF LCD

(1)

SEGMENT
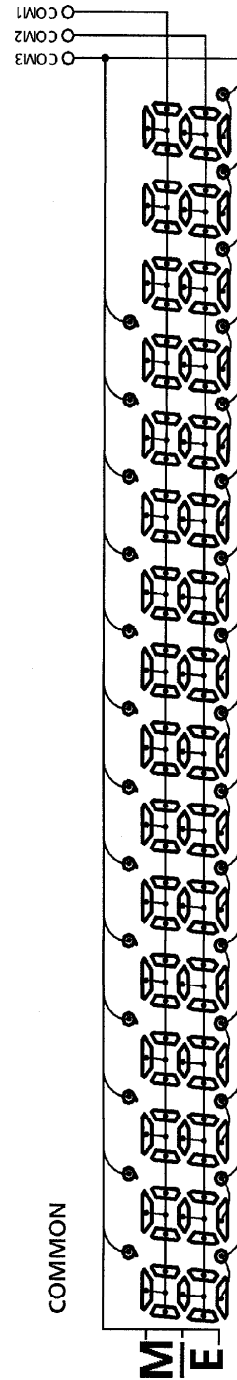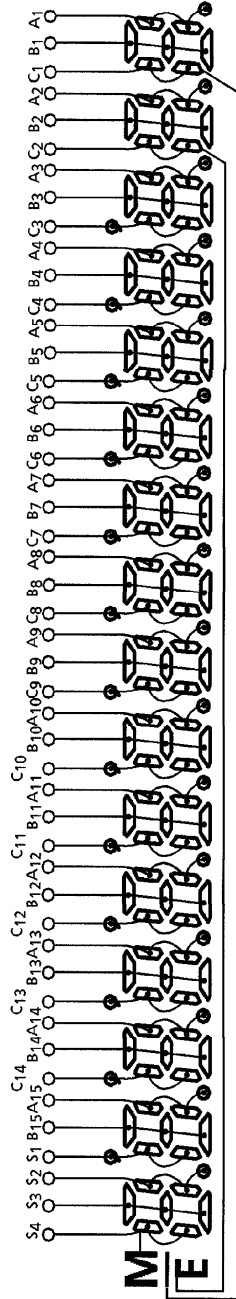
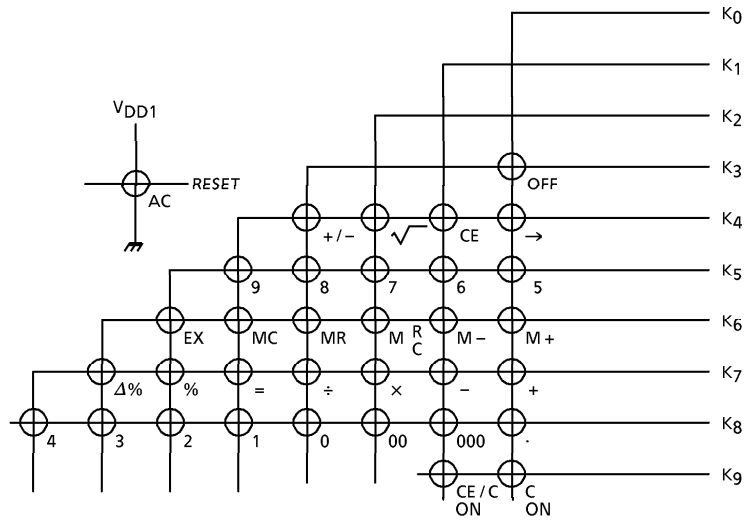**COMMON**

KEY LAYOUT

● Touch key

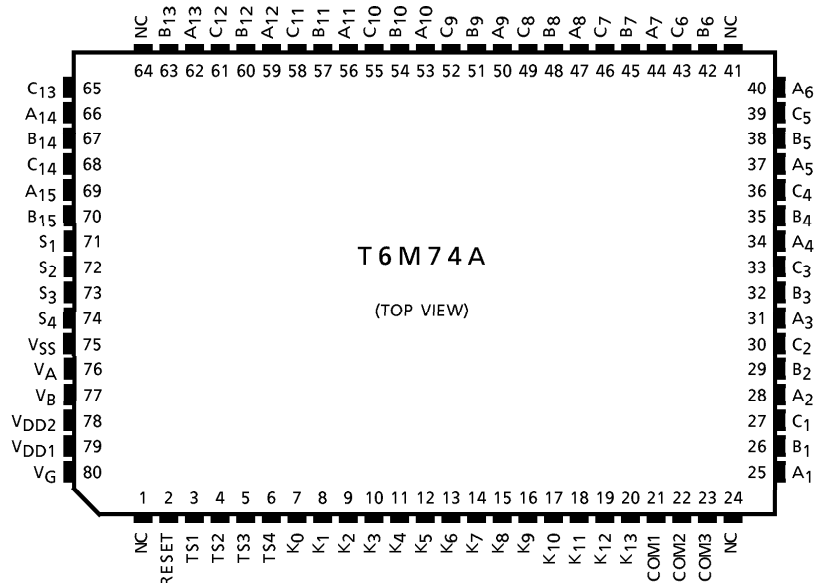

● Lock key
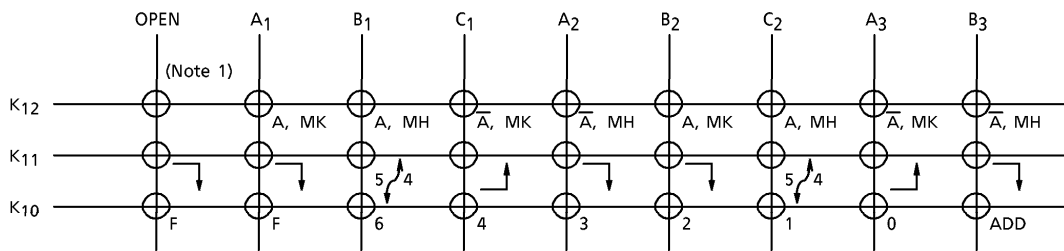
K_{12} ... Selectable with Auto Power OFF mode and Memory Hold Status. MH (Memory Hold). MK (Memory Kill)
K_{11} ... Rounding switches.
K_{10} ... Selectable with Fixed point or Floating mode.

(Note 1)
    K_{12} line is No choose then keep condition.
    K_{12} line is No choose at the system power on then initial condition is $\overline{A}$, MH Mode
    selected.

PIN LAYOUT

Top view of T6M74A pin layout.

Left side pins (top to bottom):
C_{13} 65, A_{14} 66, B_{14} 67, C_{14} 68, A_{15} 69, B_{15} 70, S_1 71, S_2 72, S_3 73, S_4 74, V_{SS} 75, V_A 76, V_B 77, V_{DD2} 78, V_{DD1} 79, V_G 80

Right side pins (top to bottom):
40 A_6, 39 C_5, 38 B_5, 37 A_5, 36 C_4, 35 B_4, 34 A_4, 33 C_3, 32 B_3, 31 A_3, 30 C_2, 29 B_2, 28 A_2, 27 C_1, 26 B_1, 25 A_1

Top pins (64 to 41): NC, B_{13}, A_{13}, C_{12}, B_{12}, A_{12}, C_{11}, B_{11}, A_{11}, C_{10}, B_{10}, A_{10}, C_9, B_9, A_9, C_8, B_8, A_8, C_7, B_7, A_7, C_6, B_6, NC

Bottom pins (1 to 24): NC, RESET, TS1, TS2, TS3, TS4, K_0, K_1, K_2, K_3, K_4, K_5, K_6, K_7, K_8, K_9, K_{10}, K_{11}, K_{12}, K_{13}, COM1, COM2, COM3, NC

SPECIFICATION OF CALCULATOR

Speed of calculation

Numeral	....	27.8~40.9ms
Function	1 $\boxed{+}$	42.7ms
	1 $\boxed{+}$ 2 $\boxed{+}$	83.9ms
Addition and subtract	123 $\boxed{+}$ 1 $\boxed{=}$	82.8ms
	9999999999999999 $\boxed{-}$ 0.000000000000001 $\boxed{=}$	106.4ms
Multiply	123 $\boxed{\times}$ 2 $\boxed{=}$	110.8ms
	1 $\boxed{\times}$ 9999999999999999 $\boxed{=}$	309.9ms
Device	123 $\boxed{\div}$ 3 $\boxed{=}$	165.1ms
	9999999999999999 $\boxed{\div}$ 1 $\boxed{=}$	348.4ms
Memory calculation	2 $\boxed{M+}$	93.8ms
	9999999999999999 $\boxed{\div}$ 1 $\boxed{M+}$	388.1ms
Square root	9999999999999999 $\boxed{\sqrt{\ }}$	259.7ms
	2 $\boxed{\sqrt{\ }}$	170.2ms

Operation example

1. Fixed point calculations

① Key	Display	Fixed point place	② Key	Display	Fixed point place
C	0.	DP = 3 (5 / 4)	C	0.	DP = 0 (＿↲)
2	2.		1	1.	
÷	2.		·	1.	
3	3.		2	1.2	
=	0.667		3	1.23	
2	2.		+	1.23	
·	2.		1	1.	
3	2.3		·	1.	
+	2.3		1	1.1	
4	4.		=	3.	
M +	6.300		9	9.	
1	1.		√	3.	
·	1.		×	3.	
2	1.2		1	1.	
M +	1.200		·	1.	
MR	7.5	DP = 4	1	1.1	DP = F
			=	3.3	

2. Adding point mode calculations

Key	Display	Key	Display	Key	Display
C	0.	M+	0.02M	=	33.27M −
1	1.	3	3.M	2	2.M
23	123	·	3.M	+	0.02M
+	1.23	123	3.123M	9	9.M
3	3.	M+	3.12M	·	9.M
=	1.26	MR	3.14M	√	3.M
3	3.	C	0.M	=	3.02M
2	32.	1	1.M		
×	32.	23	123M		
3	3.	−	1.23M		
·	3.	3	3.M		
000	3.000	4	34.M		
=	96.00	·	34.M		
2	2.	5	34.5M		

3. Constant calculations

① Multiplication

Key	Display	Constant
k	k	
×	k	
a	a	
=	k·a	k×
b	b	k×
=	k·b	k×

② Division

Key	Display	Constant
a	a	
÷	a	
k	k	
=	a / k	÷ k
b	b	÷ k
=	b / k	÷ k

③ Addition

Key	Display	Constant
a	a	
+	a	
k	k	
=	a + k	+ k
b	b	+ k
=	b + k	+ k

④ Subtraction

Key	Display	Constant
a	a	
−	a	
k	k	
=	a − k	− k
b	b	− k
=	b − k	− k

⑤ Percentage

Key	Display	Constant
k	k	
☒	k	
a	a	
☒%	k·a / 100	k ×
b	b	k ×
☒%	k·b / 100	k ×

⑥ Percentage

Key	Display	Constant
a	a	
☒÷	a	
k	k	
☒%	100·a / k	÷ k
b	b	÷ k
☒%	100·b / k	÷ k

⑦ Add-on

Key	Display	Constant
k	k	
☒+	k	
a	a	
☒%	k·(1 + a / 100)	k +
b	b	k +
☒%	k·(1 + b / 100)	k +

⑧ Discount

Key	Display	Constant
k	k	
☒−	k	
a	a	
☒%	k·(1 − a / 100)	k −
b	b	k −
☒%	k·(1 − b / 100)	k −

4. Δ% calculations

①

Key	Display
a	a
☒+	a
b	b
☒Δ%	100·(a + b) / b

②

Key	Display
a	a
☒−	a
b	b
☒Δ%	100·(a − b) / b

5. Mark-up, mark-down calculations

① Mark-up

Key	Display
a	a
☒÷	a
b	b
☒Δ%	a / (1 − b / 100)
☒Δ%	|a / (1 − b / 100)|

② Mark-down

Key	Display
a	a
☒÷	a
b	b
☒+/−	− b
☒Δ%	a / (1 + b / 100)
☒Δ%	a / (1 + b / 100) − a1

6. Add-on, discount calculations

Add-on   Discount

	Key	Display			Key	Display
①	a	a		②	a	a
	☒	a			☒	a
	b	b			b	b
	%	a·b / 100			%	a·b / 100
	+	a·b / 100			−	a·b / 100
	=	a (1 + b / 100)			=	a (1 − b / 100)
③	a	a		④	a	a
	+	a			−	a
	b	b			b	b
	%	a (1 + b / 100)			%	a (1 − b / 100)
⑤	a	a		⑥	a	a
	☒	a			☒	a
	b	b			b	b
	Δ%	a·(1 + b / 100)			+/−	− b
					Δ%	a (1 − b / 100)

MAXIMUM RATINGS

ITEM	SYMBOL	LIMITS	UNIT
Supply Voltage	V_{DD1}	$-0.3\sim2.0$	V
Input Voltage	V_{IN}	$-0.3\sim V_{DD1}+0.3$	V
Operating Temperature	T_{opr}	$0\sim40$	°C
Storage Temperature	T_{stg}	$-55\sim125$	°C

ELECTRICAL CHARACTERISTICS ($V_{DD1} = 1.5 \pm 0.2V$, $V_{DD2} = 3.0 \pm 0.4V$, $V_{SS} = 0V$, $Ta = 25°C$)

ITEM	SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD1}	—	—	—	1.2	1.5	2.0	V
"1" Input Voltage	$V_{IH(1)}$	—	$K_2\sim K_9$ RESET	—	$V_{DD1}-0.4$	—	V_{DD1}	V
"1" Input Voltage	$V_{IH(2)}$	—	$K_{10}\sim K_{13}$	—	$V_{DD2}-0.4$	—	V_{DD2}	V
"0" Input Voltage	V_{IL}	—	$K_2\sim K_{13}$ RESET	—	0	—	0.4	V
"1" Output Voltage	$V_{OH(1)}$	—	SEGMENT COM1~3	—	$V_{DD2}-0.2$	—	V_{DD2}	V
"0" Output Voltage	$V_{OL(1)}$	—	SEGMENT COM1~3	—	0	—	0.2	V
"M" Output Voltage	V_{OM}	—	COM1~3	—	$V_{DD1}-0.2$	—	$V_{DD1}+0.2$	V
"1" Output Voltage	$V_{OH(2)}$	—	$K_1\sim K_9$	—	$V_{DD1}-0.2$	—	V_{DD1}	V
"0" Output Voltage	$V_{OL(2)}$	—	$K_1\sim K_{13}$	—	0	—	0.2	V
"1" Output Resistance	R_{OH}	—	SEGMENT COM1~3	$V_{OUT} = V_{DD2}-0.5V$	—	—	70	kΩ
"0" Output Resistance	R_{OL}	—	SEGMENT COM1~3	$V_{OUT} = 0.5V$	—	—	70	kΩ
KEY Pull Up Resistance	$R_{KEYH(1)}$	—	RESET	$V_{OUT} = V_{DD1}-0.5V$	—	—	25	kΩ
	$R_{KEYH(2)}$	—	$K_0\sim K_9$	$V_{OUT} = V_{DD1}-0.5V$	—	—	14	kΩ
	$R_{KEYH(3)}$	—	$K_{10}\sim K_{13}$	$V_{OUT} = 0V$	120	—	800	kΩ
KEY Pull Down Resistance	$R_{KEYL(1)}$	—	RESET (1)	$V_{OUT} = V_{DD1}$	100	—	300	kΩ
	$R_{KEYL(2)}$	—	RESET (2)	$V_{OUT} = V_{DD1}$	18	—	300	kΩ
	$R_{KEYL(3)}$	—	$K_0\sim K_9$ (1)	$V_{OUT} = 0.5V$	—	—	50	kΩ
	$R_{KEYL(4)}$	—	$K_0\sim K_9$ (2)	$V_{OUT} = V_{DD1}$	72	—	170	kΩ
Oscillating (WAIT)	$f\phi WAIT$	—	—	$V_{DD1} = 1.5V$	5.4	9.0	15.5	kHz
Frequency (OPERATE)	$f\phi OP$	—	—	$V_{DD1} = 1.5V$	20.0	34	61.3	kHz
Frame Frequency	f_F	—	SEGMENT COM1~3	$V_{DD1} = 1.5V$	56.3	93.8	161.5	Hz

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	1 (WAIT)	I_{DDWAIT}	—	—	$V_{DD1} = 1.5V$	—	—	3.3	μA
	2 (OPERATE)	I_{DDOP}	—	—	$V_{DD1} = 1.2V$	—	—	8.9	μA
	3 (OFF)	I_{DDOFF}	—	—	$V_{DD1} = 1.5V$	—	—	2.0	μA
Power Off Timer Times		T	—	—	$V_{DD1} = 1.5V$	429	600	1001	s

WAVEFORMS FOR DISPLAY
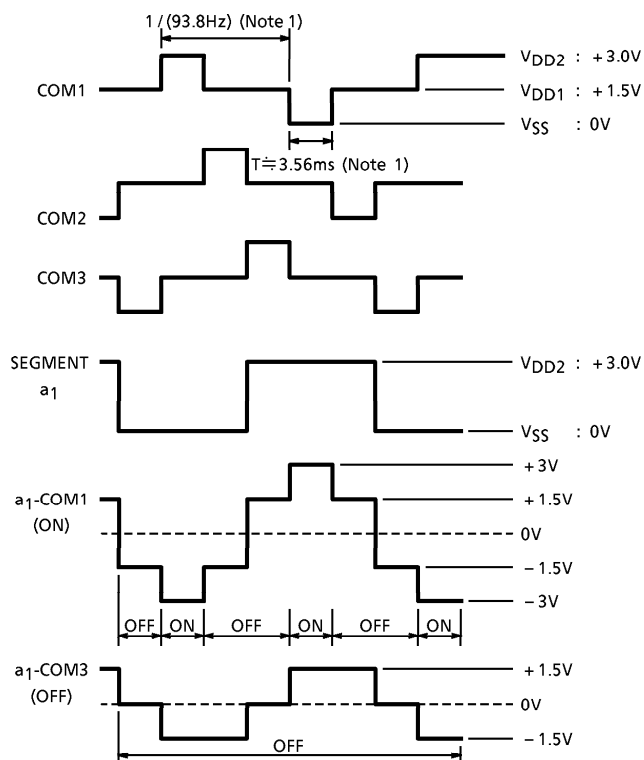
(Note 1) at $f\phi = 9kHz$

PAD LOCATION TABLE (μm)

NAME	X POINT	X POINT	NAME	X POINT	X POINT
COM3	-1757	-1680	B_{13}	1757	1680
COM2	-1757	-1520	A_{13}	1757	1520
COM1	-1757	-1360	C_{12}	1757	1360
K_{13}	-1757	-1200	B_{12}	1757	1200
K_{12}	-1757	-1040	A_{12}	1757	1040
K_{11}	-1757	-880	C_{11}	1757	880
K_{10}	-1757	-720	B_{11}	1757	720
K_9	-1757	-560	A_{11}	1757	560
K_8	-1757	-400	C_{10}	1757	400
K_7	-1757	-240	B_{10}	1757	240
K_6	-1757	-80	A_{10}	1757	80
K_5	-1757	80	C_9	1757	-80
K_4	-1757	240	B_9	1757	-240
K_3	-1757	400	A_9	1757	-400
K_2	-1757	560	C_8	1757	-560
K_1	-1757	720	B_8	1757	-720
K_0	-1757	880	A_8	1757	-880
*(TS4)	-1757	1040	C_7	1757	-1040
*(TS3)	-1757	1200	B_7	1757	-1200
*(TS2)	-1757	1360	A_7	1757	-1360
*(TS1)	-1757	1520	C_6	1757	-1520
RESET	-1757	1680	B_6	1757	-1680
V_G	-1388	1753	A_6	1278	-1752
V_{DD1}	-1151	1753	C_5	1118	-1752
V_{DD2}	-991	1753	B_5	958	-1752
V_B	-831	1753	A_5	798	-1752
V_A	-671	1753	C_4	638	-1752
V_{SS}	-511	1753	B_4	478	-1752
S_4	-351	1753	A_4	318	-1752
S_3	-191	1753	C_3	158	-1752
S_2	-31	1753	B_3	-2	-1752
S_1	129	1753	A_3	-162	-1752
B_{15}	289	1753	C_2	-322	-1752
A_{15}	449	1753	B_2	-482	-1752
C_{14}	609	1753	C_2	-642	-1752
B_{14}	769	1753	C_1	-802	-1752
A_{14}	929	1753	B_1	-962	-1752
C_{13}	1089	1753	A_1	-1122	-1752

*( ) Do not connect.

CHIP LAYOUT
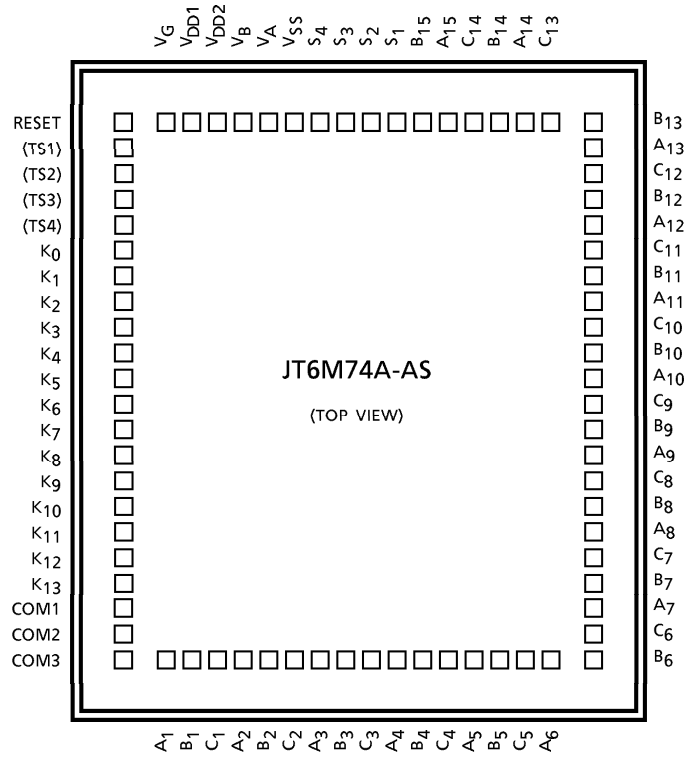
Chip size   : 3.79 × 3.84 (mm)
Chip thickness : 440 ± 30 (μm)
Substrate   : V_{SS}

PAD LAYOUT

PAD Pitch 160μm
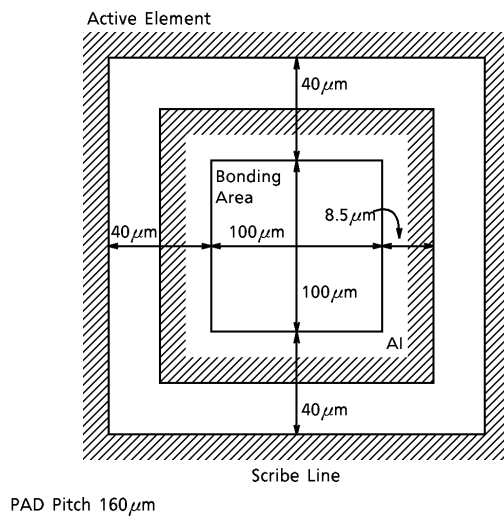
OUTLINE DRAWING
QFP80-P-1420-0.80A   Unit : mm

24.8±0.3
20.0±0.2
64   41
65   40
80   25
1   24

1.0TYP
14.0±0.2
18.8±0.3
0.8TYP   0.35±0.1   0.16 Ⓜ
0.8

2.7±0.2
3.05MAX
0.2±0.1

0.15 +0.1 -0.05
1.2±0.2
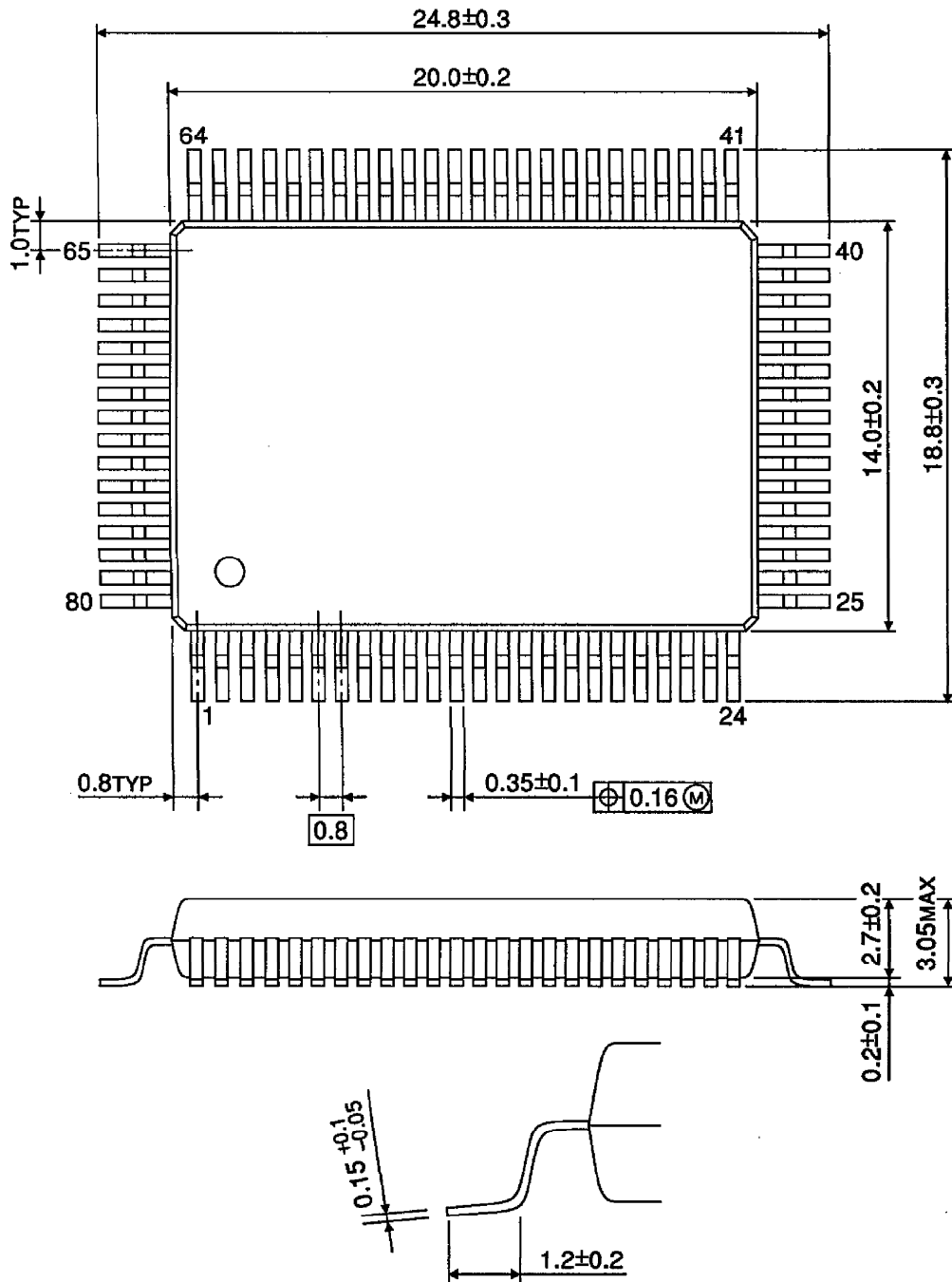
Weight : 1.52g (Typ.)

GENERAL SPECIFICATION FOR CALCULATOR LSI BARE CHIP

1. Purpose

   This is to specify the quality standard for the integrated circuit produced by TOSHIBA CORPORATION (hereinafter referred as to VENDOR) to be delivered to PURCHASER.

2. Definition

   This specification applies only to the calculator LSI bare chip produced by VENDOR and purchased by PURCHASER and defined the general specification items.

3. Priority of specifications

   When the discrepancies or questions happen to the specifications and instructions provided by VENDOR, the priority shall be ranked as follows.

   1) Individual specification for the calculator LSI bare chip.
      (Both PURCHASER and VENDOR are confirmed by the special sheets.)

   2) General specifications for the calculator LSI bare chip.

   3) Other related specifications and standards.

4. Characteristics

   To be shown in the individual specification sheets.
   The individual specification shall consist of the following 4 items in principle.

   1) Rated specifications.

   2) Electrical characteristics.

   3) Pin configuration & mechanical dimensions.

   4) Others.

5. Inspection of product for delivery

   5.1   Inspection lot

      a) Inspection lot shall consist of products produced by same material under same design, through same production process, and same facilities and assured same quality by same quality assurance method, and lot number shall be put on all trays to be able to trace the lot history.

      b) The quantity of products per Inspection lot shall consist of all the same VENDOR's lot number.

5.2   Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level II.

The acceptable quality level (AQL) shall be specified in following table :

TEST ITEM	AQL (%)
Electrical	2.5
Visual	4.0

5.3   Electrical criteria

Criteria of Electrical Characteristics are prescribed in Attachment-1.

5.4   Visual criteria

Visual Criteria are prescribed in Attachment-2.

6. Incoming inspection

   6.1   General

      a) PURCHASER's incoming inspection should be done within 15 days after PURCHASER receives the quantity of products in principle.

      b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data in failure rate and items regarding VENDOR's lot number respectively, if VENDOR demands the report from PURCHASER.

   6.2   Inspection procedure

   PURCHASER should do his incoming inspection according to the following procedure.

      a) First   :   Visual inspection should be done.

      b) Next :   Electrical and other inspection should be done under condition with bare chip before going into PURCHASER's process.

7. Treatment for defective lot and products

   Regarding the defective lot and defective products which are found through PURCHASER's incoming inspection, PURCHASER can be returned to VENDOR with detailed description on failures concerned.
   However, if VENDOR cannot receive the defective items within 30 days after PURCHASER's incoming inspection, VENDOR should be able to make no reference to the defective problem.

8. Packing and labeling

   a) Dice shall be placed in die tray with the top metalization facting up in order.

   b) In principle, a pile consists of 5 trays and several piles are packed in a package. These piles and packages are indicated with printed labels as shown below.

Date	
Name	
Lot No.	
Net	
TOSHIBA MADE IN JAPAN	

   c) PURCHASER shall return these packing materials to VENDOR on VENDOR's demand.

9. Storage criteria

   Solid state chips, unlike packaged devices, are non-hermetic devices normally fragile and small in physical size, and therefore, require special handling considerations as follows :

   9.1   Chips must be stored under proper conditions to insure that they are not subjected to a moist and / or contaminated atmosphere that alter their electrical, physical, or mechanical characteristics.
   After the shipping container is opened, the chips must be stored under the following conditions :

   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.

   9.2   The user must exercise proper care when handling chips or wafers to prevent even the slightest physical damage to the chip.

   9.3   During mounting and lead bounding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.

   9.4   After the chip has been mounted and bounded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
   In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful in handling chips.
In any event, because of the extremely small size and fragile nature of chips, care should be taken in handling these devices.

10.1 Grounding

   a) Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.

   b) Operator should be properly grounded.

10.2 In-process handling

   a) Assemblies or subassemblies of chips should be transported and stored in conductive carriers.

   b) All external leads of the assemblies or subassemblies should be shorted together.

VISUAL INSPECTION CRITERIA

1. Visual inspection magnification shall be 40 × in principle.

2. Defects defined :

   2.1   Thickness

   See the technical data sheet.

   2.2   Chip and crack

   A die shall be rejected if :

   a) Any crack of chip extends greater than 35μm in length into the inside of the scribble line. (see Fig.1)

   2.3   Metallization

   A die shall be rejected if :

   a) More than 25% of the designed area of the metallization is missing at any bonding pad.

   b) There is a short or break which affects electrical characteristics in any lead pattern.
      (see Fig.2)

   2.4   Glass protection coat

   A die shall be rejected if :

   a) It exhibits glass protection coat which covers more than 25% of any active bonding pad.

2.5   Attached foreign material

A die shall be rejected if :

a) A die is covered by stains or attached foreign material which size is more than 5 times as large as a bonding pad area.

b) It exhibits residual ink, stains or attached foreign material which covers more than 20% of any active bonding pad. (see Fig.3)

2.6   Others

A die shall be rejected if :

a) There have no evident probed impression on the bonding pads.

b) A inked die, defective die, is intermized.

3. Limit samples should be fized, if necessary.
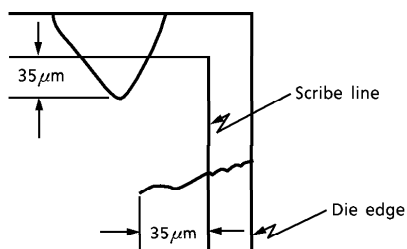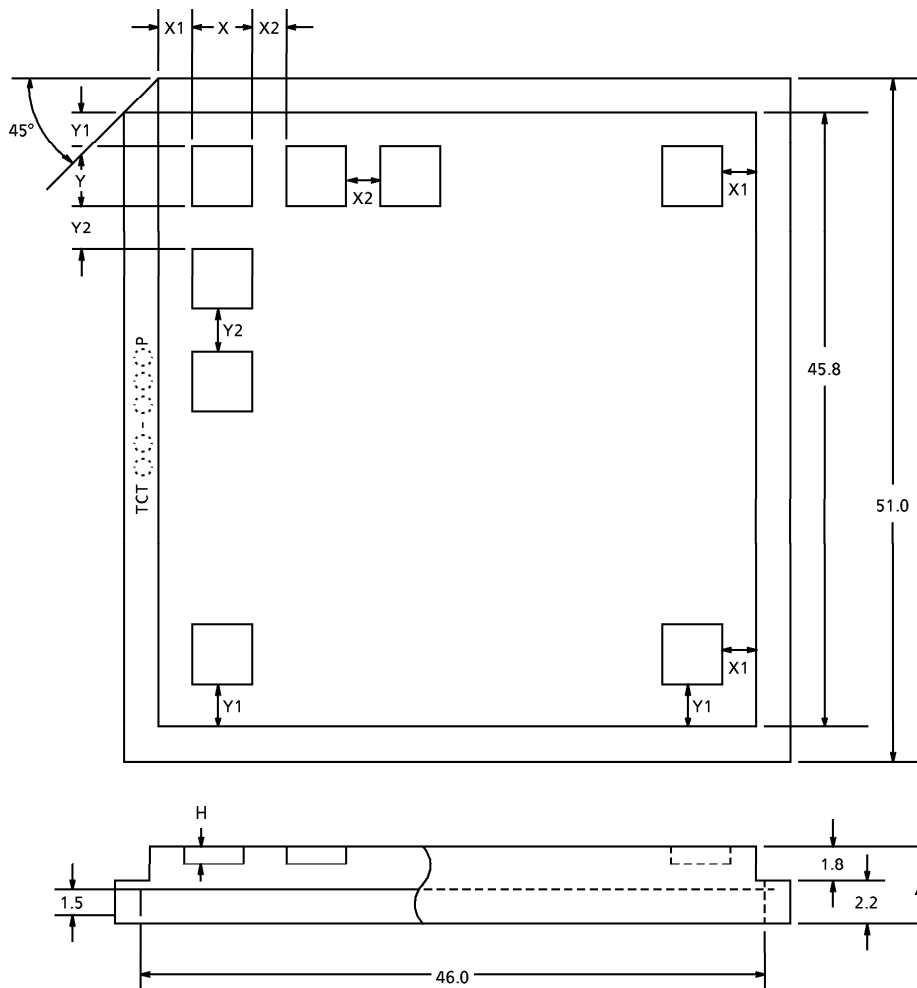

Fig.1
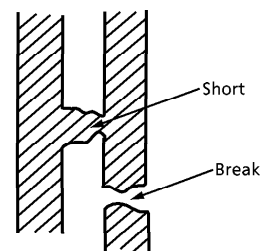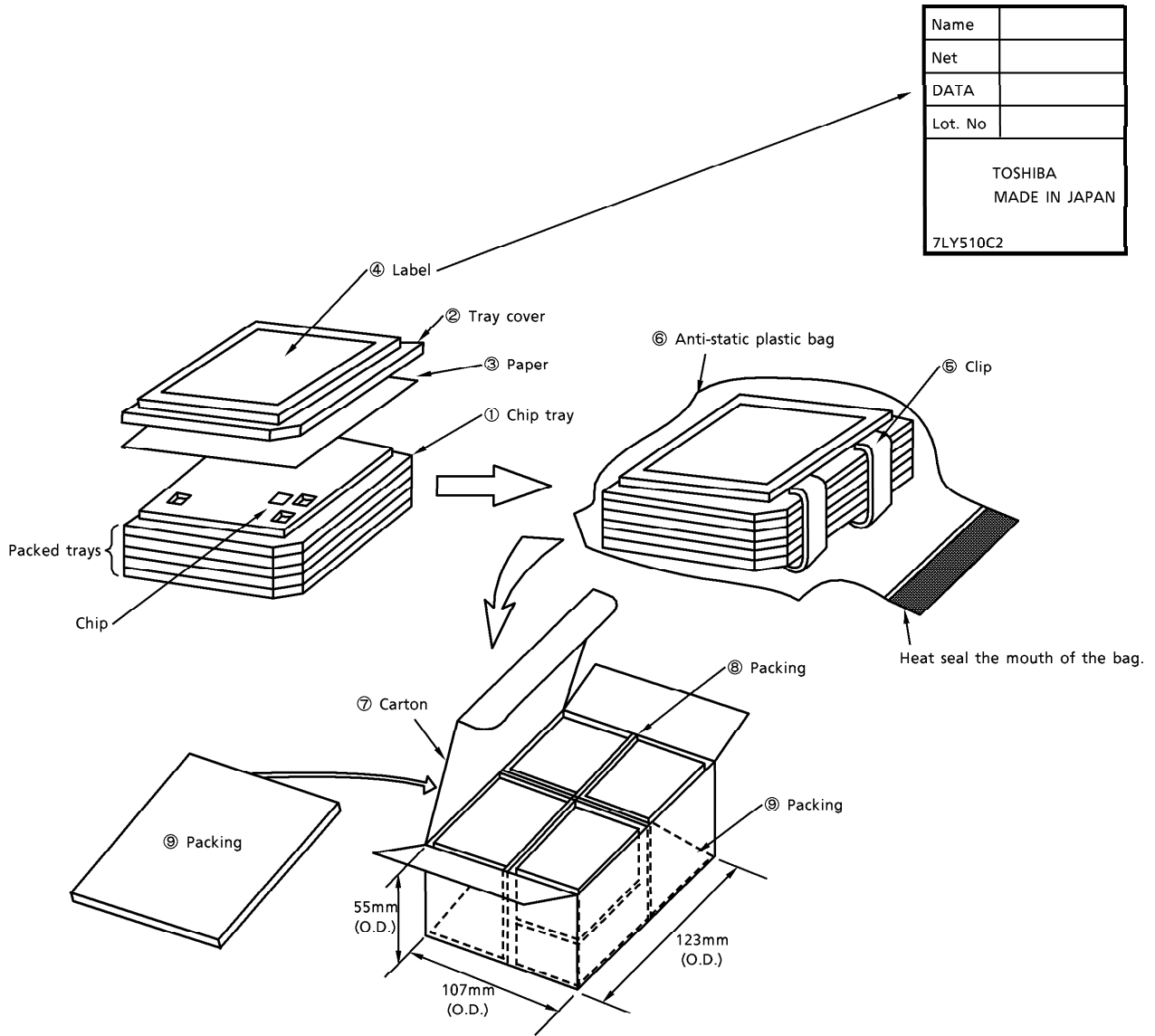

Fig.2   Lead pattern
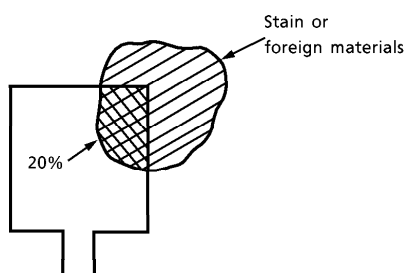
Fig.3

OUTSIDE DIMENSIONS OF CHIP TRAY

Unit : mm

CHIP NAME	TRAY NAME	X	Y	(H)	No. OF POCKETS	X1	X2	Y1	Y2
JT6M74A-AS	TCT45-060P	4.50	4.50	0.60	7×7 (49)	2.050	1.700	2.050	1.700

Tray material :

　　Carbon-containing polypropylene

PACKING METHOD-1

Name	
Net	
DATA	
Lot. No	

TOSHIBA
MADE IN JAPAN

7LY510C2

④ Label

② Tray cover

⑥ Anti-static plastic bag

⑤ Clip

③ Paper

① Chip tray

Packed trays

Chip

Heat seal the mouth of the bag.

⑧ Packing

⑦ Carton

⑨ Packing

⑨ Packing

55mm (O.D.)

123mm (O.D.)

107mm (O.D.)

Place eight bags of chip trays in each carton box ⑦. Lay one sheet of packing ⑨ (7UF44F) before closing the lid of the cart box. (See the diagram above.)

Prepare packing ⑧ by cutting 7UF44F into halves and folding each in half as shown below ; use them as inner partitions.

PACKING METHOD-2

Shipping box
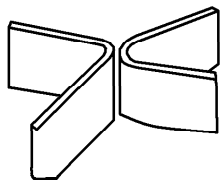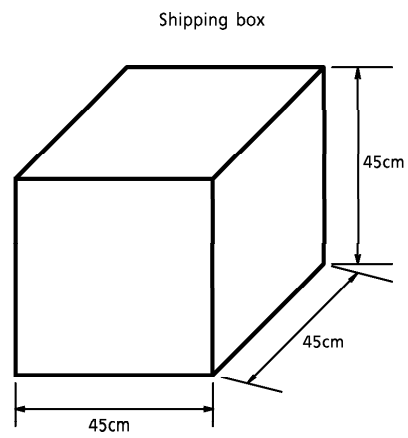
- ● Inner box   : Containing 20 boxes
- ● Weight   : Approx. 15kg (including packing material)
- ● Material   : Corrugated cardboard
- ● IC contents : $36 \times 5 \times 8 \times 20 = 28.8$kpcs.