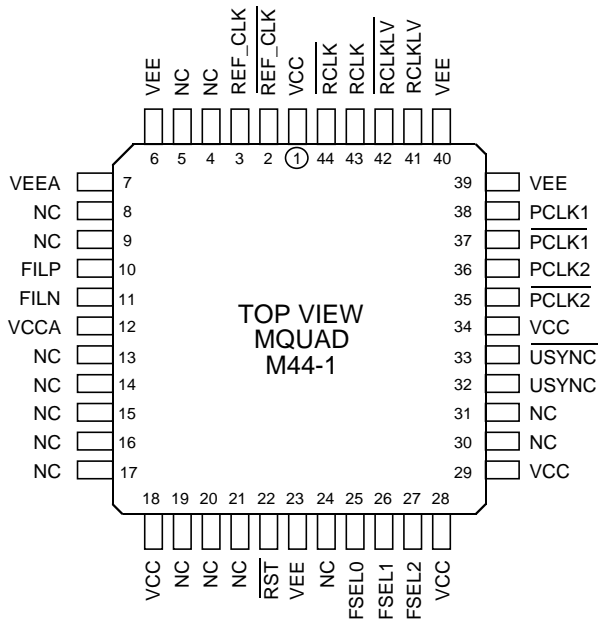


## FEATURES

- 3.3V, -1.9V power supplies
- Differential LVPECL clock input
- Differential HSTL/LVPECL outputs
- Compatible with HP PA-8000 microprocessors
- Low-jitter source for all PA-8000 required timing signals
- Available in 44-pin MQUAD package

## PIN CONFIGURATION



## DESCRIPTION

Micrel-Synergy's SY89801A PLL based clock generator provides, in a single chip, all the necessary clocks for Hewlett-Packard's PA-8000 Microprocessor.

Utilizing Micrel-Synergy's advanced PLL technology, the SY89801A accepts a Positive-ECL (PECL) reference clock input at 100MHz-132MHz, and provides precisely aligned, ultra-low-jitter ratios of frequencies necessary for the operation of the processor. In addition, the SY89801A provides the "USYNC" synchronizing signals as required by the PA-8000. The frequency ratios are 1:1, 4:3, 3:2, 5:3 and 2:1.

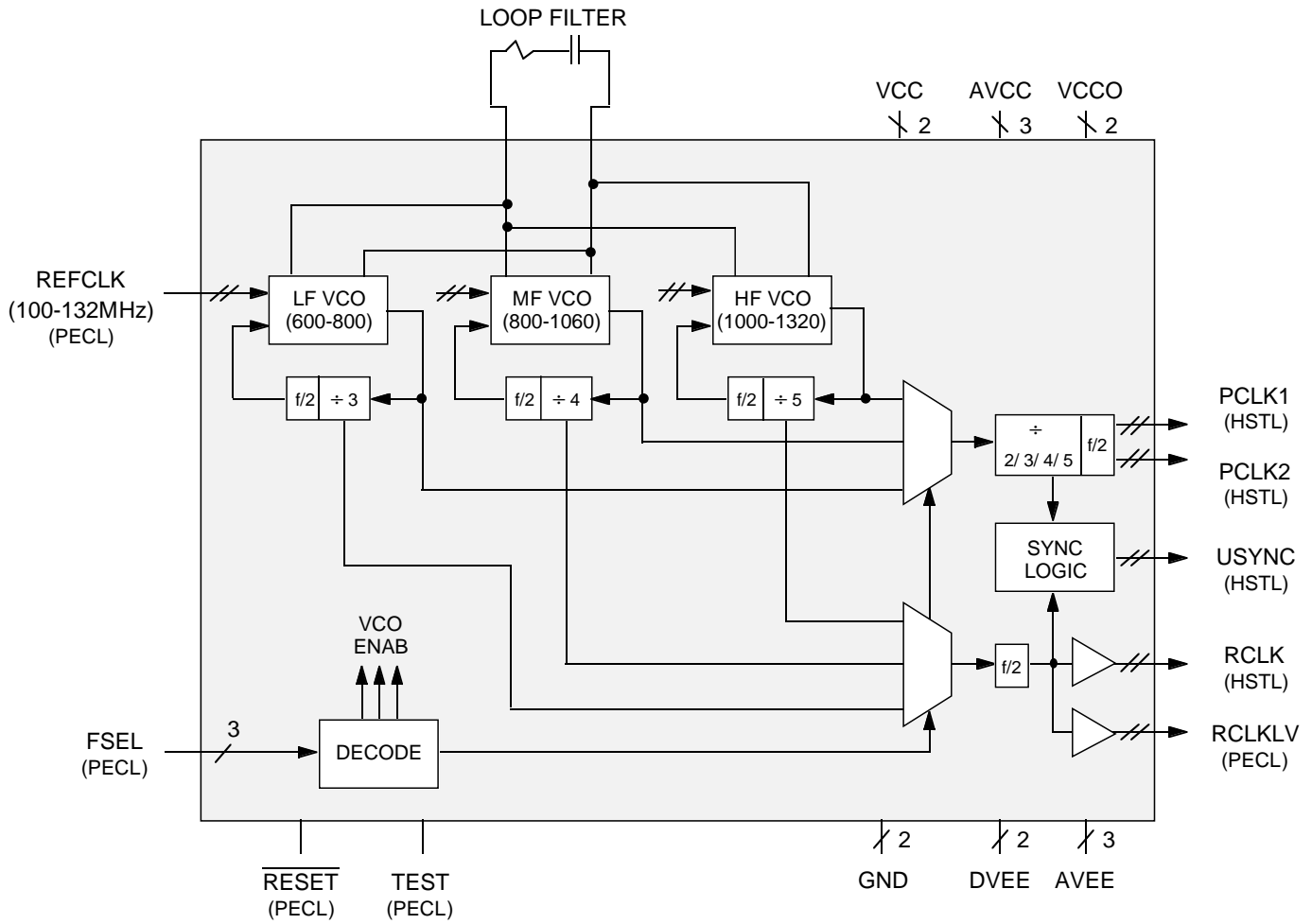
To facilitate direct interfacing to the PA-8000, the SY89801A operates across +3.3 volt and -1.9 volt supplies. The processor clock (PCLK), runway clock (RCLK), and USYNC outputs are HSTL-compatible. Additionally, there is a PECL-compatible runway clock output (RCLKLV). The SY89801A requires only a simple external series-RC loop filter.

Coupling Micrel-Synergy's advanced PLL technology with our proprietary ASSET bipolar process has produced a Timing Generator IC which meets the stringent requirements of the PA-8000  $\mu$ P, while setting a new standard for performance and flexibility.

## PIN NAMES

Pin	Function
REF_CLK, $\overline{\text{REF\_CLK}}$	Differential Input Ref. Clock
FILP, FILN	Filter Pins (Positive & Negative)
VCCA, VEEA	Analog VCC, VEE
$\overline{\text{RST}}$	Master Reset
FSEL2-0	LVPECL Frequency Select Pins
USYNC, $\overline{\text{USYNC}}$	Diff. HSTL Sync Signal for PA-8000
PCLK1-2, $\overline{\text{PCLK1-2}}$	Diff. HSTL Processor Clock Signal
RCLK, $\overline{\text{RCLK}}$	Diff. HSTL Runway Clock Signal
RCLKLV, $\overline{\text{RCLKLV}}$	Diff. LVPECL Clock Signal

**BLOCK DIAGRAM**



**3.3V DC ELECTRICAL CHARACTERISTICS**

VCC = VCCA = 3.3V ±10%; VEEA = VEE = -1.9V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VCC	Power Supply Voltage	3.0	—	3.6	V	VEE = -1.9V
Icc	Power Supply Current (Vcc)	—	250	321	mA	

**PECL DC ELECTRICAL CHARACTERISTICS**

VCC = 3.3V ±10%; VEE = -1.9V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VOH	Output HIGH Voltage	VCC - 1.075	—	VCC - 0.830	V	
VOL	Output LOW Voltage	VCC - 1.860	—	VCC - 1.570	V	
VIH	Input HIGH Voltage	VCC - 1.165	—	VCC - 0.880	V	
VIL	Input LOW Voltage	VCC - 1.810	—	VCC - 1.475	V	
VBB	PECL Threshold	—	VCC - 1.35	—	V	

**HSTL DC ELECTRICAL CHARACTERISTICS**

VCC = 3.3V ±10%; VEE = -1.9V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VOH	Output HIGH Voltage	VCC - 2.3	—	VCC - 2.1	V	
VOL	Output LOW Voltage	VCC - 3.1	—	VCC - 2.9	V	

**AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

VCC = 3.3V ±10%; VEE = -1.9V

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +70°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
fVCO	Maximum VCO Frequency	1320	—	—	1320	—	—	1320	—	—	MHz	
fMAX	Maximum PCLK Output Frequency	264	—	—	264	—	—	264	—	—	MHz	
	Maximum RCLK Output Frequency	132	—	—	132	—	—	132	—	—	MHz	
tskew <sup>(2)</sup>	PCLK to PCLK	—	—	±50	—	—	±50	—	—	±50	ps	Measured at differential crossover
	RCLK to RCLKLV	—	—	±100	—	—	±100	—	—	±100	ps	
	PCLK to RCLK	—	—	±100	—	—	±100	—	—	±100	ps	
	PCLK (neg.) to USYNC	—	—	±500	—	—	±500	—	—	±500	ps	
tpe	Phase Error RCLK to REF_CLK	—	—	±250	—	—	±250	—	—	±250	ps	
tj <sup>(2)</sup>	Output Jitter	-50	—	+50	-50	—	+50	-50	—	+50	ps	Peak to Peak, Cycle to Cycle
tdc <sup>(2)</sup>	Output Duty Cycle	49	—	51	49	—	51	49	—	51	%	
tr <sup>(2)</sup> tf	Rise/Fall Times (20% to 80%)	100	—	800	100	—	800	100	—	800	ps	

**NOTES:**

- All HSTL outputs terminated into 50 ohms in parallel with 3pf to GND.
- tskew, tj, tdc, tr and tf are specified by HP for the PA-8000. This is our best information as of the date of this document.

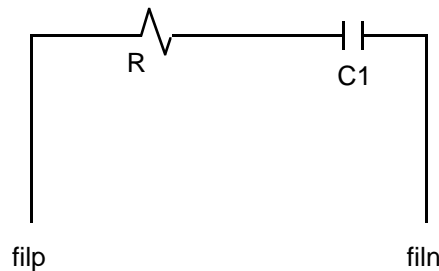
**APPLICATIONS INFORMATION**

The following table lists the various PCLK and RCLK ratios supported by the SY89801A and the corresponding PCLK, RCLK, FB and VCO frequencies. The table is arranged in order of increasing PCLK:RCLK ratio. The table was designed to balance several constraints:

- 2.5:1 VCO frequency range
- Maximum system frequency of 120MHz plus 10% margin
- Maximum output frequency of 264MHz

FSEL <2:0>	PCLK:RCLK	fPCLK (MHz)	fRCLK (MHz)	VCO ÷ ratios VCO/P:VCO/R	fVCO (MHz)
000	1:1	100-132	100-132	8:8	800-1056
001	4:3	133.3-176	100-132	6:8	800-1056
010	3:2	150-198	100-132	4:6	600-792
011	5:3	166.7-220	100-132	6:10	1000-1320
100	2:1	200-264	100-132	4:8	800-1056
101	1:1	100-132	100-132	6:6	600-792
110	1:1	100-132	100-132	10:10	1000-1320
111	n/a	n/a	n/a	n/a	n/a

**LOOP FILTER COMPONENT SELECTION**



R = 500Ω ±10%

C1 = 1000pF ±10%

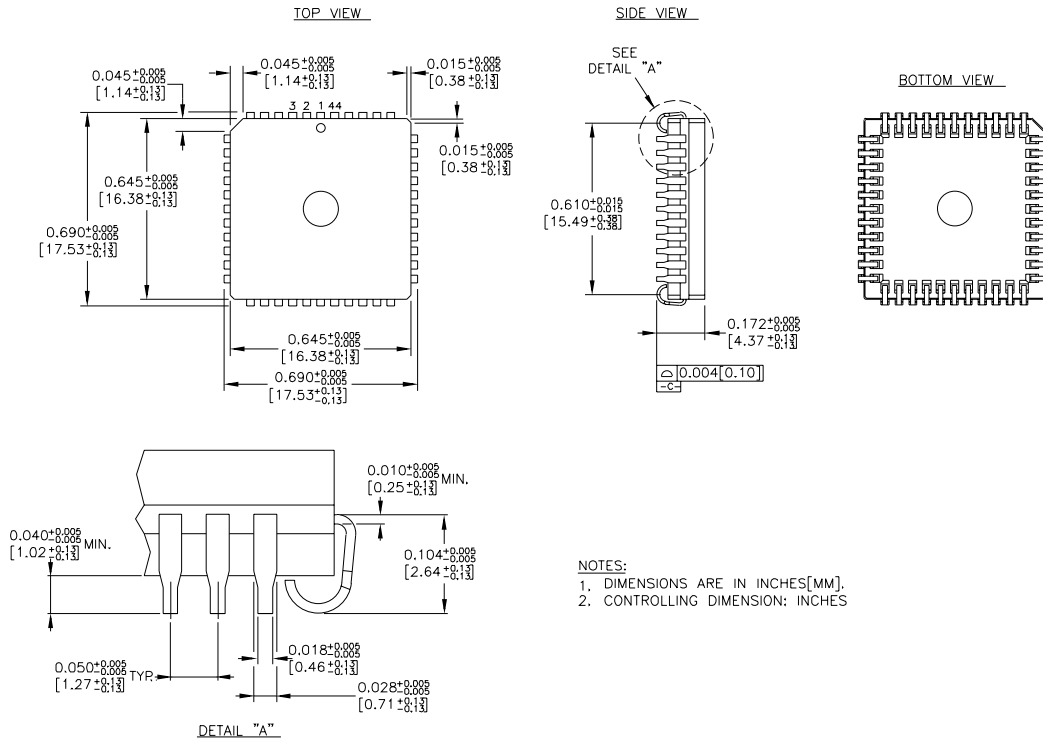
**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY89801AMC	M44-1	Commercial
SY89801AMCA <sup>(1)</sup>	M44-1	Commercial

**NOTES:**

1. "A" denotes enhanced 200MHz testing.

**44 LEAD MLCC (M44-1)**



Rev. 02

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