5V/3.3V 3.2Gbps HIGH-SPEED LIMITING POST AMPLIFIER

SY88993V

FEATURES

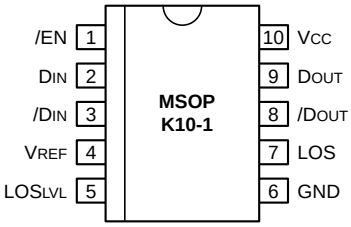
- **> 3.2Gbps operation**
- **3.3V or 5V power supply option**
- **Low noise CML data outputs**
- **Chatter-Free LOS generation**
- **Open Collector TTL LOS output**
- **TTL /EN Input**
- **Differential PECL inputs for data**
- **Single power supply**
- **Available in a tiny 10-pin (3mm) MSOP**

DESCRIPTION

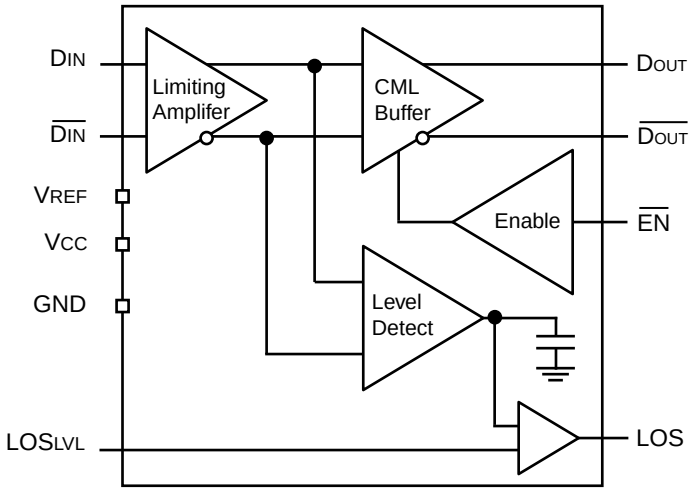
The SY88993V limiting post amplifier with its high and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 3.2Gbps. Signals as small as 4mVp-p can be amplified to drive devices with CML inputs. The SY88993V generates a chatter-free Loss of Signal (LOS) open collector TTL output.

The SY88993V incorporates a programmble level detect function to identify when the input signal has been lost. This information can be fed back to the /EN input of the device to maintain stability under loss of signal conditions. Using LOS_{LVL} pin the sensitivity of the level detect can be adjusted. The LOS_{LVL} voltage can be set by connecting a resistor divider between V_{CC} and V_{REF}, Figure 2.

PIN CONFIGURATION



BLOCK DIAGRAM



APPLICATIONS

- **1.25Gbps Gigabit Ethernet**
- **531Mbps and 1062Mbps Fibre Channel**
- **622Mbps SONET**
- **Gigabit interface converter**
- **2.5Gbps SDH/SONET**

PIN NAMES

Pin	Type	Function
D_{IN}	Data Input	Data Input
$/D_{IN}$	Data Input	Inverting Data Input
LOS_{LVL}	Input	Loss of Signal Level Set
/EN	TTL Input	Output Enable (Active Low)
LOS	TTL Output (Open Collector)	Loss of Signal Indicator (Active High)
GND	Ground	Ground
D_{OUT}	CML Output	Data Output
$/D_{OUT}$	CML Output	Inverting Data Output
V_{CC}	Power Supply	Positive Power Supply
V_{REF}	Output	Reference Voltage Output for LOS Level Set (see Fig. 3)

GENERAL DESCRIPTION

General

The SY88993V is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical transimpedance amplifiers found within a fiber-optics link. The linear signal output from a transimpedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The SY88993V limiting amplifier quantizes the signal and outputs a voltage-limited waveform.

The /EN pin allows the user to disable the output signal without removing the input signal.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	0 to +7.0	V
D_{IN}, $/D_{IN}$	Input Voltage	0 to V_{CC}	V
T_A	Operating Temperature Range	–40 to +85	°C
T_{store}	Storage Temperature Range	–55 to +125	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5V ±10%, R_{LOAD} = 50Ω to V_{CC}

Symbol	Parameter		T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
			Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{CC}	Power Supply Current[1]	5V	—	40	—	40	—	34	40	—	45	mA
		3.3V	—	35	—	35	—	30	35	—	40	mA
I_{IL}	/EN Input LOW–0.3[8] Current		—	–0.3[6]	—	–0.3[6]	—	—	–0.3[8]	—	mA	
I_{IH}	/EN Input HIGH Current		—	20[4]	—	20[4]	—	—	20[4]	—	20[4]	µA
			—	100[5]	—	100[5]	—	—	100[5]	—	100[5]	
I_{OH}	LOS Output Leakage[2]		—	100	—	100	—	—	100	—	100	uA
LOS_{LVL}	LOS_{LVL} Level		V_{REF}	V_{CC}	V_{REF}	V_{CC}	V_{REF}	—	V_{CC}	V_{REF}	V_{CC}	V
V_{OL}	LOS Output Low Level[3]		—	0.5	—	0.5	—	—	0.5	—	0.5	V
V_{REF}	Reference Voltage		V_{CC} –1.38	V_{CC} –1.26	V_{CC} –1.38	V_{CC} –1.26	V_{CC} –1.38	V_{CC} –1.32	V_{CC} –1.26	V_{CC} –1.38	V_{CC} –1.26	V
V_{IH}	/EN Input HIGH Voltage		2.0	—	2.0	—	2.0	—	—	2.0	—	V
V_{IL}	/EN Input LOW Voltage		—	—	0.8	—	0.8	—	—	0.8	—	V
V_{OFFSET}	Differential Output Offset		—	±80	—	±80	—	±10	±80	—	±80	mV
V_{CMR}	Common Mode Range		GND±2	V_{CC}–0.2	GND±2	V_{CC}–0.2	GND±2		V_{CC}–0.2	GND±2	V_{CC}–0.2	V

NOTES:

1. No output load.
2. V_{OH} = 5.5V.
3. I_{OL} = +2mA.
4. V_{IN} = 2.7V
5. V_{IN} = V_{CC}
6. V_{IN} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5V ±10%, R_{LOAD} = 50Ω to V_{CC}

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
HYS	LOS Hysteresis	2	8	2	8	2	5.6	8	2	8	dB
PSRR	Power Supply[1] Rejection Ratio	—	—	—	—	—	35	—	—	—	dB
t_{OFFL}	LOS Release Time[2] Minimum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	µs
t_{OFFH}	LOS Release Time[3] Maximum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	µs
t_{ONL}	LOS Assert Time[2]	—	0.5	—	0.5	—	0.2	0.5	—	0.5	µs
t_r, t_f	Differential Output[3] Rise/Fall Time	—	120	—	120	—	70	120	—	120	ps
V_{ID}	Input Voltage Range	4	1800	4	1800	4	—	1800	4	1800	mVp-p
V_{OD}	Differential Output Voltage Swing[4]	—	—	—	—	—	400[5]	—	—	—	mVp-p
V_{SR}	LOS Sensitivity Range	4	50	4	50	4	—	50	4	50	mVp-p
Output Spec (D_{OUT} and $/D_{OUT}$)											
V_{OH}	HIGH Level Output Voltage	V_{CC} –20	V_{CC}	V_{CC} –20	V_{CC}	V_{CC} –20	V_{CC} –5	V_{CC}	V_{CC} –20	V_{CC}	mV
V_{OL}	LOW Level Output[6] Voltage	V_{CC} –280	V_{CC} –140	V_{CC} –280	V_{CC} –140	V_{CC} –280	V_{CC} –200	V_{CC} –140	V_{CC} –280	V_{CC} –140	mV
Z_O	Single-Ended Output[7] Impedance	40	60	40	60	40	50	60	40	60	Ω
Input Spec (D_{IN} and $/D_{IN}$)											
$A_{V(Diff)}$	Differential Voltage Gain	—	—	—	—	—	38	—	—	—	dB
$B_{–3dB}$	3dB Bandwidth	—	—	—	—	—	2.5	—	—	—	GHz
S_{21}	Single-Ended Small Signal-Gain	26	—	26	—	26	32	—	26	—	dB

NOTES:

1. Input referred noise = RMS output noise/low frequency gain. Input referred, 55MHz.
2. Input is a 200MHz square wave, t_r < 300ps, 1.8Vp-p.
3. With input signal V_{ID} > 5mVp-p.
4. Input is a 200MHz square wave, t_r < 300ps, 50Ω load.
5. V_{ID} > 5mVp-p.
6. Output levels are based on 50Ω impedance. If the load impedance is different, the output level will be changed.
7. See output structure.

APPLICATION NOTE

Output Termination

The SY88993V outputs must be terminated with a 50Ω load to VCC.

Layout and PCB Design

Since the SY88993V is a high-frequency component, performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via power supply.

The SY88993V ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

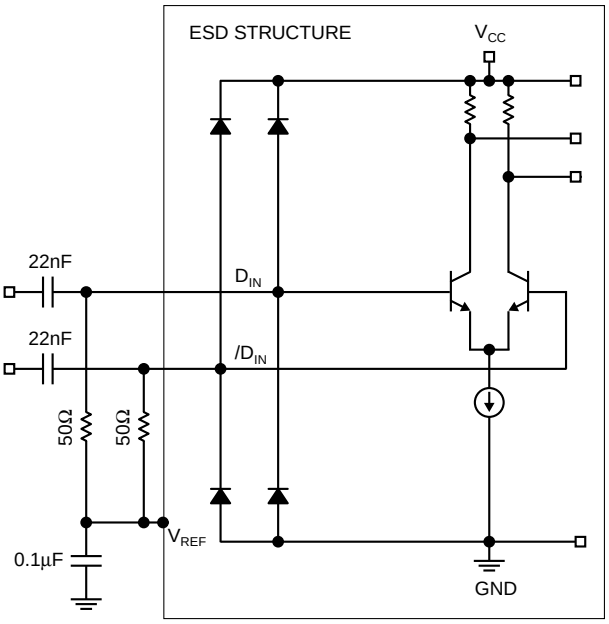


Figure 1. Differential Input Configuration

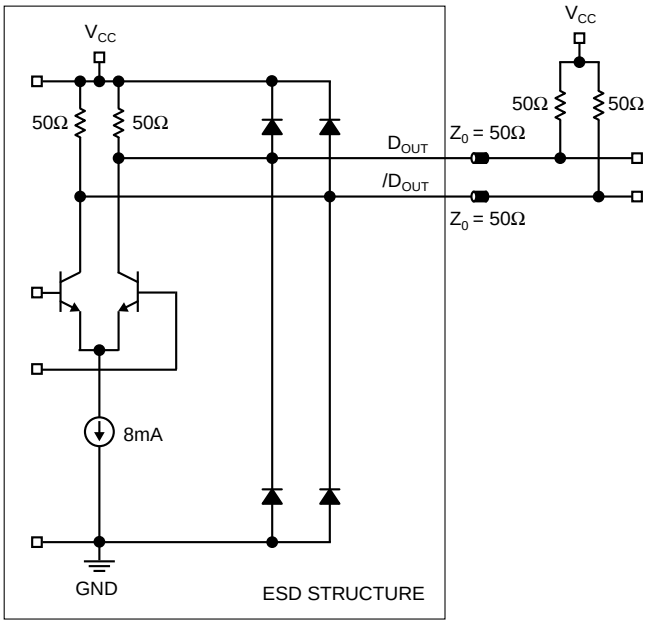
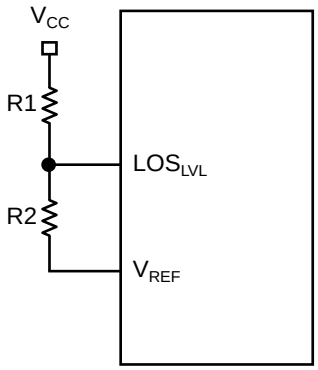


Figure 2. Differential Output Configuration



NOTES:

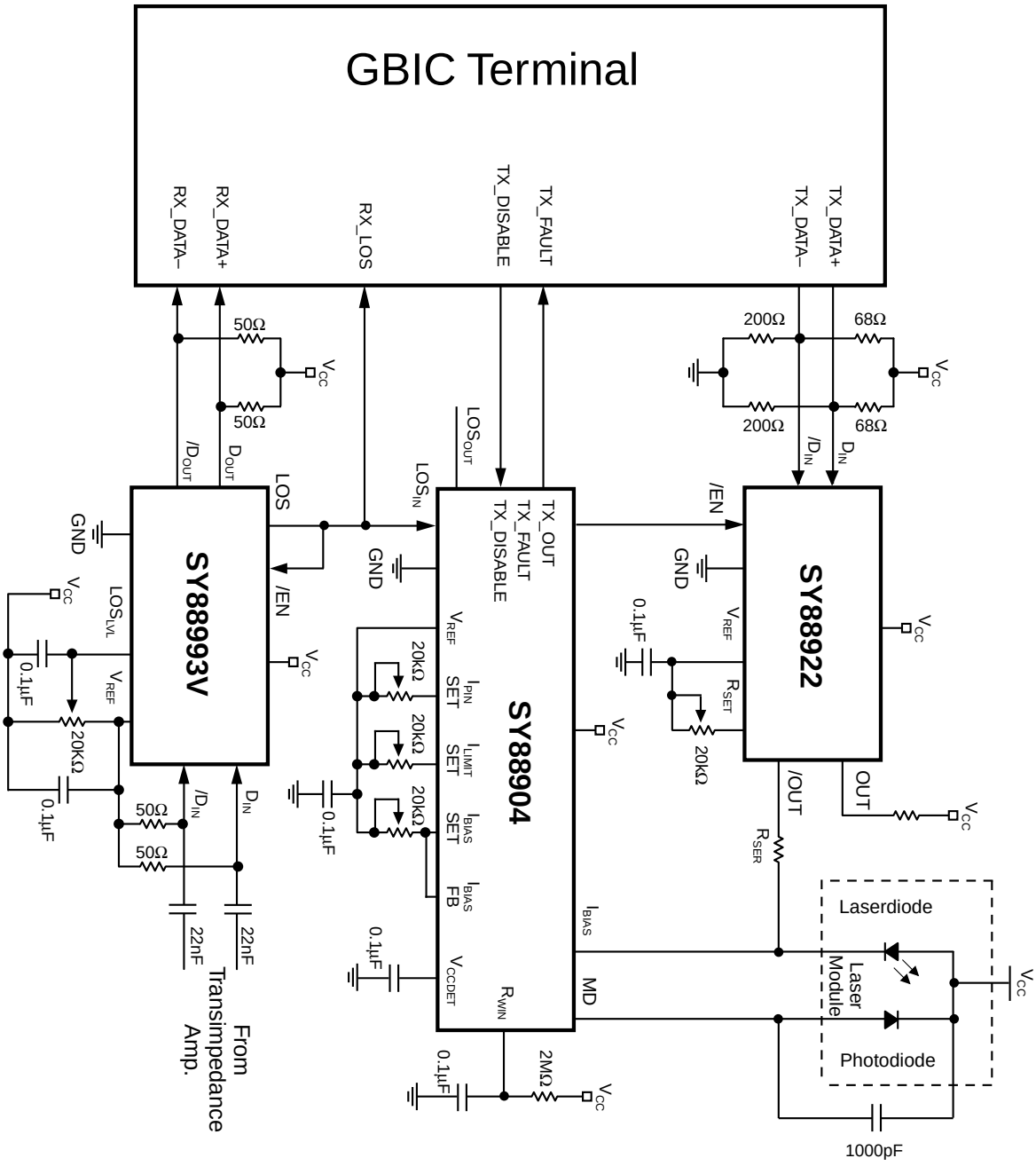
1. Resistor Divider = R2/ (R1 + R2)
2. R1 + R2 ≥ 5kΩ

Figure 3. LOS_{LVL} Circuit

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY88993VKC	K10-1	Commercial

APPLICATION EXAMPLE FOR 3-CHIP SET SOLUTION



PERFORMANCE CURVE

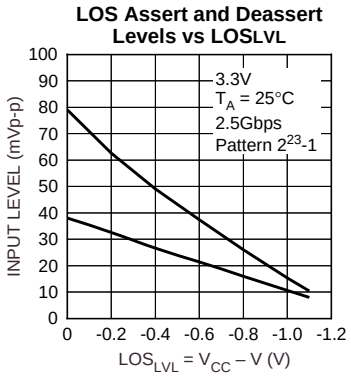


Figure 4.

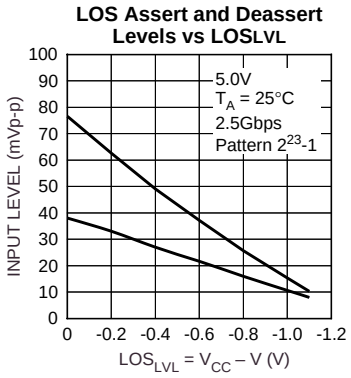


Figure 5.

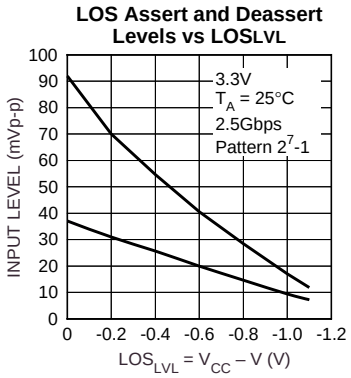


Figure 6.

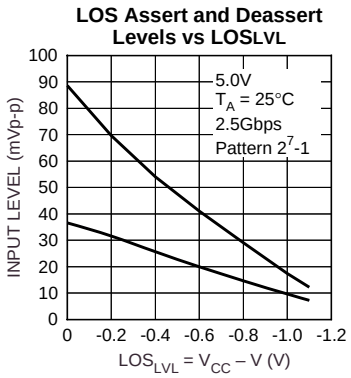
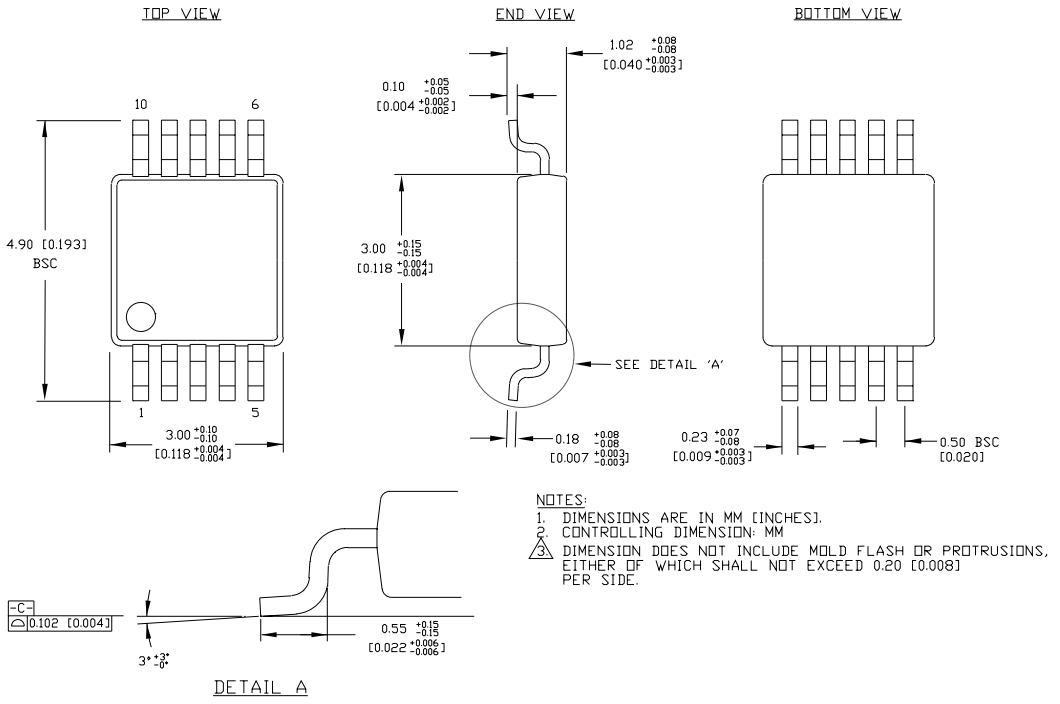


Figure 7.

10 LEAD MSOP (K10-1)



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

Rev. 00

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