NT7703

160 Output LCD Segment/Common Driver

Features

(Segment mode)

- Shift Clock frequency:
  14 MHz (Max.) (V_{DD} = 5V ± 10%)
  8 MHz (Max.) (V_{DD} = 2.5V - 4.5V)
- Adopts a data bus system
- 4-bit / 8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function with an enable signal
- Automatic counting function when in “chip select” mode, which causes the internal clock to be stopped by automatically counting 160 bits of input data

(Common mode)

- Shift clock frequency:
  4.0MHz (Max.)
- Built-in 160-bits bidirectional shift register (divisible into 80-bits x 2)
- Available in a single mode (160-bits shift register) or in a dual mode (80-bits shift register x 2)
  1. Y1 → Y160 Single mode
  2. Y160 → Y1 Single mode
  3. Y1 → Y80, Y81 → Y160 Dual mode
  4. Y160 → Y81, Y80 → Y1 Dual mode

  The above 4 shift directions are pin-selectable

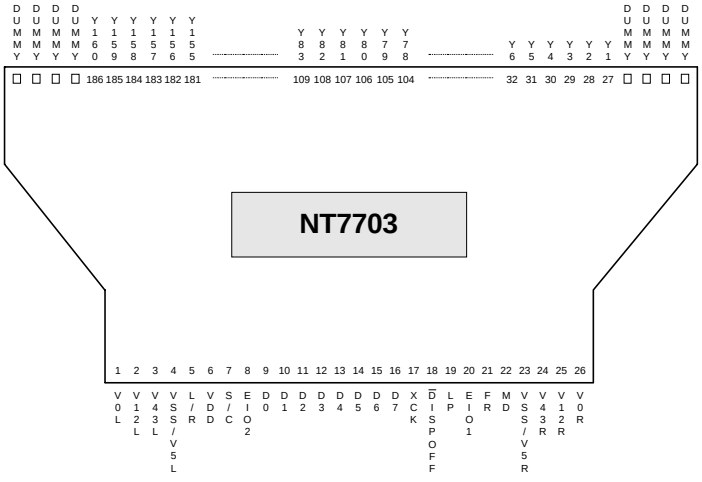
(Both segment mode and common mode)

- Supply voltage for LCD drive: 15.0 to 30.0V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5V
- COMS process
- Package: Gold bump die / 186 Pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

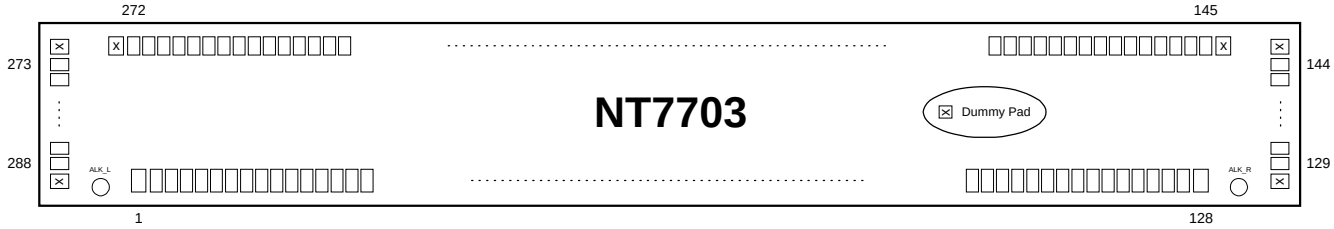
General Description

The NT7703 is a 160-bit output segment/common driver LSI suitable for driving the large scale dot matrix LCD panels used by PDA's, personal computers and work stations for example. Through the use of COG technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The NT7703 is good as both a segment driver and a common driver, and a low power consuming, high-precision LCD panel display can be assembled using the NT7703. In the segment mode, the data input is selected as 4bit parallel input mode or as 8bit parallel input mode by a mode (MD) pin. In common mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

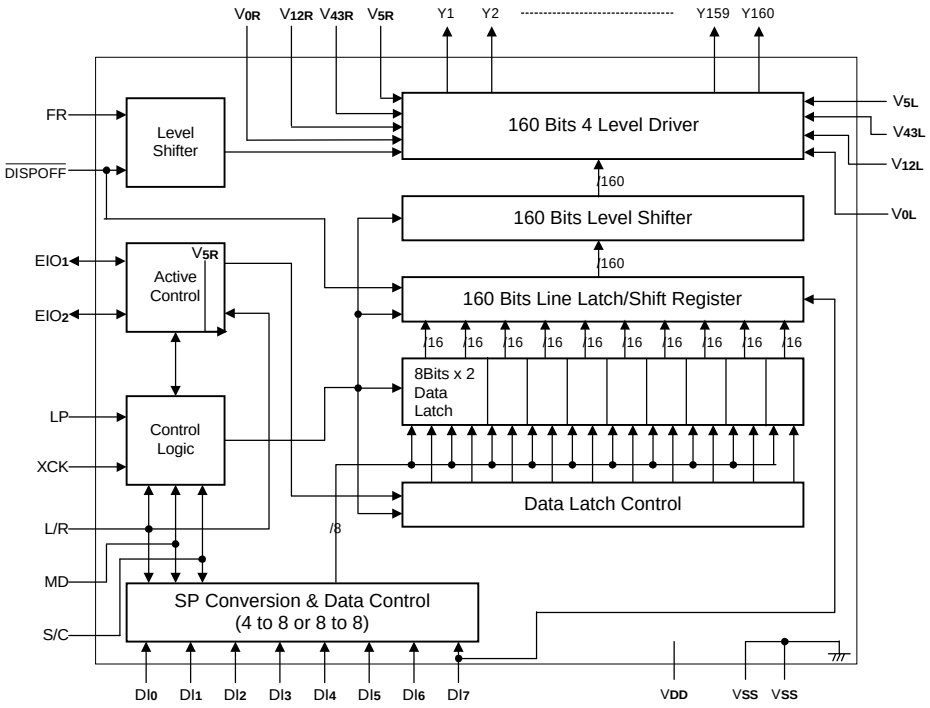
Pin Configuration



Pad Configuration



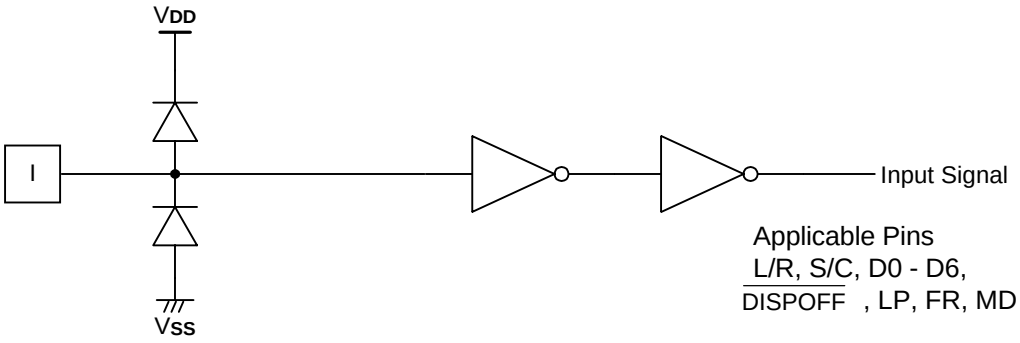
Block Diagram



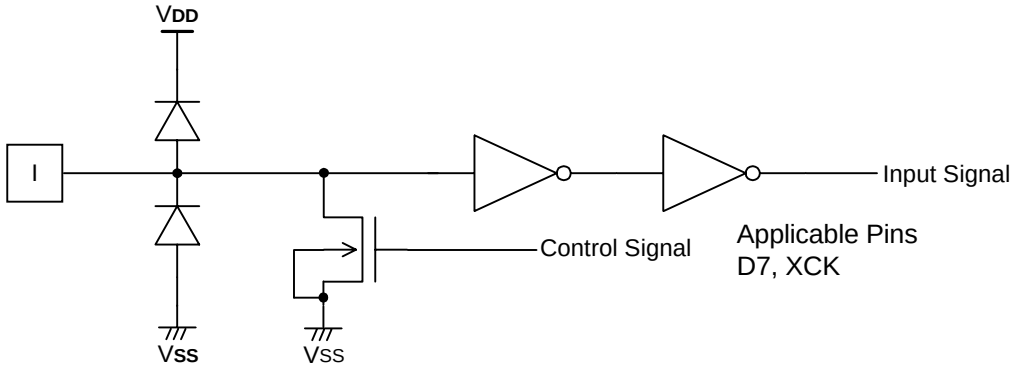
Pad Description

Pad No.	Designation	I/O	Description
1 - 7	V_{0L}	P	Power supply for LCD driver
8 - 12	V_{12L}	P	Power supply for LCD driver
13 - 17	V_{43L}	P	Power supply for LCD driver
18 - 22	V_{5L}	P	Power supply for LCD driver
23 - 39	V_{SS}	P	Ground (0V), these two pads must be connected to each other
40 - 41	L/R	I	Display data shift direction selection
42 - 57	V_{DD}	P	Power supply for the logic system (+2.5 to + 5.5V)
58 - 59	S/C	I	Segment mode / common mode selection
60 - 61	EIO_2	I/O	Input / output for chip select or data of shift register
62, 63 - 74, 75	D0 - D6	I	Display data input for segment mode
76 - 77	D7	I	Display data input for Segment mode / Dual mode data input
78 - 79	XCK	I	Display data shift clock input for segment mode
80 - 81	$\overline{DISPOFF}$	I	Control input for deselect output level
82 - 83	LP	I	Latch pulse input / shift clock input for the shift register
84 - 85	EIO_1	I/O	Input / output for chip select or data of the shift register
86 - 87	FR	I	AC-converting signal input for LCD driver waveform
88 - 89	MD	I	Mode selection input
90 - 106	V_{SS}	P	Ground (0V), these two pads must be connected to each other
107 - 111	V_{5R}	P	Power supply for LCD driver
112 - 116	V_{43R}	P	Power supply for LCD driver
117 - 121	V_{12R}	P	Power supply for LCD driver
122 - 128	V_{0R}	P	Power supply for LCD driver
129 - 288	Y1 - Y160	O	LCD driver output

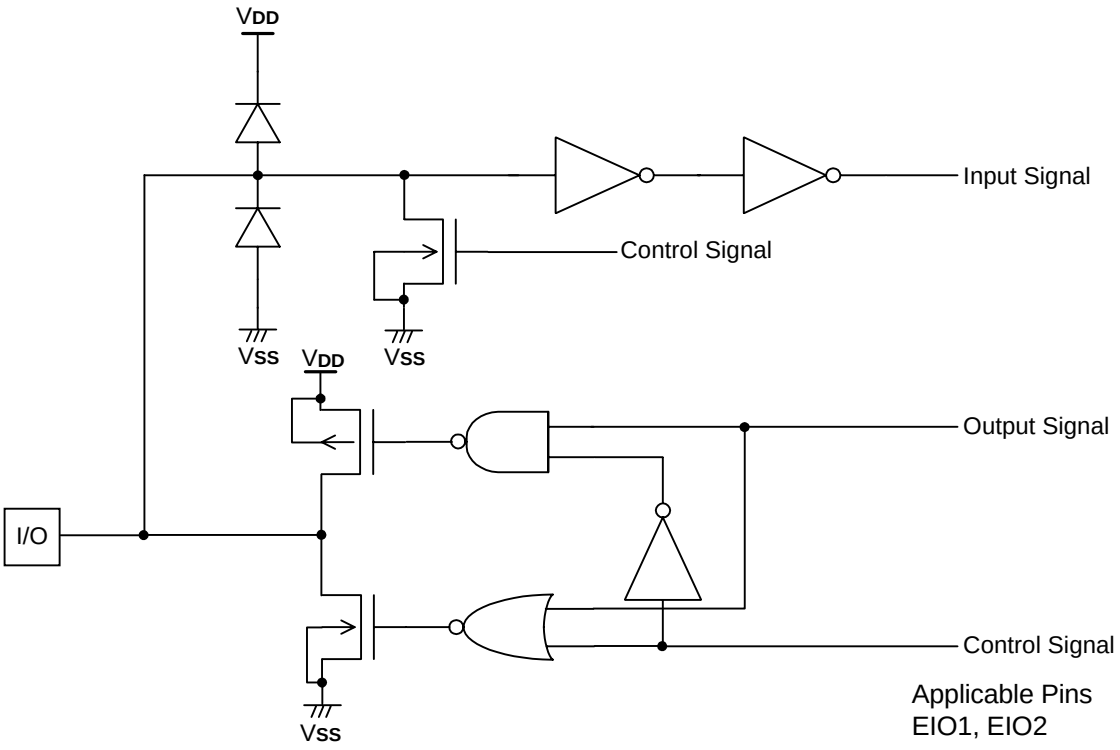
Input / Output Circuits



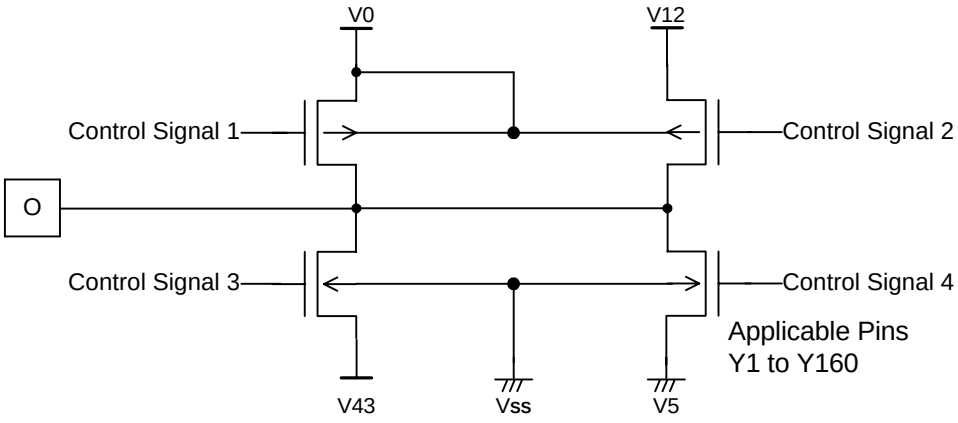
Input Circuit (1)



Input Circuit (2)



Input / Output Circuit



LCD Driver Output circuit

Pad Description

Segment mode

Symbol	Function
V_{DD}	Logic system power supply pin connects from +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{OR}, V_{OL} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{160}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43)
D_0 - D_7	Input pin for display data ● In 4-bit parallel input mode, input data into the 4 pins D_0 - D_3. Connect D_4 - D_7 to V_{SS} or V_{DD} ● In 8-bit parallel input mode, input data into the 8 pins D_0 - D_7
XCK	Clock input pin for taking display data ● Data is read on the falling edge of the clock pulse
LP	Latch pulse input pin for display data ● Data is latched on the falling edge of the clock pulse
L/R	Direction selection pin for reading display data ● When set to V_{SS} level "L", data is read sequentially from Y160 to Y1 ● When set to V_{DD} level "H", data is read sequentially from Y1 to Y160
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit ● When set to V_{SS} level “L”, the LCD driver output pins (Y1 - YI60) are set to level V_5 ● When $\overline{\text{DISPOFF}}$ is set to “L”, the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of $\overline{\text{DISPOFF}}$. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs the deselect level (V_{12} or V_{43}), then outputs the contents of the date latch onto the next falling edge of the LP At that time, if the $\overline{\text{DISPOFF}}$ removal time can not keep in regulation with what is shown on the AC characteristics, then it can not output the reading data correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls LCD driver circuit ● It normally inputs a frame inversion signal The LCD driver output pin’s output voltage level can be set to the line latch output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level “L”, 4-bit parallel input mode is set ● When set to V_{DD} level “H", 8-bit parallel input mode is set

Segment mode continued

Symbol	Function
S/C	Segment mode/common mode selection pin ● When set to V_{DD} level "H", segment mode is set ● When set to V_{SS} level "L", common mode is set
EIO_1, EIO_2	Input/output pin for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output ● During output, it is set to "H" when LP* $\overline{XCK}$ is "H" and then after 160-bits of data have been read, it is set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H" ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected
Y_1 - Y_{160}	LCD driver output pins These correspond directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Common mode

Symbol	Function
V_{DD}	Logic system power supply pin connects from +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias. ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{160}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43)
EIO_1	Bi-directional shift register shift data input/output pin ● Is an Output pin when L/R is at V_{SS} level "L" and is an input pin when L/R is at V_{DD} level "H" ● When EIO_1 is used as an input pin, it will be pulled-down ● When EIO_1 is used as an output pin, it won't be pulled-down
EIO_2	Bi-directional shift register shift data input/output pin ● Is an Input pin when L/R is at V_{SS} level "L" and is an output pin when L/R is at V_{DD} level "H" ● When EIO_2 is used as an input pin, it will be pulled-down ● When EIO_2 is used as an output pin, it won't be pulled-down
LP	Bi-directional shift register shift clock pulse input pin ● Data is shifted on the falling edge of the clock pulse
L/R	Bi-directional shift register shift direction selection pin ● Data is shifted from Y_{160} to Y_1 when it is set to V_{SS} level "L", and data is shifted from Y_1 to Y_{160} when set it is to V_{DD} level "H"

Common mode continued

Symbol	Function
$\overline{DISPOFF}$	Control input pin for output deselect level ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level and it controls the LCD driver circuit ● When set to V_{SS} level "L", the LCD driver output pins (Y_1 - Y_{160}) are set to level V_5 ● While set to "L", the contents of the shift resister are reset and are not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_{12} or V_{34}), and the shift data is read on the falling edge of the LP. At that time, if the $\overline{DISPOFF}$ removal time can not keep regulation with what is shown on the AC characteristics, then the shift data is not read correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit ● Normally, it inputs a frame inversion signal The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level "L", Single Mode operation is selected. When set to V_{DD} level "H", Dual Mode operation is selected
D_7	Dual Mode data input pin ● According to the data shift direction of the data shift register, data can be input starting from the 81st bit When the chip is used in Dual Mode, D_7 will be pulled-down When the chip is used in Single Mode, D_7 won't be pulled-down
S/C	Segment mode/common mode selection pin ● When set to V_{SS} level "L", common mode is set
D_0 - D6	Not used ● Connect D_0-D_6 to V_{SS} or V_{DD}. Avoid floating
XCK	Not used ● XCK is pulled-down in common mode, so connect to V_{SS} or leave open
Y_1 - Y_{160}	LCD driver output pins ● These correspond directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Functional Description

1. Block description

1.1. Active Control

In segment mode, it controls the selection or deselection of the chip. Following a LP signal input and after the select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for the cascade connection is output, and the ship is deselected.

In common mode, it controls the input/output data of the bidirectional pins.

1.2. SP Conversion & Data Control

In segment mode, it keeps input data, which are 2 clocks of XCK at 4-bit parallel mode in the latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel mode in the latch circuit, after which they are put on the internal data bus 8 bits at a time.

1.3. Data Latch Control

In segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

1.4. Data Latch

In segment mode, it latches the data onto the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control. 160 bits of data are read in 20 sets of 8 bits.

1.5. Line Latch / Shift Register

In segment mode, it ensures that all 160 bits which have been read into the data latch are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block.

In common mode, shifts data from the data input pin on to the falling edge of the LP signal.

1.6. Level Shifter

It ensures the logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

1.7. 4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

1.8. Control Logic

It controls the operation of each block. In segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

In common mode, it controls the direction of the data shift.

2. LCD Driver Output Voltage Level

The relationship between the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

2.1. Segment Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{160})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

2.2. Common Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{160})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which is assigned by specification for each power pin.
That time "Don't care" should be fixed to "H" or "L", avoiding floating.

3. Relationship between the Display Data and Driver Output Pins

3.1. Segment Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Number of Clock						
					40clock	39clock	38clcok	~	3clock	2clock	1clock
L	L	Output	Input	D_0	Y1	Y5	Y9	~	Y149	Y153	Y157
				D_1	Y2	Y6	Y10	~	Y150	Y154	Y158
				D_2	Y3	Y7	Y11	~	Y151	Y155	Y159
				D_3	Y4	Y8	Y12	~	Y152	Y156	Y160
L	H	Input	Output	D_0	Y160	Y156	Y152	~	Y12	Y8	Y4
				D_1	Y159	Y155	Y151	~	Y11	Y7	Y3
				D_2	Y158	Y154	Y150	~	Y10	Y6	Y2
				D_3	Y157	Y153	Y149	~	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Number of Clock						
					20clock	19clock	18clcok	~	3clock	2clock	1clock
H	L	Output	Input	D_0	Y1	Y9	Y17	~	Y137	Y145	Y153
				D_1	Y2	Y10	Y18	~	Y138	Y146	Y154
				D_2	Y3	Y11	Y19	~	Y139	Y147	Y155
				D_3	Y4	Y12	Y20	~	Y140	Y148	Y156
				D_4	Y5	Y13	Y21	~	Y141	Y149	Y157
				D_5	Y6	Y14	Y22	~	Y142	Y150	Y158
				D_6	Y7	Y15	Y23	~	Y143	Y151	Y159
				D_7	Y8	Y16	Y24	~	Y144	Y152	Y160
H	H	Input	Output	D_0	Y160	Y152	Y144	~	Y24	Y16	Y8
				D_1	Y159	Y151	Y143	~	Y23	Y15	Y7
				D_2	Y158	Y150	Y142	~	Y22	Y14	Y6
				D_3	Y157	Y149	Y141	~	Y21	Y13	Y5
				D_4	Y156	Y148	Y140	~	Y20	Y12	Y4
				D_5	Y155	Y147	Y139	~	Y19	Y11	Y3
				D_6	Y154	Y146	Y138	~	Y18	Y10	Y2
				D_7	Y153	Y145	Y137	~	Y17	Y9	Y1

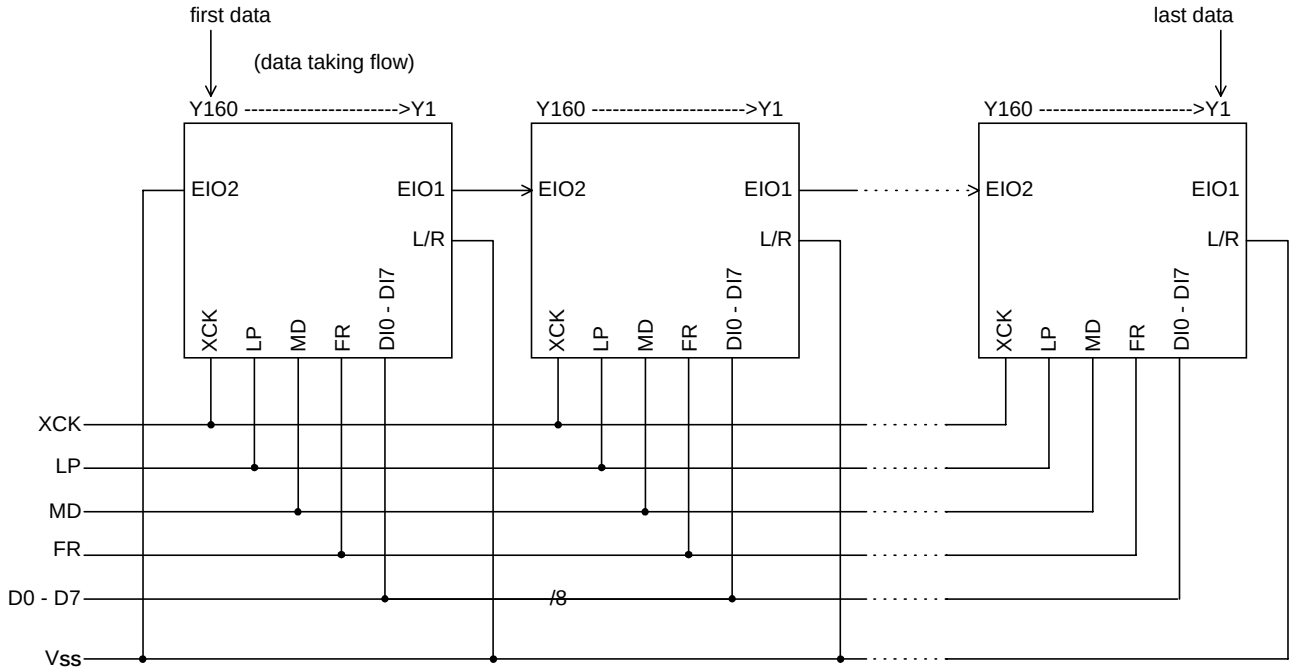
3.2. Common Mode

MD	L/R	Data Transfer Direction	EIO_1	EIO_2	D_7
L (Single)	L (shift to left)	Y160 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y160	Input	Output	X
H (Dual)	L (shift to left)	Y160 to Y81 Y80 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y80 Y81 to Y160	Input	Output	Input

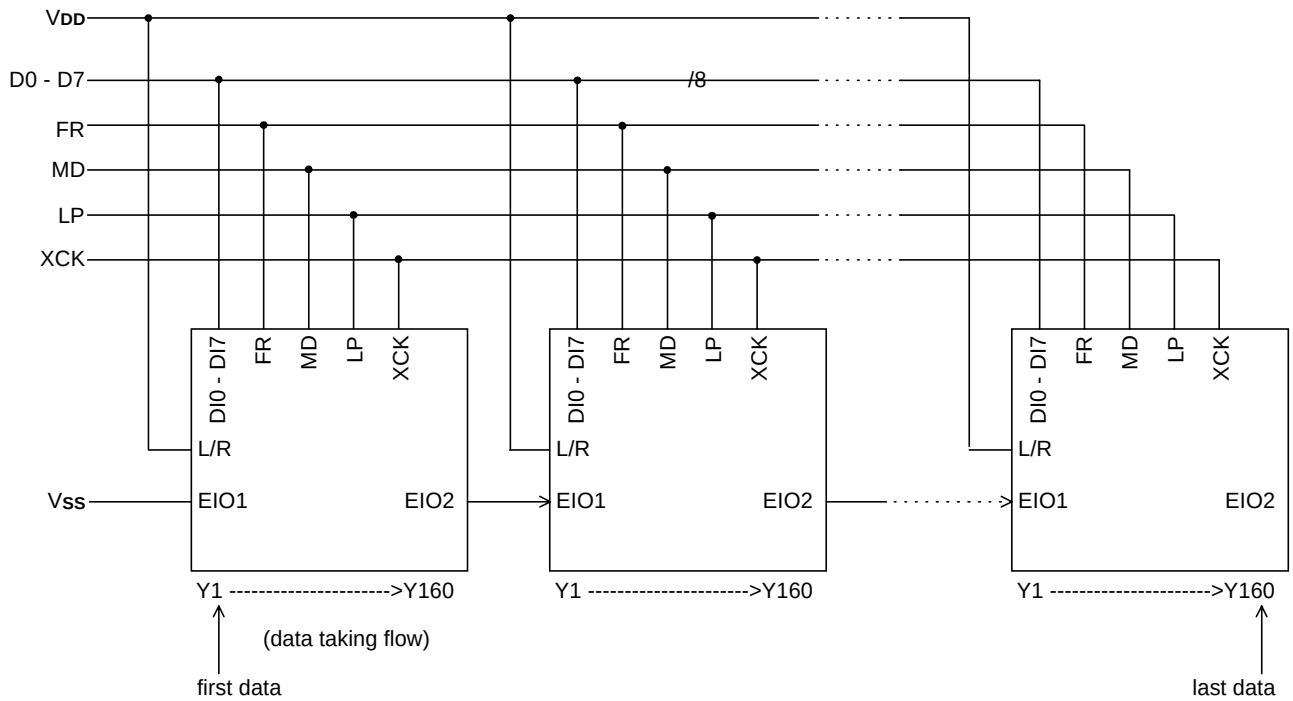
Here, L: V_{SS} (0V), H: V_{DD} (+2.5V to +5.5V), X: Don't care
Note: "Don't care" should be fixed to "H" or "L", avoiding floating.

4. Connection Examples of Segment Drivers

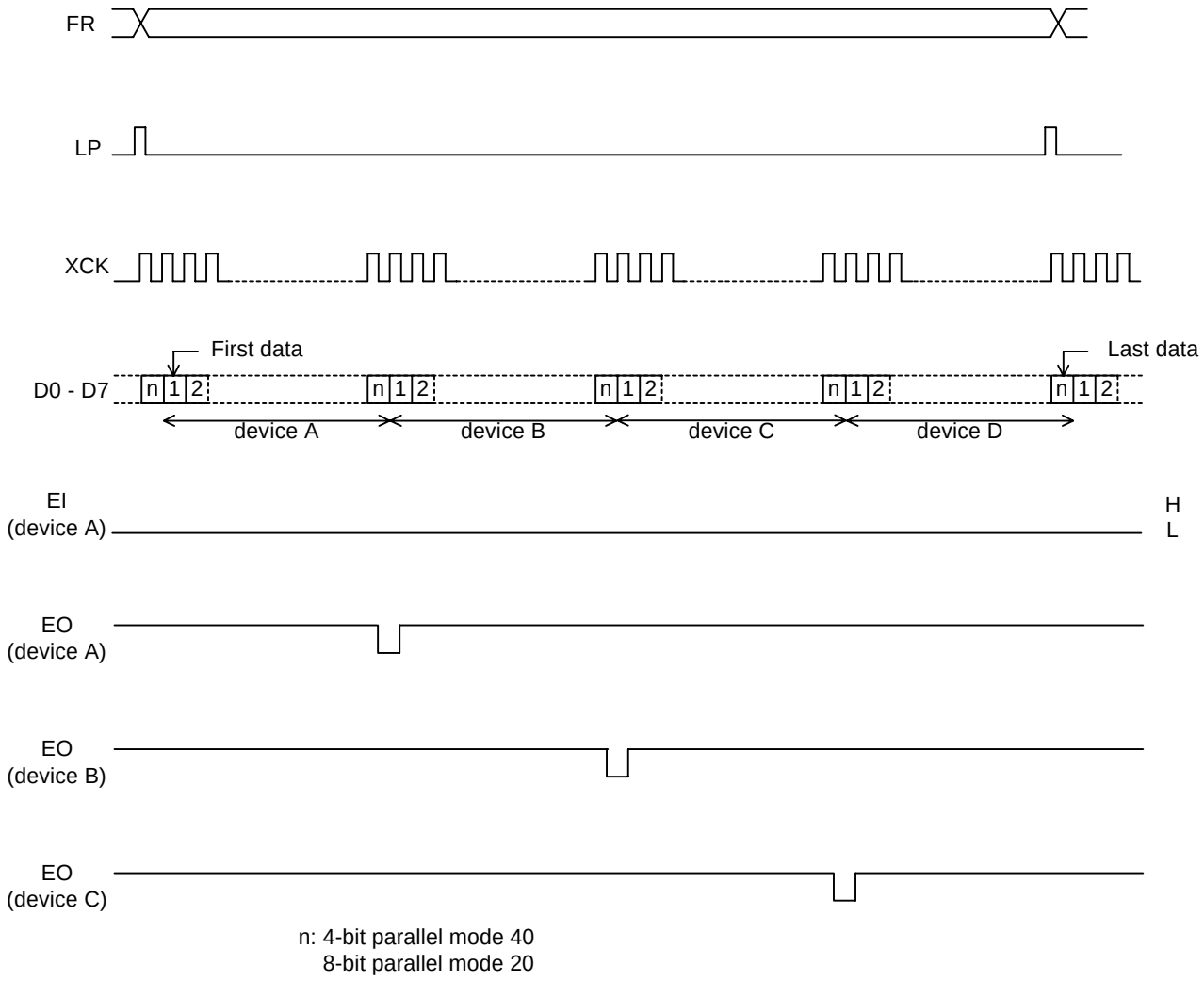
4.1. Case of L/R = “L”



4.2 Case of L/R = “H”

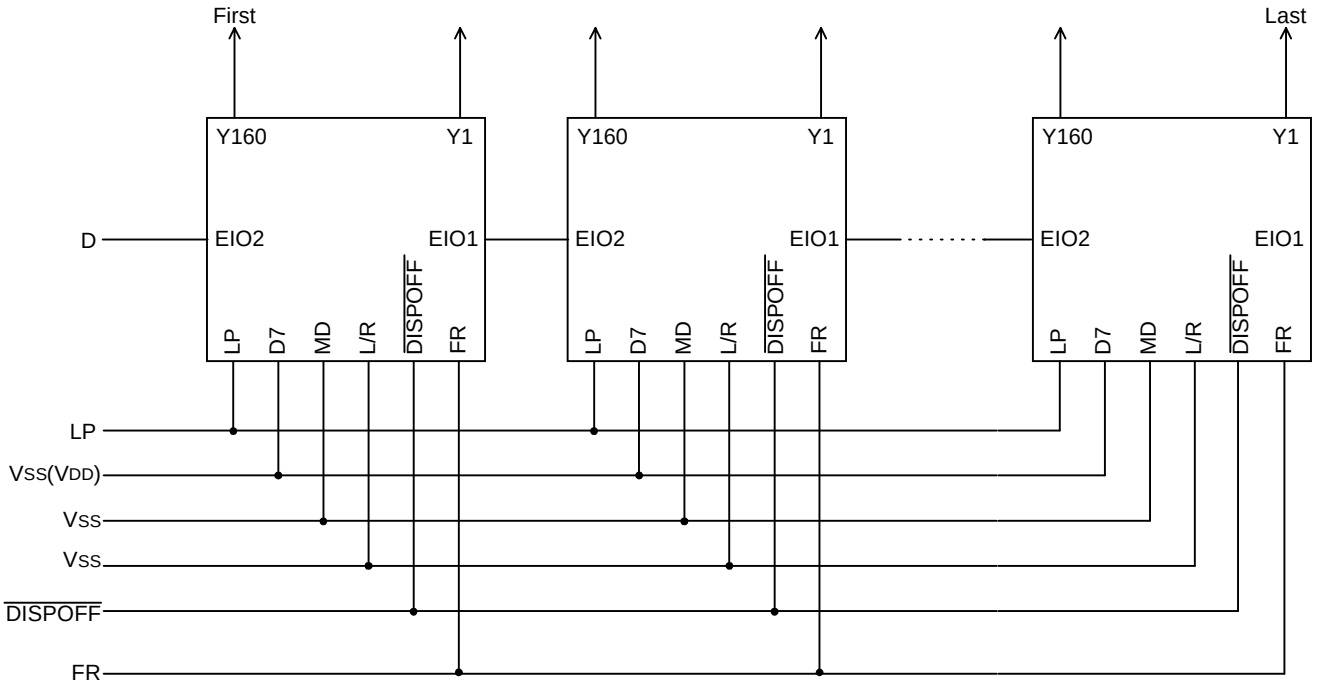


5. Timing Waveform of 4-Device Cascade Connection of Segment Drivers.

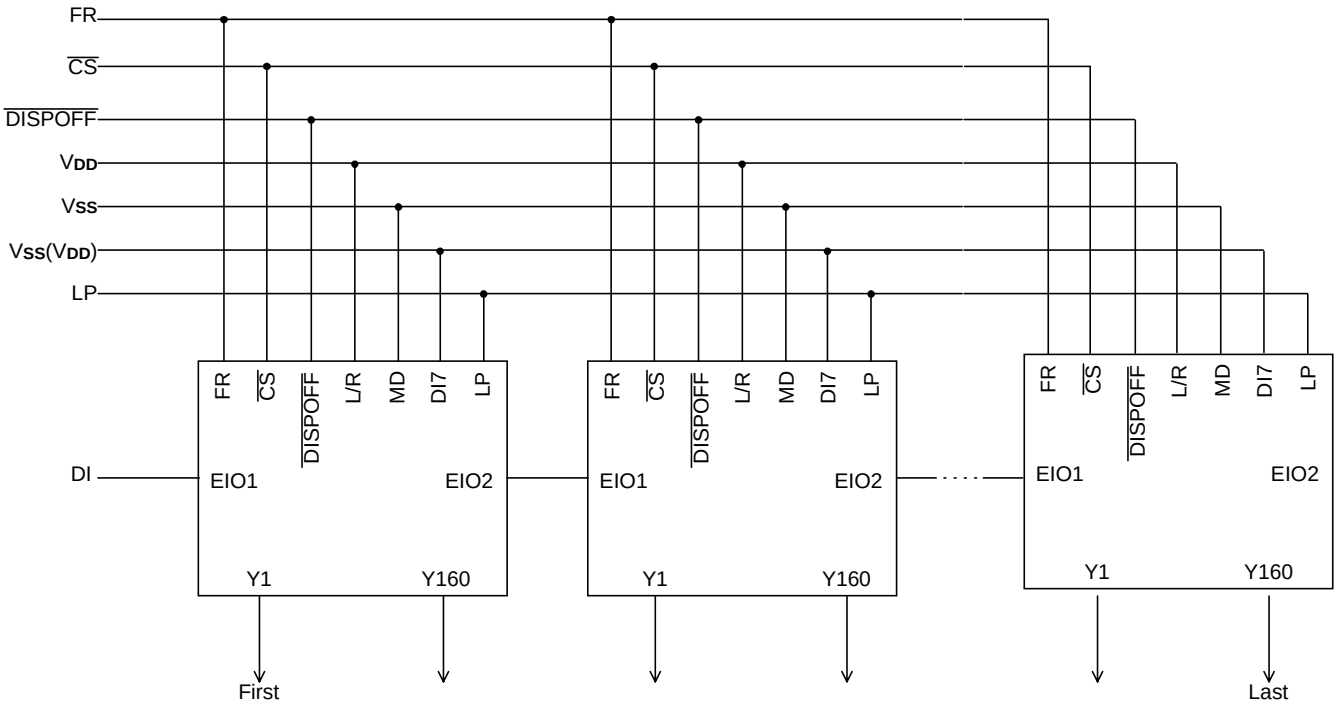


n: 4-bit parallel mode 40
8-bit parallel mode 20

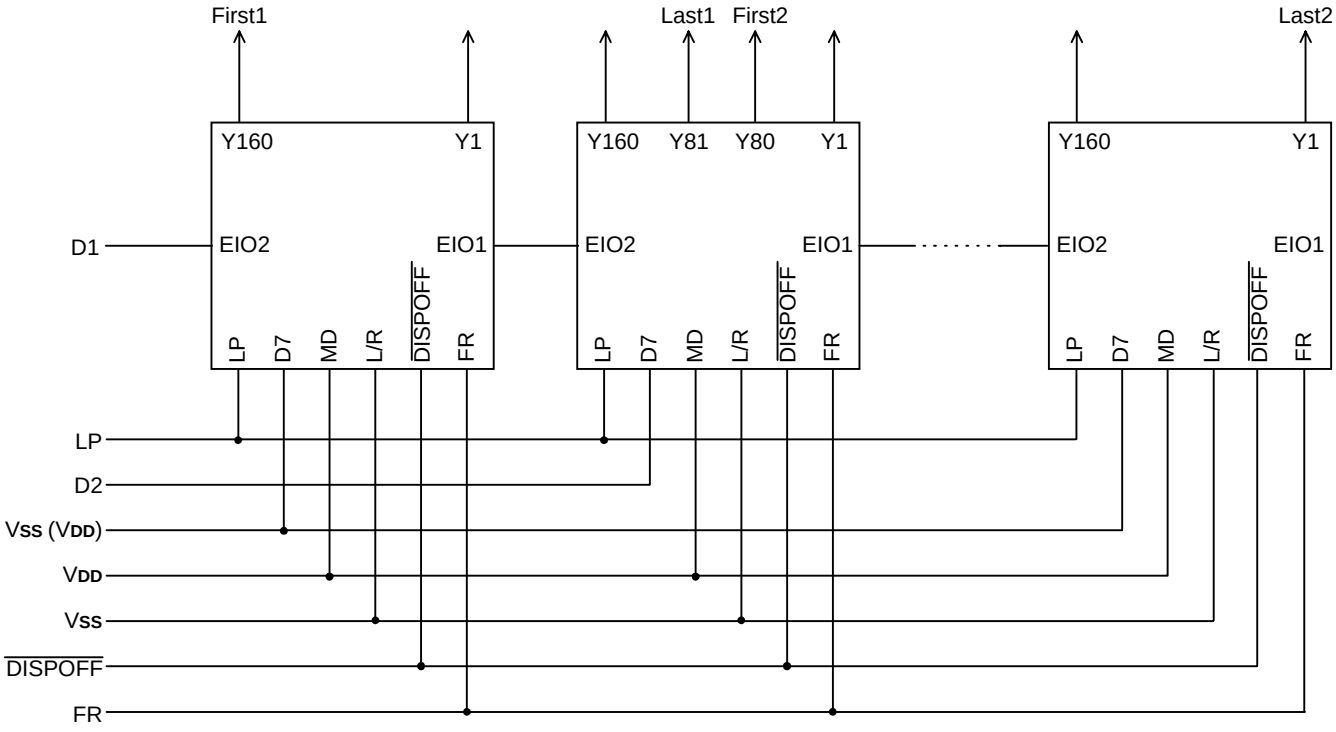
6. Connection Examples for Common Drivers



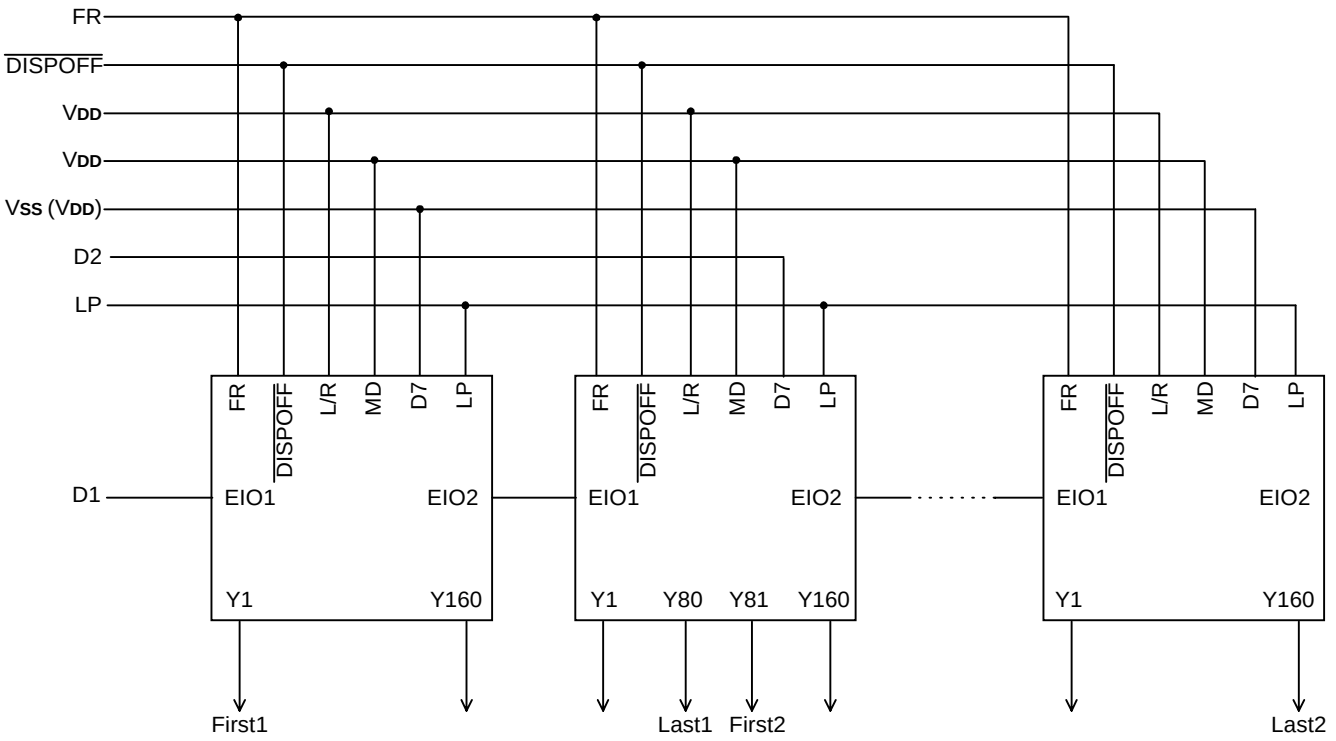
Single Mode (Shifting towards the left)



Single Mode (Sifting towards the right)



Dual mode (Shifting towards the left)



Dual mode (Shifting towards the right)

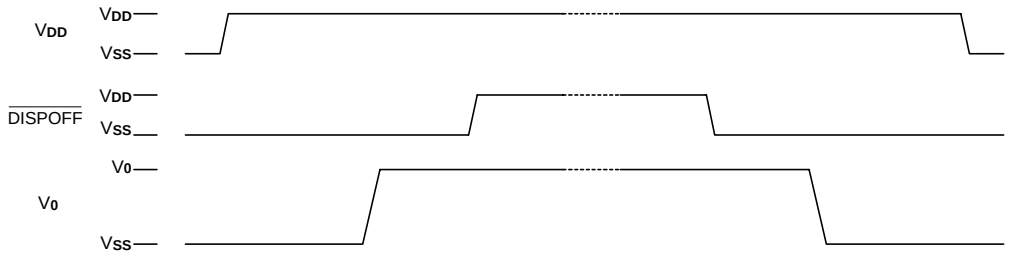
7. Precaution

Be careful when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur if voltage is supplied to the LCD driver power supply while the logic system power supply is floating.
The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100Ω) or fuse to the LCD driver power V_0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply only after resetting the logic condition of this LSI inside to the $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ will cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level V_{SS} on the $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD driver power.
When connecting the power supply, follow the recommended sequence shown.



Absolute Maximum Rating*

DC Supply Voltage V_{DD} . . . . . -0.3V to +7.0V

DC Supply Voltage V_0 . . . . . -0.3V to +30V

Input Voltage . . . . . -0.3V to V_{DD} +0.3V

Operating Ambient Temperature . . . . -30°C to +85°C

Storage Temperature . . . . . -45°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

Segment Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30 V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.5	-	5.5	V	
Operating Voltage	V_0	15	-	30	V	
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2 and $\overline{DISPOFF}$ pins
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V	
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA
Input leakage current 1	I_{IH}	-	-	+1.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2 and $\overline{DISPOFF}$ pins, V_I = V_{DD}
Input leakage current 2	I_{IL}	-	-	-1.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2 and $\overline{DISPOFF}$ pins, V_I = V_{SS}
Output resistance	R_{ON}	-	1.0	1.5	kΩ	V_0 = +30.0V; Y_1 - Y_{160} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	1.5	2.0		V_0 = +20.0V
Stand-by current	I_{SB}	-	-	5.0	μA	V_{SS} pin, Note 1
Consumed current (1) (Deselection)	I_{DD1}	-	-	2.0	mA	V_{DD} pin, Note 2
Consumed current (2) (Selection)	I_{DD2}	-	-	8.0	mA	V_{DD} pin, Note 3
Consumed current	I_0	-	-	1.0	mA	V_0 pin, Note 4

Note:

1. V_{DD} = +5.0V, V_0 = +30V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 14MHz, No-load, EI = V_{DD}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
3. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 14MHz, No-load. EI = V_{SS}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 14MHz, f_{LP} = 41.6kHz. f_{FR} = 80 Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)

Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage	V_{DD}	2.5	-	5.5	V		
Operating Voltage	V_0	15	-	30	V		
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2 and $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V		
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA	
Input leakage current 1	I_{IH}	-	-	+1.0	μA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, V_I = V_{DD}	
Input leakage current 2	I_{IL}	-	-	-1.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, V_I = V_{SS}	
Output resistance	R_{ON}	-	1.0	1.5	kΩ	V_0 = +30.0V	Y_1 - Y_{160} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	1.5	2.0		V_0 = +20.0V	
Stand-by current	I_{SB}	-	-	5	μA	V_{SS} pin, Note 1	
Consumed current (1)	I_{DD}	-	-	80	μA	V_{DD} pin, Note 2	
Consumed current (2)	I_0	-	-	160	μA	V_0 pin, Note 2	

Note:

1. V_{DD} = +5.0V, V_0 = +30V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +30V, f_{LP} = 41.6KHz, f_{FR} = 80Hz, case of 1/480 duty operation, No-load

AC Characteristics

Segment Mode 1 (V_{SS} = V_5 = 0V, V_{DD} = 4.5 - 5.5V, V_0 = 15 to 30, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	71	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hole time	t_{DH}	20	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	23	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	25	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock rise time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	21	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	40	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (T_{ck} - t_{WCKII} - t_{wckl})/2 is the maximum in the case of high speed operation.

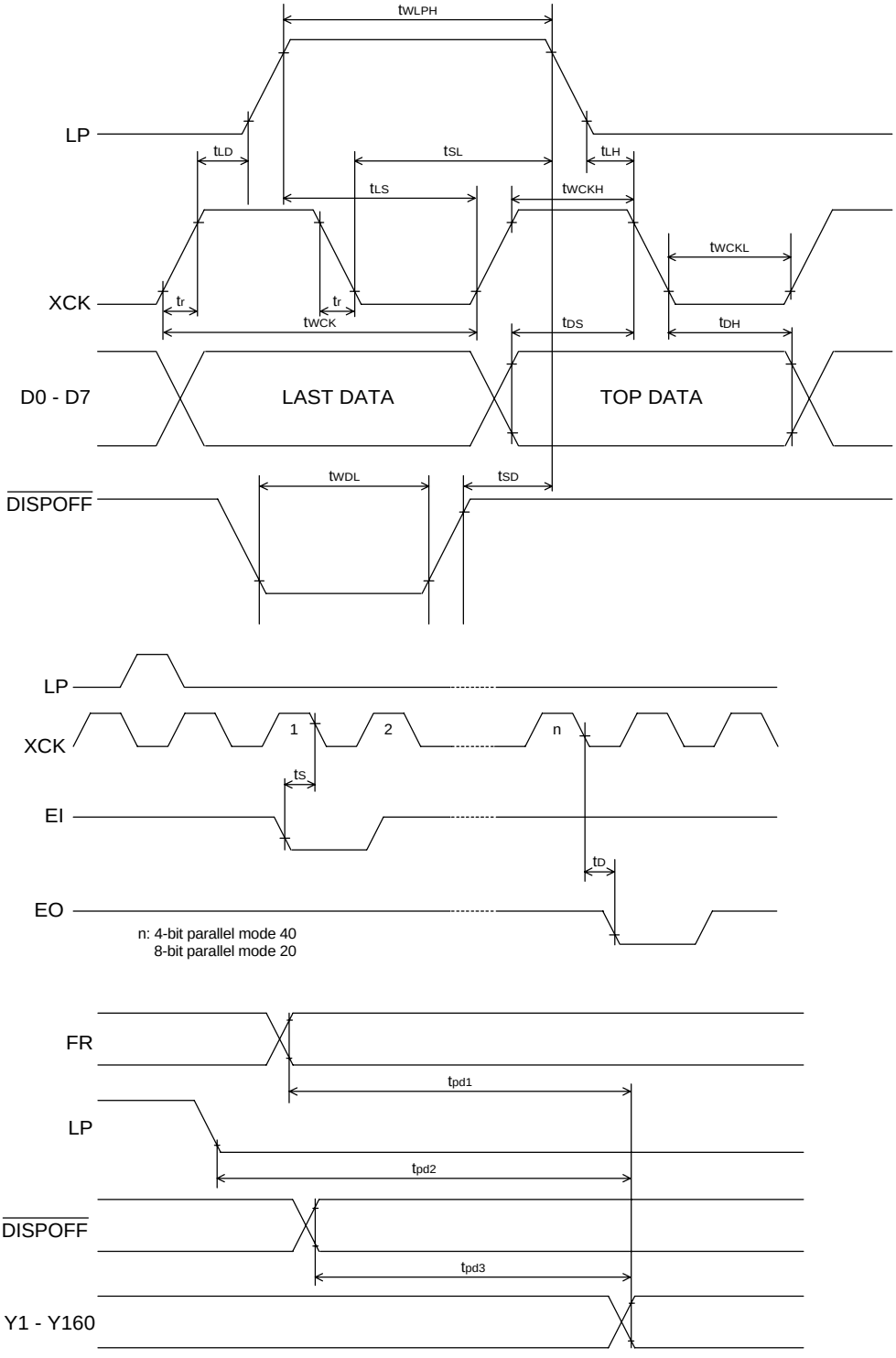
Segment Mode 2 (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 4.5V, V_0 = 15 to 30, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	125	-		ns	tr, tf ≦ 11ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	51	-		ns	
Shift clock "L" pulse width	t_{WCKL}	51	-		ns	
Data setup time	t_{DS}	30	-		ns	
Data hole time	t_{DH}	40	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	51	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	51	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	51	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	51	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	36	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	78	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (t_{CK} - t_{WCKII} - t_{WCKL})/2 is the maximum in the case of high speed operation.

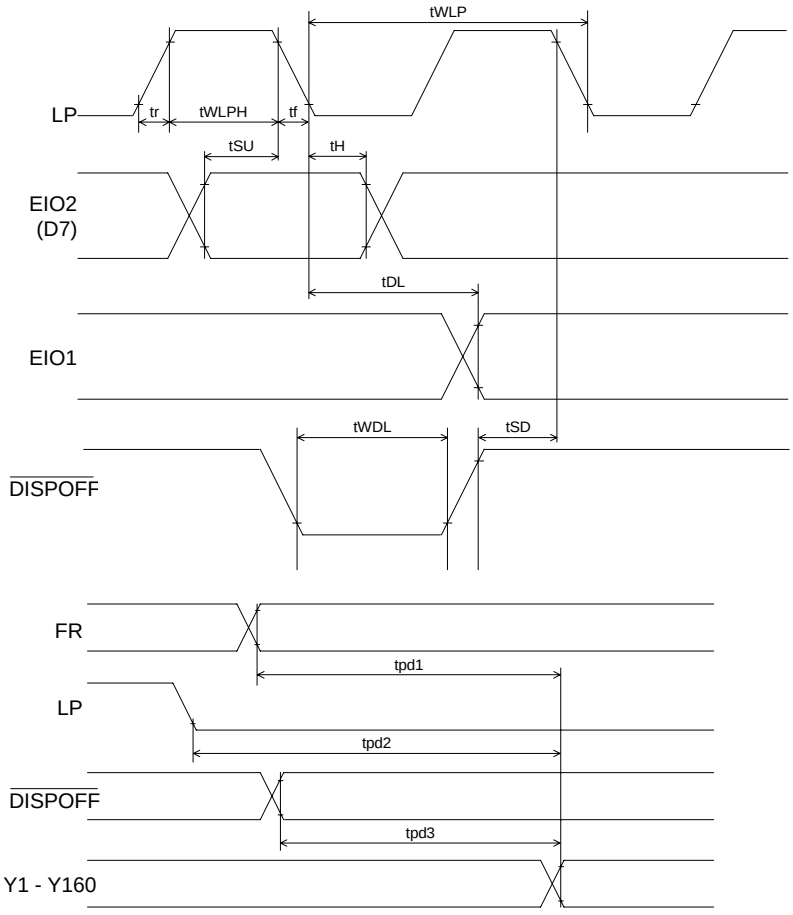
Timing waveform of the Segment Mode



Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30V and T_A = -30 to +85°C, unless otherwise noted)

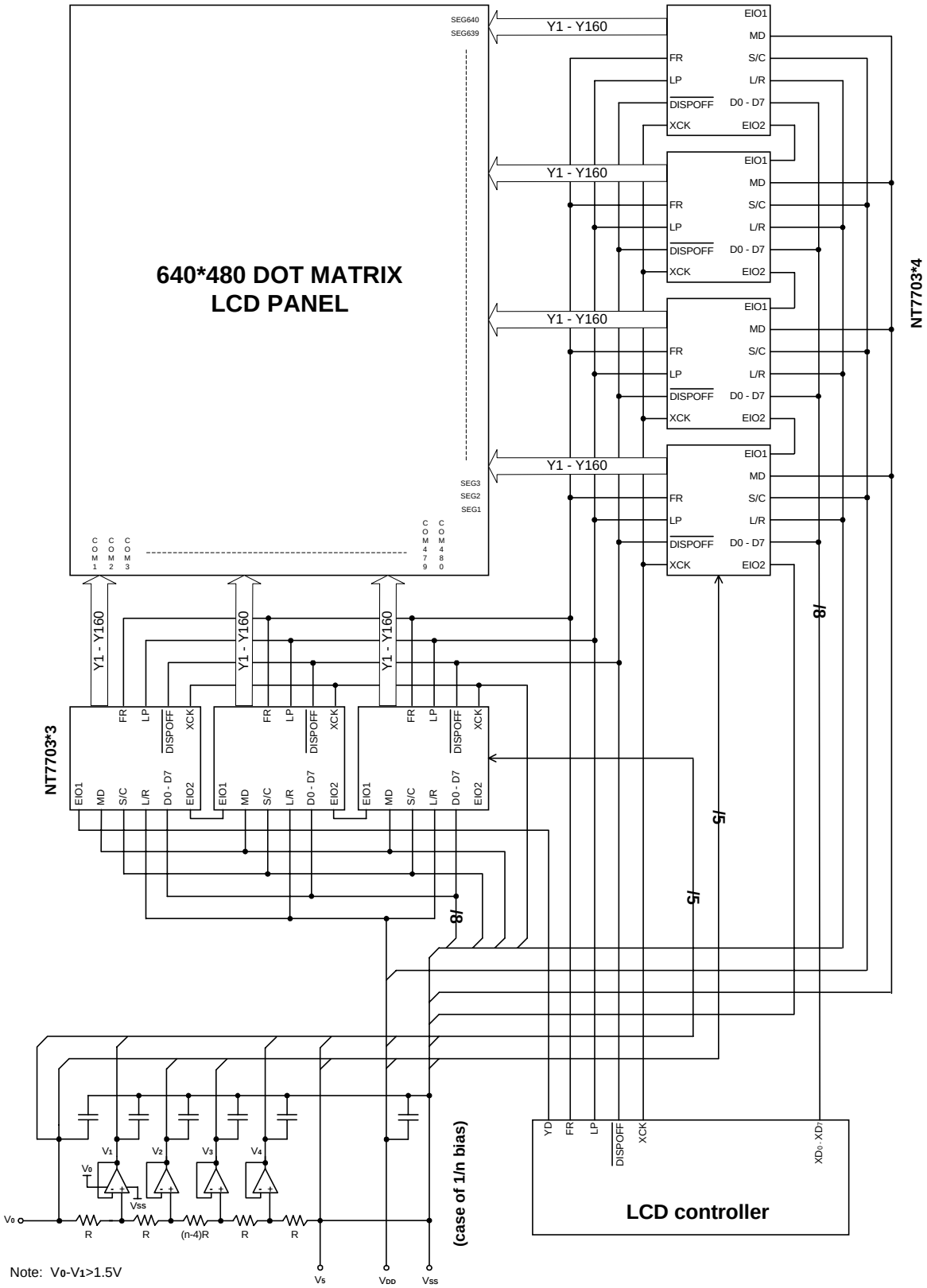
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	t_r, t_f ≦ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
$\overline{DISPOFF}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{DISPOFF}$ enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	C_L = 15pF

Timing Characteristics of Common Mode

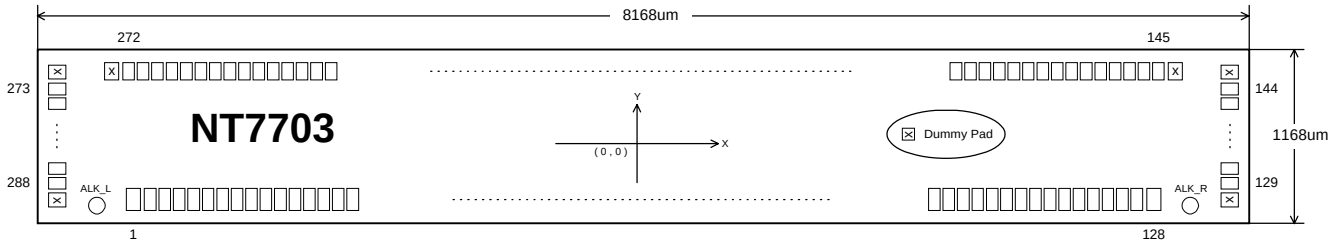


L/R = "L"

Application Circuit (for reference only)



Bonding Diagram



Pad Location

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	V_{0L}	-3820	-521	31	V_{SS}	-2010	-521
2	V_{0L}	-3750	-521	32	V_{SS}	-1950	-521
3	V_{0L}	-3690	-521	33	V_{SS}	-1890	-521
4	V_{0L}	-3630	-521	34	V_{SS}	-1830	-521
5	V_{0L}	-3570	-521	35	V_{SS}	-1770	-521
6	V_{0L}	-3510	-521	36	V_{SS}	-1710	-521
7	V_{0L}	-3450	-521	37	V_{SS}	-1650	-521
8	V_{12L}	-3390	-521	38	V_{SS}	-1590	-521
9	V_{12L}	-3330	-521	39	V_{SS}	-1530	-521
10	V_{12L}	-3270	-521	40	L/R	-1470	-521
11	V_{12L}	-3210	-521	41	L/R	-1410	-521
12	V_{12L}	-3150	-521	42	V_{DD}	-1350	-521
13	V_{43L}	-3090	-521	43	V_{DD}	-1290	-521
14	V_{43L}	-3030	-521	44	V_{DD}	-1230	-521
15	V_{43L}	-2970	-521	45	V_{DD}	-1170	-521
16	V_{43L}	-2910	-521	46	V_{DD}	-1110	-521
17	V_{43L}	-2850	-521	47	V_{DD}	-1050	-521
18	V_{5L}	-2790	-521	48	V_{DD}	-990	-521
19	V_{5L}	-2730	-521	49	V_{DD}	-930	-521
20	V_{5L}	-2670	-521	50	V_{DD}	-870	-521
21	V_{5L}	-2610	-521	51	V_{DD}	-810	-521
22	V_{5L}	-2550	-521	52	V_{DD}	-750	-521
23	V_{SS}	-2490	-521	53	V_{DD}	-690	-521
24	V_{SS}	-2430	-521	54	V_{DD}	-630	-521
25	V_{SS}	-2370	-521	55	V_{DD}	-570	-521
26	V_{SS}	-2310	-521	56	V_{DD}	-510	-521
27	V_{SS}	-2250	-521	57	V_{DD}	-450	-521
28	V_{SS}	-2190	-521	58	S/C	-390	-521
29	V_{SS}	-2130	-521	59	S/C	-330	-521
30	V_{SS}	-2070	-521	60	EIO_2	-270	-521

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	EIO_2	-210	-521	101	V_{SS}	2190	-521
62	D0	-150	-521	102	V_{SS}	2250	-521
63	D0	-90	-521	103	V_{SS}	2310	-521
64	D1	-30	-521	104	V_{SS}	2370	-521
65	D1	30	-521	105	V_{SS}	2430	-521
66	D2	90	-521	106	V_{SS}	2490	-521
67	D2	150	-521	107	V_{5R}	2550	-521
68	D3	210	-521	108	V_{5R}	2610	-521
69	D3	270	-521	109	V_{5R}	2670	-521
70	D4	330	-521	110	V_{5R}	2730	-521
71	D4	390	-521	111	V_{5R}	2790	-521
72	D5	450	-521	112	V_{43R}	2850	-521
73	D5	510	-521	113	V_{43R}	2910	-521
74	D6	570	-521	114	V_{43R}	2970	-521
75	D6	630	-521	115	V_{43R}	3030	-521
76	D7	690	-521	116	V_{43R}	3090	-521
77	D7	750	-521	117	V_{12R}	3150	-521
78	XCK	810	-521	118	V_{12R}	3210	-521
79	XCK	870	-521	119	V_{12R}	3270	-521
80	$\overline{DISPOFF}$	930	-521	120	V_{12R}	3330	-521
81	$\overline{DISPOFF}$	990	-521	121	V_{12R}	3390	-521
82	LP	1050	-521	122	V_{0R}	3450	-521
83	LP	1110	-521	123	V_{0R}	3510	-521
84	EIO_1	1170	-521	124	V_{0R}	3570	-521
85	EIO_1	1230	-521	125	V_{0R}	3630	-521
86	FR	1290	-521	126	V_{0R}	3690	-521
87	FR	1350	-521	127	V_{0R}	3750	-521
88	MD	1410	-521	128	V_{0R}	3820	-521
89	MD	1470	-521	129	Y1	4030	-450
90	Vss	1530	-521	130	Y2	4030	-390
91	Vss	1590	-521	131	Y3	4030	-330
92	Vss	1650	-521	132	Y4	4030	-270
93	Vss	1710	-521	133	Y5	4030	-210
94	Vss	1770	-521	134	Y6	4030	-150
95	Vss	1830	-521	135	Y7	4030	-90
96	Vss	1890	-521	136	Y8	4030	-30
97	Vss	1950	-521	137	Y9	4030	30
98	Vss	2010	-521	139	Y10	4030	90
99	Vss	2070	-521	139	Y11	4030	150
100	Vss	2130	-521	140	Y12	4030	210

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	Y13	4030	270	181	Y53	1650	529
142	Y14	4030	330	182	Y54	1590	529
143	Y15	4030	390	183	Y55	1530	529
144	Y16	4030	450	184	Y56	1470	529
145	Y17	3810	529	185	Y57	1410	529
146	Y18	3750	529	186	Y58	1350	529
147	Y19	3690	529	187	Y59	1290	529
148	Y20	3630	529	188	Y60	1230	529
149	Y21	3570	529	189	Y61	1170	529
150	Y22	3510	529	190	Y62	1110	529
151	Y23	3450	529	191	Y63	1050	529
152	Y24	3390	529	192	Y64	990	529
153	Y25	3330	529	193	Y65	930	529
154	Y26	3270	529	194	Y66	870	529
155	Y27	3210	529	195	Y67	810	529
156	Y28	3150	529	196	Y68	750	529
157	Y29	3090	529	197	Y69	690	529
158	Y30	3030	529	198	Y70	630	529
159	Y31	2970	529	199	Y71	570	529
160	Y32	2910	529	200	Y72	510	529
161	Y33	2850	529	201	Y73	450	529
162	Y34	2790	529	202	Y74	390	529
163	Y35	2730	529	203	Y75	330	529
164	Y36	2670	529	204	Y76	270	529
165	Y37	2610	529	205	Y77	210	529
166	Y38	2550	529	206	Y78	150	529
167	Y39	2490	529	207	Y79	90	529
168	Y40	2430	529	208	Y80	30	529
169	Y41	2370	529	209	Y81	-30	529
170	Y42	2310	529	210	Y82	-90	529
171	Y43	2250	529	211	Y83	-150	529
172	Y44	2190	529	212	Y84	-210	529
173	Y45	2130	529	213	Y85	-270	529
174	Y46	2070	529	214	Y86	-330	529
175	Y47	2010	529	215	Y87	-390	529
176	Y48	1950	529	216	Y88	-450	529
177	Y49	1890	529	217	Y89	-510	529
178	Y50	1830	529	218	Y90	-570	529
179	Y51	1770	529	219	Y91	-630	529
180	Y52	1710	529	220	Y92	-690	529

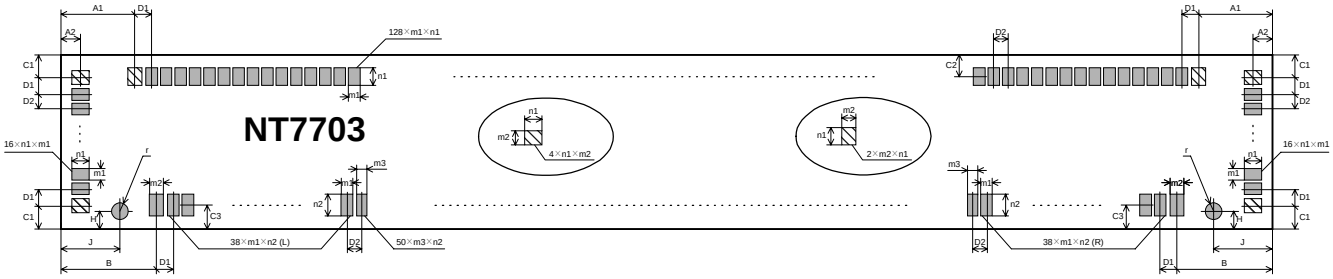
Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
221	Y93	-750	529	256	Y128	-2850	529
222	Y94	-810	529	257	Y129	-2910	529
223	Y95	-870	529	258	Y130	-2970	529
224	Y96	-930	529	259	Y131	-3030	529
225	Y97	-990	529	260	Y132	-3090	529
226	Y98	-1050	529	261	Y133	-3150	529
227	Y99	-1110	529	262	Y134	-3210	529
228	Y100	-1170	529	263	Y135	-3270	529
229	Y101	-1230	529	264	Y136	-3330	529
230	Y102	-1290	529	265	Y137	-3390	529
231	Y103	-1350	529	266	Y138	-3450	529
232	Y104	-1410	529	267	Y139	-3510	529
233	Y105	-1470	529	268	Y140	-3570	529
234	Y106	-1530	529	269	Y141	-3630	529
235	Y107	-1590	529	270	Y142	-3690	529
236	Y108	-1650	529	271	Y143	-3750	529
237	Y109	-1710	529	272	Y144	-3810	529
238	Y110	-1770	529	273	Y145	-4030	450
239	Y111	-1830	529	274	Y146	-4030	390
240	Y112	-1890	529	275	Y147	-4030	330
241	Y113	-1950	529	276	Y148	-4030	270
242	Y114	-2010	529	277	Y149	-4030	210
243	Y115	-2070	529	278	Y150	-4030	150
244	Y116	-2130	529	279	Y151	-4030	90
245	Y117	-2190	529	280	Y152	-4030	30
246	Y118	-2250	529	281	Y153	-4030	-30
247	Y119	-2310	529	282	Y154	-4030	-90
248	Y120	-2370	529	283	Y155	-4030	-150
249	Y121	-2430	529	284	Y156	-4030	-210
250	Y122	-2490	529	285	Y157	-4030	-270
251	Y123	-2550	529	286	Y158	-4030	-330
252	Y124	-2610	529	287	Y159	-4030	-390
253	Y125	-2670	529	288	Y160	-4030	-450
254	Y126	-2730	529		ALK_L	-3921	-534
255	Y127	-2790	529		ALK_R	3921	-534

Dummy Pad Location (Total: 6 pin)

NO.	X	Y	NO.	X	Y
1	4030	-520	4	-3880	529
2	4030	520	5	-4030	520
3	3880	529	6	-4030	-520

Package Information

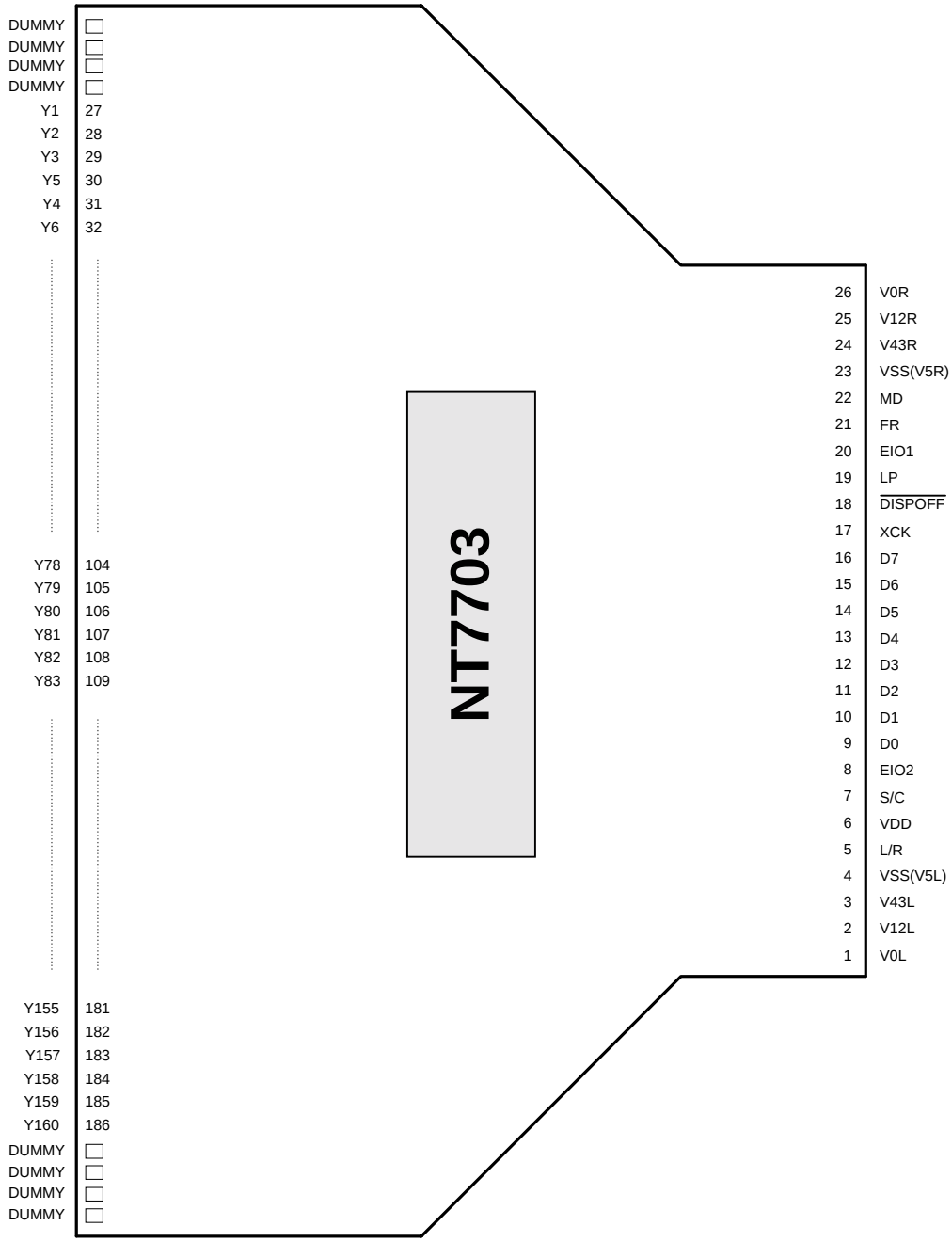


Chip Outline Dimensions

unit: um

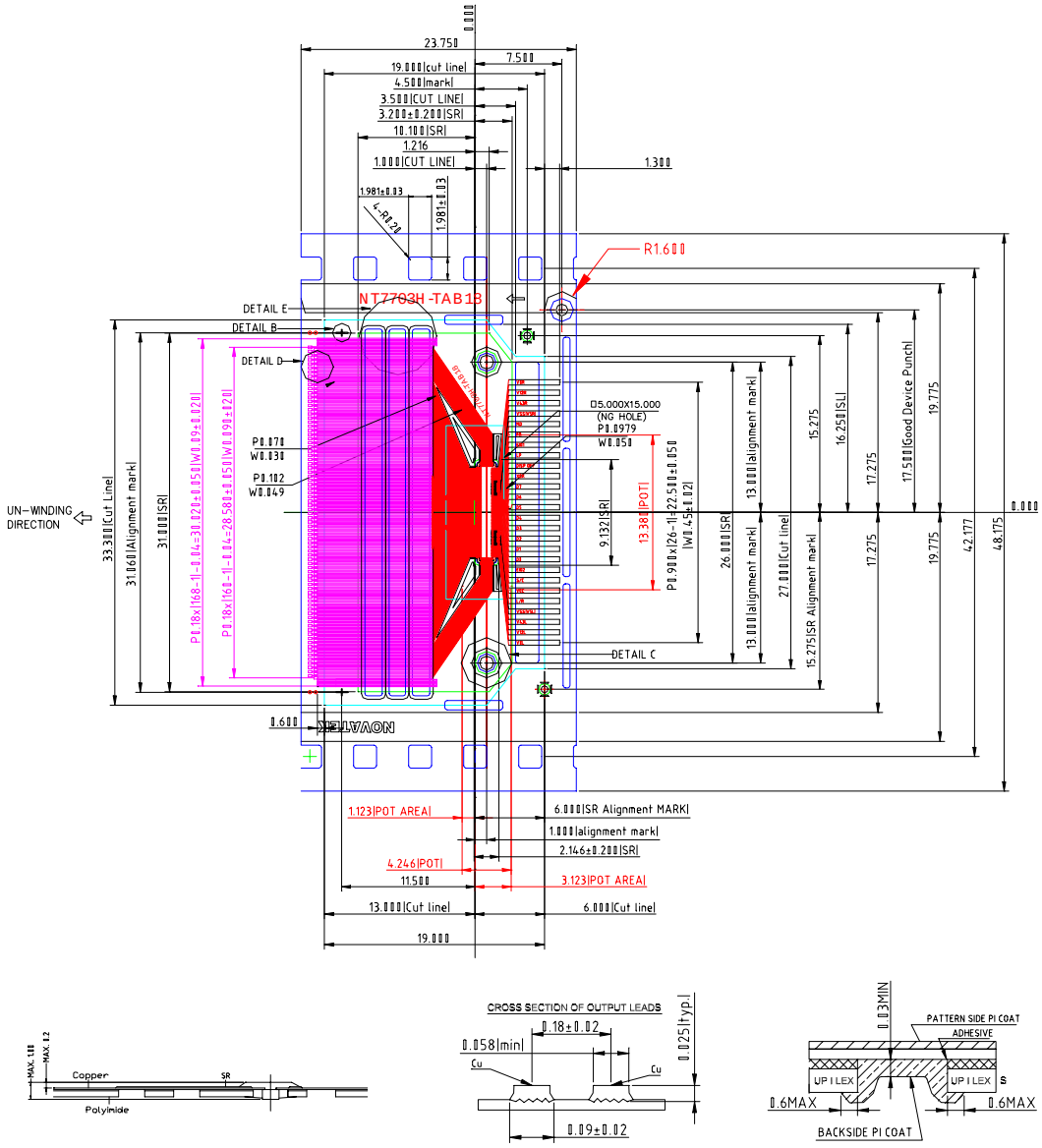
Symbol	Dimensions in um	Symbol	Dimensions in um
A1	204	H	50
A2	54	J	163
B	264	m1	39
C1	64	m2	55
C2	55	m3	38
C3	63	n1	72
D1	70	n2	90
D2	60	r	35

TCP Pin Layout



(COPPER SIDE VIEW)

External View of TCP Pins

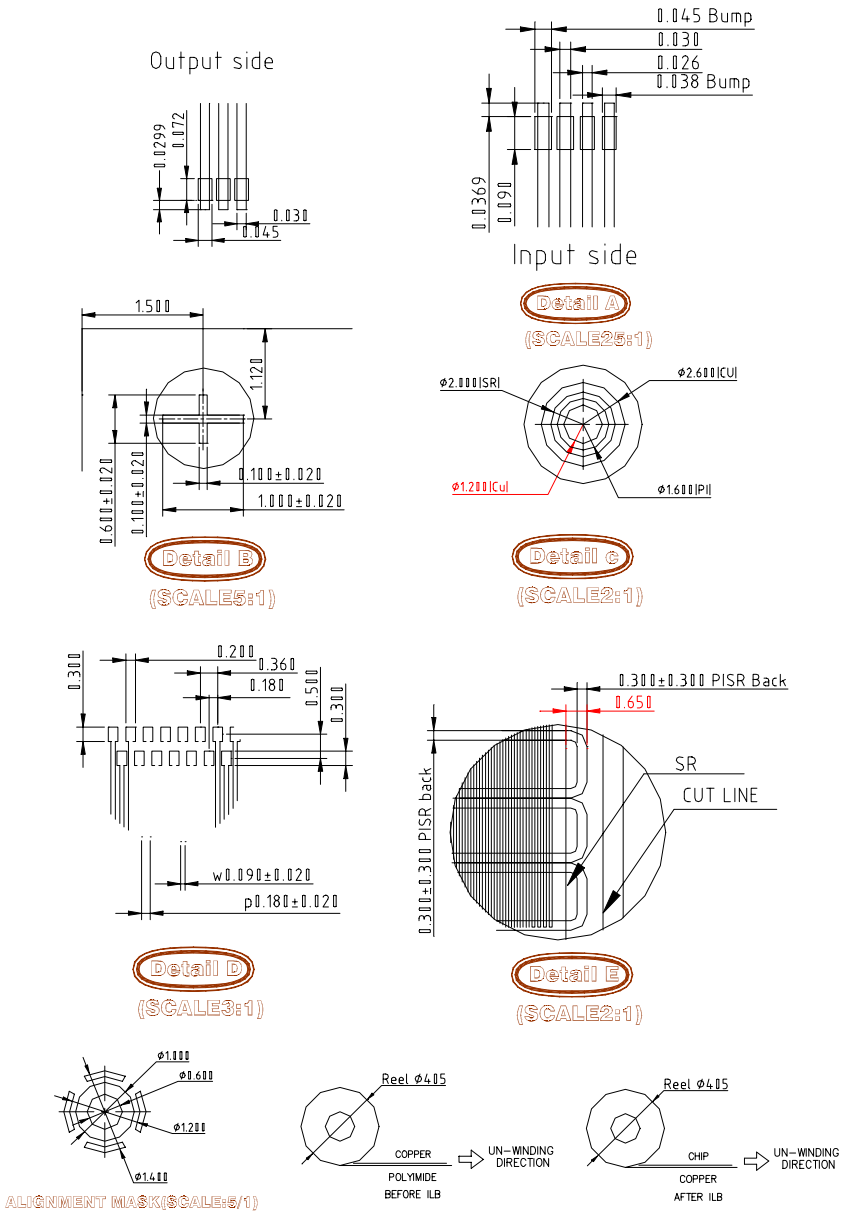


Specification

1 .GENERAL TOLERANCE ±0.050mm
2 .ALL CHAMFER IS R±0.200mm
3 .MATERIAL

Polyimide	UPILEX-S:	75±6um
Adhesive	TORAY #7100	12±3um
Copper	FQ-VLP	25±5um
Plating	Sn:	0.20±0.05um
Solder Resist	AE-70-M11	26±14um
	OTHER TOLERANCE:±0.200mm	
Flex Coating	FS-100L	MIN10
Space Tape Material	Polyester (PET)	
Leader Tape Material	Polyester (PET)	
PKG Reel Size	405 mm	

4 .5 SPROCKET HOLES (23.75MM) FOR 1 TAPES



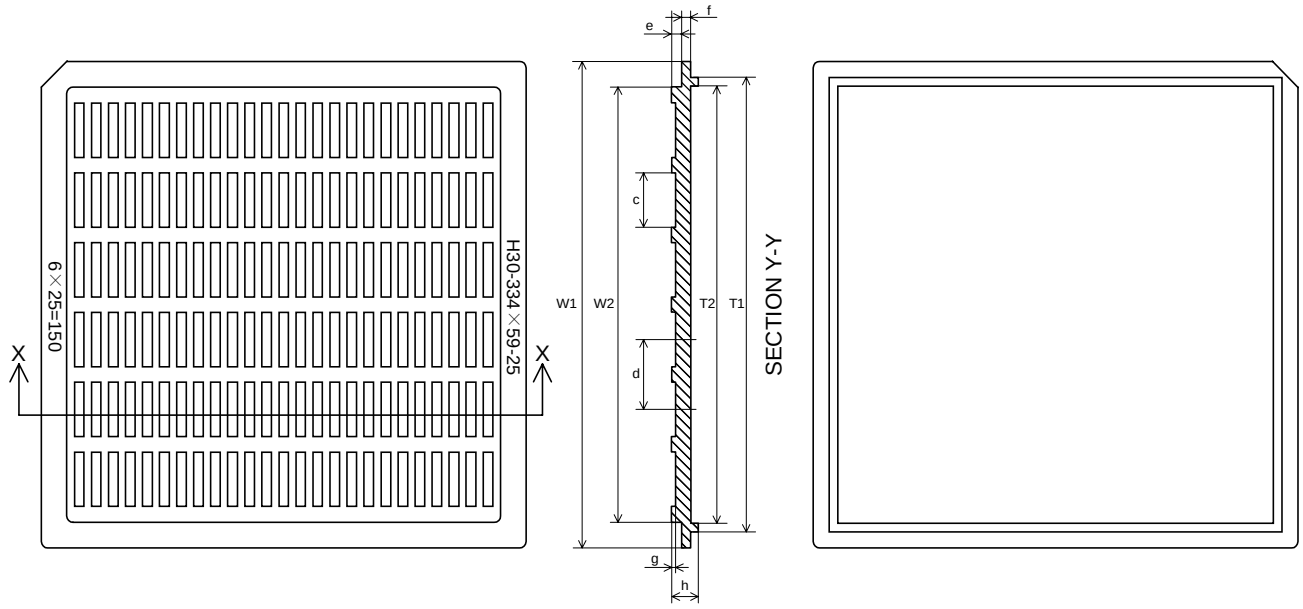
Cautions concerning storage:

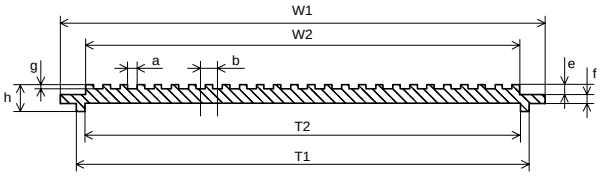
1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broke, store the products in a nitrogen atmosphere.
2. Storage conditions :

Storage state	Storage conditions
unopened **(less than 90 days)**	Temperature: 5 to 30℃; humidity: 80%RH or less
After seal of broken **(less than 30 days)**	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

Tray Information





SECTION X-X

Tray Outline Dimensions

unit: mm

Symbol	Dimensions in mm	Symbol	Dimensions in mm
a	1.50	g	0.64
b	2.67	h	4.20
c	8.50	W1	76.0
d	10.90	W2	68.0
e	1.60	T1	71.0
f	1.40	T2	68.3

Ordering Information

Part No.	Package
NT7703H-BDT	Au bump on chip tray
NT7703H-TAB18	TCP Form

Product Spec. Change Notice

NT7703 Specification Revision History		
Version	**Content**	**Date**
1.0	TCP and tray information addition (Page 33 - 36)	Dec. 2001
0.2	Gold Bump Size revision (Page 31) m1: 45 → 39, m2: 58 → 55	Sep. 2001
0.1	Pad Location Addition	Nov. 2000
0.0	Original	Nov. 2000