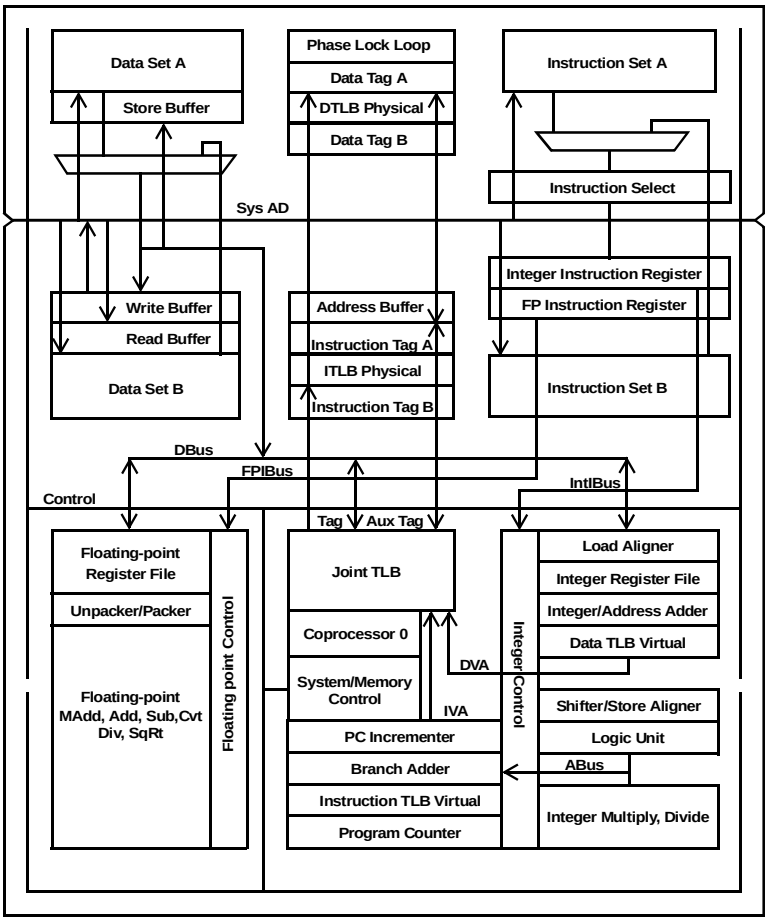
ACT5230
32-Bit Superscaler Microprocessor

Features

- **Full militarized QED RM5230 microprocessor**
- **Dual Issue superscalar microprocessor - can issue one integer and one floating-point instruction per cycle**
  - **100, 133 and 150 MHz operating frequency – Consult Factory for latest speeds**
  - **228 Dhrystone2.1 MIPS**
  - **SPECInt95 4.2 SPECfp95 4.5**
- **System interface optomized for embedded applications**
  - **32-bit system interface lowers total system cost with up to 87.5 MHz operating frequency**
  - **High performance write protocols maximize uncached write bandwidth**
  - **Operates at processor clock divisors 2 through 8**
  - **5V tolerant I/O's**
  - **IEEE 1149.1 JTAG boundary scan**
- **Integrated on-chip caches**
  - **16KB instruction - 2 way set associative**
  - **16KB data - 2 way set associative**
  - **Virtually indexed, physically tagged**
  - **Write-back and write-through on per page basis**
  - **Early restart on data cache misses**
- **Integrated memory management unit**
  - **Fully associative joint TLB (shared by I and D translations)**
  - **48 dual entries map 96 pages**
  - **Variable page size (4KB to 16MB in 4x increments)**
- **High-performance floating point unit**
  - **Single cycle repeat rate for common single precision operations and some double precision operations**
  - **Two cycle repeat rate for double precision multiply and double precision combined multiply-add operations**
  - **Single cycle repeat rate for single precision combined multiply-add operation**
- **MIPS IV instruction set**
  - **Floating point multiply-add instruction increases performance in signal processing and graphics applications**
  - **Conditional moves to reduce branch frequency**
  - **Index address modes (register + register)**
- **Embedded application enhancements**
  - **Specialized DSP integer Multiply-Accumulate instruction and 3 operand multiply instruction**
  - **I and D cache locking by set**
  - **Optional dedicated exception vector for interrupts**
- **Fully static CMOS design with power down logic**
  - **Standby reduced power mode with WAIT instruction**
  - **2.5 Watts typical with less than 70 mA standby current**
- **128-pin Power Quad-4 package (F22), Consult Factory for package configuration**

Block Diagram



Preliminary

DESCRIPTION

The ACT5230 is a highly integrated superscalar microprocessor that implements a superset of the MIPS IV Instruction Set Architecture(ISA). It has a high performance 64-bit integer unit, a high throughput, fully pipelined 64-bit floating point unit, an operating system friendly memory management unit with a 48-entry fully associative TLB, a 16 KByte 2-way set associative instruction cache, a 16 KByte 2-way set associative data cache, and a high-performance 32-bit system interface. The ACT5230 can issue both an integer and a floating point instruction in the same cycle.

The ACT5230 is ideally suited for high-end embedded control applications such as internetworking, high performance image manipulation, high speed printing, and 3-D visualization.

HARDWARE OVERVIEW

The ACT5230 offers a high-level of integration targeted at high-performance embedded applications. Some of the key elements of the ACT5230 are briefly described below.

Superscalar Dispatch

The ACT5230 has an efficient asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating-point computation instruction simultaneously. With respect to superscalar issue, integer instructions include alu, branch, load/store, and floating-point load/store, while floating-point computation instructions include floating-point add, subtract, combined multiply-add, converts, etc. In combination with its high throughput fully pipelined floating-point execution unit, the superscalar capability of the ACT5230 provides unparalleled price/performance in computationally intensive embedded applications.

CPU Registers

Like all MIPS ISA processors, the ACT5230 CPU has a simple, clean user visible state consisting of 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits.

Pipeline

For integer operations, loads, stores, and other non-floating-point operations, the ACT5230 uses the simple 5-stage pipeline also found in the QED circuits R4600, R4700, and R5000. In addition to this standard pipeline, the ACT5230 uses an extended seven stage pipeline for floating-point operations. Like the QED R5000, the ACT5230 does virtual to physical translation in parallel with cache access.

Integer Unit

Like the QED R5000, the ACT5230 implements the MIPS IV Instruction Set Architecture, and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I-III instruction sets. Additionally, the ACT5230 includes two implementation specific instructions not found in the baseline MIPS IV ISA but that are useful in the embedded market place. Described in detail in the QED RM5230 datasheet,, these instructions are integer multiply-accumulate and 3-operand integer multiply.

The ACT5230 integer unit includes thirty-two general purpose 64-bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/divide unit. Additional register resources include: the HI/LO result registers for the two-operand integer multiply/ divide operations, and the program counter(PC).

Register File

The ACT5230 has thirty-two general purpose registers with register location 0 hard wired to zero. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

ALU

The ACT5230 ALU consists of the integer adder/ subtractor, the logic unit, and the shifter. The adder performs address calculations in addition to arithmetic operations, the logic unit performs all logical and zero shift data moves, and the shifter performs shifts and store alignment operations. Each of these units is optimized to perform all operations in a single processor cycle

For Detail Information regarding the operation of the Quantum Effect Design (QED) RISCMark™ RM5230™, 32-Bit Superscalar Microprocessor see the QED datasheet (Revision 1.2 July 1998).

Absolute Maximum Ratings[1]

Symbol	Rating	Range	Units
T_{TERM}	Terminal Voltage with respect to GND	-0.5[2] to 4.6	V
T_{CASE}	Operating Temperature	0 to +85	°C
T_{BIAS}	Case Temperature under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{IN}	DC Input Current	20[3]	mA
I_{OUT}	DC Output Current	50	mA

Notes:
1. Stresses above those listed under "AbsoluteMaximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VIN minimum = -2.0V for pulse width less than 15nS. VIN maximum should not exceed +5.5 Volts.
3. When VIN < 0V or VIN > Vcc.
4. No more than one output should be shorted at one time. Duration of the short should not exceed more than 30 second.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+3.135	+3.465	V
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	$0.2V_{CC}$	V
T_C	Operating Temperature Case (Commercial)	0	+85	°C

DC Characteristics

(VCC = 3.3V ±5%; TCASE = 0°C to +85°C)

Parameter	Sym	Conditions	133 / 150MHz		Units
			Min	Max	
Output Low Voltage	V_{OL1}	I_{OL} = 20 µA		0.1	V
Output High Voltage	V_{OH1}	I_{OL} = 20 µA	Vcc - 0.1		V
Output Low Voltage	V_{OL2}	I_{OL} = 4 mA		0.4	V
Output High Voltage	V_{OH2}	I_{OL} = 4 mA	2.4		V
Input High Voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}		-0.5	$0.2V_{CC}$	V
Input Current	I_{IN1}	V_{IN} = 0V	-20	+20	µA
Input Current	I_{IN2}	V_{IN} = V_{CC}	-20	+20	µA
Input Current	I_{IN3}	V_{IN} = 5.5V	-250	+250	µA
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF

Power Consumption

Parameter	Symbol	Conditions	133MHz, 3.3V		150MHz, 3.3V		Units
			Typ[5]	Max	Typ[5]	Max	
Active Operating Supply Current	I_{CC1}	C_L = 0pF, 150/75MHz, No SysAD activity	TBD	TBD	TBD	TBD	mA
	I_{CC2}	C_L = 50pF, 150/75MHz, R4000 write protocol without FPU operation	1000	1750	1150	1950	mA
	I_{CC3}	C_L = 50pF, 150/75MHz, write re-issue or pipelined writes	1100	2000	1250	2250	mA
Standby Current	I_{SB1}	C_L = 0pF, 150/75MHz		TBD		TBD	mA
	I_{SB1}	C_L = 50pF, 150/75MHz		TBD		TBD	mA

Notes:
5. Typical integer instruction mix and cache miss rates.

AC Characteristics
(V_{CC} = 3.3V ±5%; T_{CASE} = 0°C to +85°C)

Capacitive Load Deration

Symbol	Parameter	133 / 150MHz		Units
		Minimum	Maximum	
C_{LD}	Load Derate		2	ns/25pF

Clock Parameters

Parameter	Symbol	Test Conditions	133/150MHz		Units
			Min	Max	
SysClock High	t_{SCHigh}	Transition ≤ 5ns	4		ns
SysClock Low	t_{SCLow}	Transition ≤ 5ns	4		ns
SysClock Frequency[6]			33	75	MHz
SysClock Period	t_{SCP}			30	ns
Clock Jitter for SysClock	$t_{JitterIn}$			±250	ps
SysClock Rise Time	t_{SCRise}			5	ns
SysClock Fall Time	t_{SCFall}			5	ns
ModeClock Period	$t_{ModeCKP}$			$256*t_{SCP}$	ns
JTA Clock Period	$t_{JTAGCKP}$			$4*t_{SCP}$	ns

Notes:
6. Operation of the ACT5230 is only guaranteed with the Phase Loop enabled.

System Interface Parameters[7]

Parameter	Symbol	Test Conditions	133MHz		150MHz		Units
			Min	Max	**Min**	Max	
Data Output[8]	t_{DO}	$mode_{14...13}$ = 10 (fastest)	TBD	TBD	TBD	TBD	ns
		$mode_{14...13}$ = 11	TBD	TBD	TBD	TBD	ns
		$mode_{14...13}$ = 00	1.0	8.0	1.0	8.0	ns
		$mode_{14...13}$ = 01 (slowest)	TBD	TBD	TBD	TBD	ns
Data Setup	t_{DS}	t_{RISE} = 5ns	4.0		4.0		ns
Data Hold	t_{DH}	t_{FALL}= 5ns	0		0		ns

Notes:
7. Timmings are are measured from from 1.5V of the clock to 1.5V of the signal.
8. Capacitive load for all output timing is 50pF.

Boot Time Interface Parameters

Parameter	Symbol	Test Conditions	133/150MHz		Units
			Min	Max	
Mode Data Setup	t_{DS}		4		SysClock cycles
Mode Data Hold	t_{DH}		0		SysClock cycles

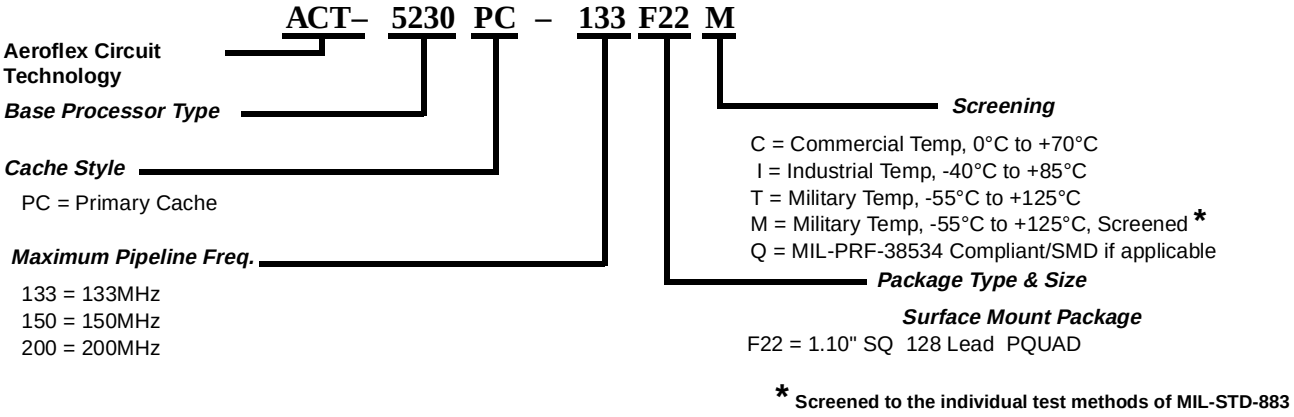
ACT5230 Microprocessor – PQUAD Pinouts

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	Vcc	53	NC	105	Vcc	157	NC
2	NC	54	NC	106	NMI*	158	NC
3	NC	55	NC	107	ExtRqst*	159	NC
4	Vcc	56	Vcc	108	Reset*	160	NC
5	Vss	57	Vss	109	ColdReset*	161	Vcc
6	SysAD4	58	ModeIn	110	VccOK	162	Vss
7	NC	59	RdRdy*	111	BigEndian	163	SysAD28
8	SysAD5	60	WrRdy*	112	Vcc	164	NC
9	NC	61	ValidIn*	113	Vss	165	SysAD29
10	Vcc	62	ValidOut*	114	SysAD16	166	NC
11	Vss	63	Release*	115	NC	167	Vcc
12	SysAD6	64	VccP	116	Vcc	168	
13	NC	65	VssP	117	Vss	169	
14	Vcc	66	SysClock	118	SysAD17	17[illegible]	NC
15	Vss	67	Vcc	119	NC	[illegible]	Vcc
16	SysAD7	68	Vss	120	SysAD1[illegible]	[illegible]	Vss
17	NC	69	Vcc	121	N[illegible]	173	SysAD31
18	SysAD8	70	Vss	122	[illegible]	174	NC
19	NC	71	Vcc	12[illegible]	[illegible]ss	175	SysADC2
20	Vcc	72	Vss	[illegible]	SysAD19	176	SysADC6
21	Vss	73	SysCmd[illegible]	[illegible]	NC	177	Vcc
22	SysAD9	74	SysC[illegible]	126	Vcc	178	Vss
23	NC	75	[illegible]	127	Vss	179	SysADC3
24	Vcc	76	[illegible]md3	128	SysAD20	180	SysADC7
25	Vss	[illegible]	Vcc	129	NC	181	Vcc
26	SysAD10	[illegible]	Vss	130	SysAD21	182	Vss
27	NC	79	SysCmd4	131	NC	183	SysADC0
28	S[illegible]	80	SysCmd5	132	Vcc	184	SysADC4
29	[illegible]	81	Vcc	133	Vss	185	Vcc
30	Vcc	82	Vss	134	SysAD22	186	Vss
31	Vss	83	SysCmd6	135	NC	187	SysADC1
32	SysAD12	84	SysCmd7	136	Vcc	188	SysADC5
33	NC	85	SysCmd8	137	Vss	189	SysAD0
34	Vcc	86	SysCmdP	138	SysAD23	190	NC
35	Vss	87	Vcc	139	NC	191	Vcc
36	SysAD13	88	Vss	140	SysAD24	192	Vss
37	NC	89	Vcc	141	NC	193	SysAD1
38	SysAD14	90	Vss	142	Vcc	194	NC
39	NC	91	Vcc	143	Vss	195	Vcc
40	Vcc	92	Vss	144	SysAD25	196	Vss
41	Vss	93	Int0*	145	NC	197	SysAD2
42	SysAD15	94	Int1*	146	Vcc	198	NC
43	NC	95	Int2*	147	Vss	199	SysAD3
44	Vcc	96	Int3*	148	SysAD26	200	NC
45	Vss	97	Int4*	149	NC	201	Vcc
46	ModeClock	98	Int5*	150	SysAD27	202	Vss
47	JTDO	99	Vcc	151	NC	203	NC
48	JTDI	100	Vss	152	Vcc	204	NC
49	JTCK	101	NC	153	Vss	205	NC
50	JTMS	102	NC	154	NC	206	NC
51	Vcc	103	NC	155	NC	207	Vcc
52	Vss	104	NC	156	Vss	208	Vss

Sample Ordering Information

Part Number	Screening	Speed (MHz)	Package
ACT-5230PC-133F22I	Industrial Temperature	133	128 Lead PQUAD
ACT-5230PC-150F22C	Commercial Temperature	150	128 Lead PQUAD
ACT-5230PC-200F22T	Military Temperature	200	128 Lead PQUAD
ACT-5230PC-200F22M	Military Screening	200	128 Lead PQUAD

Part Number Breakdown



* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice.

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