TS4973

1.2W TWO AUDIO INPUTS WITH GAIN CONTROL POWER AMPLIFIER WITH STANDBY MODE ACTIVE LOW

ADVANCE DATA

- OPERATING FROM V_{CC} **= 2.8V to 5.5V**
- RAIL TO RAIL **OUTPUT**
- 1.2W OUTPUT POWER @ Vcc=5V, THD=1%, F=1kHz, with **8**Ω Load
- ULTRA LOW CONSUMPTION IN STANDBY MODE **(10nA)**
- **53dB** PSRR @ 217Hz from 2.8 to 5V
- LOW POP & CLICK
- ULTRA LOW DISTORTION **(0.05%)**
- GAIN SETTINGS PIN : **GS**
- UNITY GAIN STABLE
- **FLIP CHIP PACKAGE 9 x 300µm bumps**

DESCRIPTION

At 3.3v, the TS4973 is an Audio Power Amplifier capable of delivering 400mW of continuous RMS ouput power into a 8Ω bridged-tied loads with 1% THD+N, and 30mW(typ) per channel of continuous average power into stereo 32Ω BTL loads with 0.5% THD+N from 20Hz to 20kHz. An external standby mode control reduces the supply current to less than 10nA. An internal over-temperature shutdown protection is provided.

The TS4973 has been designed for high quality audio applications such as mobile phones and to minimize the number of external components. It has two inputs which can be used to switch the gain between 6dB (internal) or a user's adjustable gain setting with one external resitance.

APPLICATIONS

- Mobile Phones (Cellular / Cordless)
- PDAs
- Laptop/Notebook computers
- Portable Audio Devices

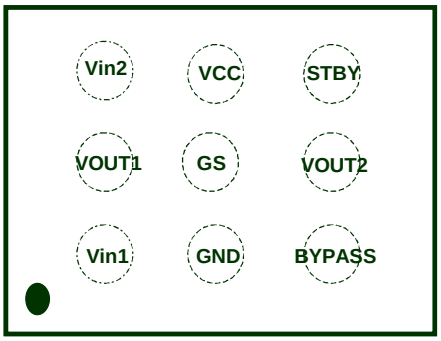
ORDER CODE

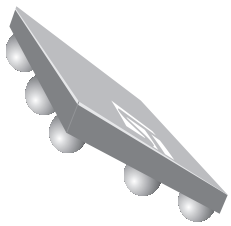
Part Number	Temperature Range	Package	Marking
		J	
TS4973IJT	-40, +85°C	•	A73

J = Flip Chip Package - only available in Tape & Reel (JT))

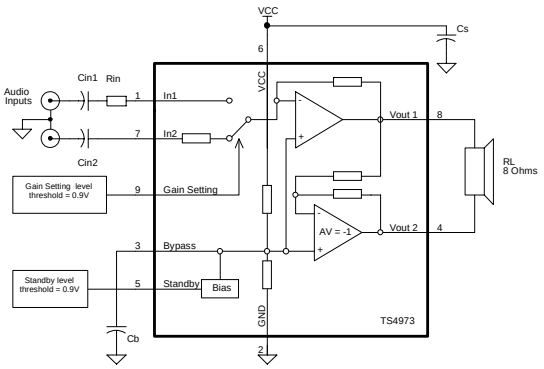
PIN CONNECTIONS (top view)

TS4973IJT - FLIP CHIP





TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient [3]	200	°C/W
Pd	Power Dissipation	Internally Limited[4]	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period, involves abnormal operating condition.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.8 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range	G_{ND} to V_{CC} - 1.5V	V
V_{STB}	Standby Voltage Input : Device ON Device OFF	 $1.5 \le V_{STB} \le V_{CC}$ $GND \le V_{STB} \le 0.4$	V
V_{GS}	Gain Setting Voltage Input : External Gain (In1 Input) Internal Gain (In2 Input)	 $1.5 \le V_{STB} \le V_{CC}$ $GND \le V_{STB} \le 0.4$	V
R_L	Load Resistor	4 - 32	Ω
R_{thja}	Thermal Resistance Junction to Ambient [1]	90	°C/W

1. With Heat Sink Surface = 125mm^2

ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = Gnd, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω	0.85	1.2		W
BTL GAIN	GS = Low input signal Vin = 100mV rms, RL = 8Ω	5.6	6	6.4	dB
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, GS = Low, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio[2] F = 217Hz, RL = 8Ω, GS = Low, Vripple = 200mV rms Input Grounded, Cin = 220nF, Cb = 1µF	50	53		dB
PSRR	Power Supply Rejection Ratio[3] F = 217Hz, RL = 8Ω, GS = Low, Vripple = 200mV rms Input floating, Cb = 1µF		75		dB
Zin	Input Impedance GS = Low	37.5	50	62.5	KΩ
Rfeed	Internal Feedback Resistor	37.5	50	62.5	KΩ
Φ_M	Phase Margin at GS = Low R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Gnd
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ f = 217Hz
3. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ f = 217Hz

ELECTRICAL CHARACTERISTICS

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)[4)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1)] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω	350	500		mW
BTL GAIN	GS = Low input signal Vin = 100mV rms, RL = 8Ω	5.6	6	6.4	dB
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio[2)] f = 217Hz, RL = 8Ω, GS = Low, Vripple = 200mV rms Input Grounded, Cin = 220nF, Cb = 1µF	50	53		dB
PSRR	Power Supply Rejection Ratio[3)] f = 217Hz, RL = 8Ω, GS = Low, Vripple = 200mV rms Input floating, Cb = 1µF		75		dB
Zin	Input Impedance GS = Low	37.5	50	62.5	KΩ
Rfeed	Internal Feedback Resistor	37.5	50	62.5	KΩ
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ f = 217Hz
3. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ f = 217Hz
4. All electrical values are made by correlation between 2.8V and 5V measurements

ELECTRICAL CHARACTERISTICS

V_{CC} = **2.8V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
BTL GAIN	GS = Low input signal Vin = 100mV rms, RL = 8Ω	5.6	6	6.4	dB
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω	250	350		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio[2] F = 217Hz, RL = 8Ω, GS = Low, Vripple = 200mV rms Input Grounded, Cin = 220nF, Cb = 1µF	50	53		dB
PSRR	Power Supply Rejection Ratio[3] F = 217Hz, RL = 8Ω, GS = Low, Vripple = 200mV rms Input Floating, Cb = 1µF		75		dB
Zin	Input Impedance GS = Low	37.5	50	62.5	KΩ
Rfeed	Internal Feedback Resistor	37.5	50	62.5	KΩ
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Gnd
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz
3. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

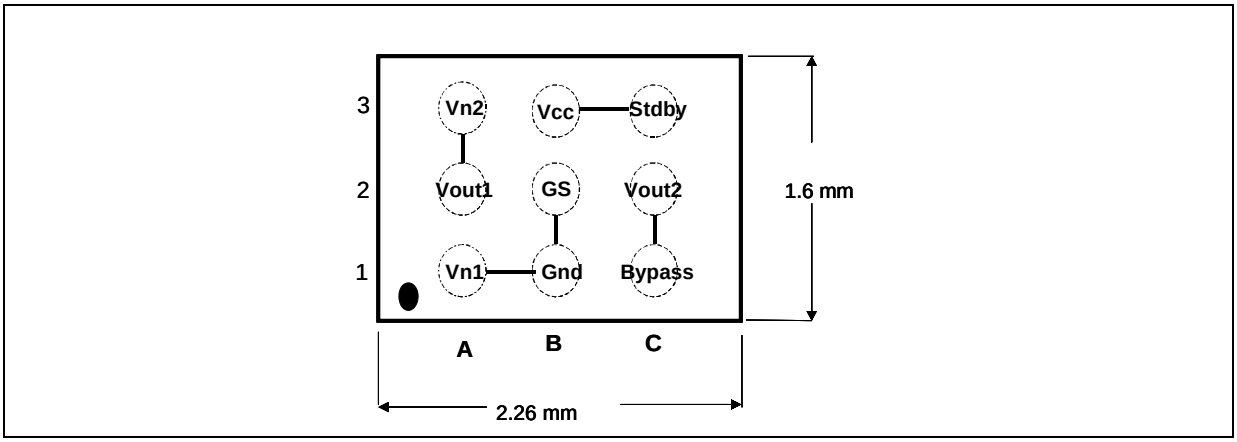
Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain (when GS = high) in conjunction with the internal feedback resistor Rfeed. This resistor also forms a high pass filter with Cin1 Fc = 1 / (2 x Pi x Rin x Cin1)
Cin1	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal In1
Cin2	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal In2. This capacitor also forms a high pass filter with Zin (internal input impedance when Gs = Low Fc = 1 / (2 x Pi x Zin x Cin2)
Cs	Supply Bypass capacitor which provides power supply filtering (Recommended value = 1µF)
Cb	Bypass pin capacitor which provides half supply filtering (Recommended value = 1µF)
Gv	Closed loop gain in BTL configuration When Gs = Low, Gv = 2 or 6dB When GS = high, Gv = 2 x (Rfeed / Rin). Rfeed value see Electrical Characteristics.

REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor Cs = 1µF.

2. The standby response time is about 1µs.

DAISY CHAIN MECHANICAL DATA (Top View : all drawings dimensions are in millimeters)



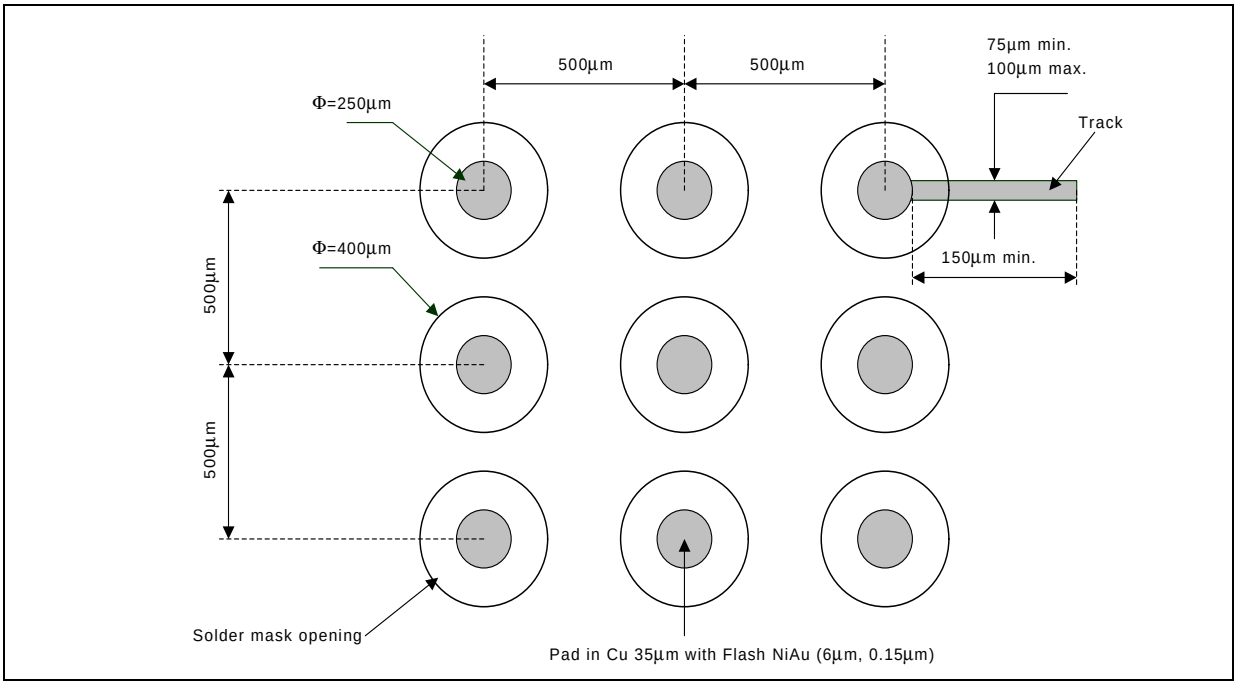
REMARKS

Daisy chain sample is featuring pins connection two by two. The schematic above is illustrating the way connecting pins each other. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting an Ohmeter between pin 8 and pin 1, the soldering process continuity can be tested.

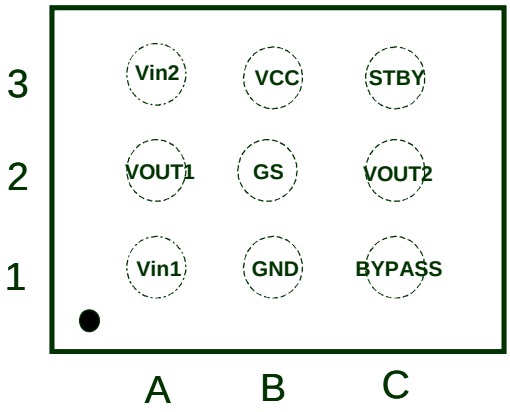
ORDER CODE

Part Number	Temperature Range	Package	Marking
		J	
TSDC05IJT	-40, +85°C	•	DC5

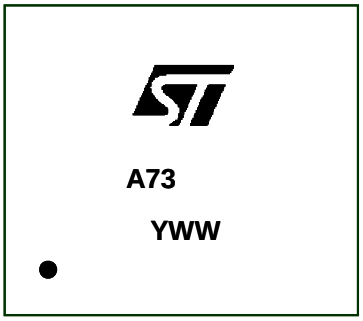
TS4973 Footprint Recommendation



PIN OUT (top view)



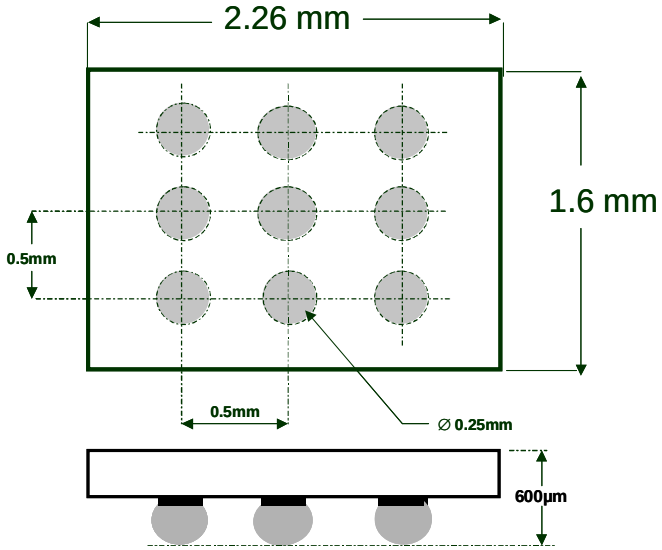
MARKING (top view)



- Logo : **ST**
- Part Number : **A73**
- Date Code : YWW
- The Dot is for marking pin **A1**

PACKAGE MECHANICAL DATA

FLIP CHIP - 9 BUMPS



- Die size : **2.26mm x 1.6mm** (±10%)
- Die height (including bumps) : **600µm ±30µm**
- Bumps diameter : **300µm ±15µm**
- Pitch: **500µm ±10µm**

TAPE & REEL SPECIFICATION (top view)