TOSHIBA TPD2005F

TOSHIBA INTELLIGENT POWER DEVICE SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD2005F

HIGH-SIDE POWER SWITCH ARRAY (8 CHANNELS) for MOTORS, SOLENOIDS, and LAMP DRIVES

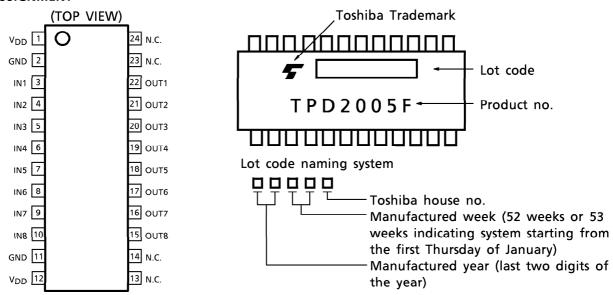
The TPD2005F is an 8-channel high-side switch array for vertical power MOS FET output. A monolithic power IC, it can directly drive a power load from a CMOS or TTL logic circuit (such as an MPU). It offers overcurrent and overtemperature protection functions.

FEATURES

- A high-side switch array incorporating an N-channel power MOS FET (1.2 Ω max.) and an 8-channel charge
- Can directly drive a power load from a microprocessor.
- Built-in protection against overtemperature protection and overcurrent protection.
- 8-channel access enables space-saving design.
- High operating voltage: 40 V
- : 1.2 Ω max. @V_{DD} = 12 V, I_O = 0.5 A (per channel) Low on-resistance
- Supports parallel operation.
- Low operating current : 5 mA max. $@V_{DD} = 40 \text{ V}, V_{IN} = 0 \text{ V}$
- Supplied in an SSOP-24 package (300 mil) in embossed taping.

PIN ASSIGNMENT

MARKING



This device uses MOS structure, it is sensitive to electrostatics. Please take this into account.

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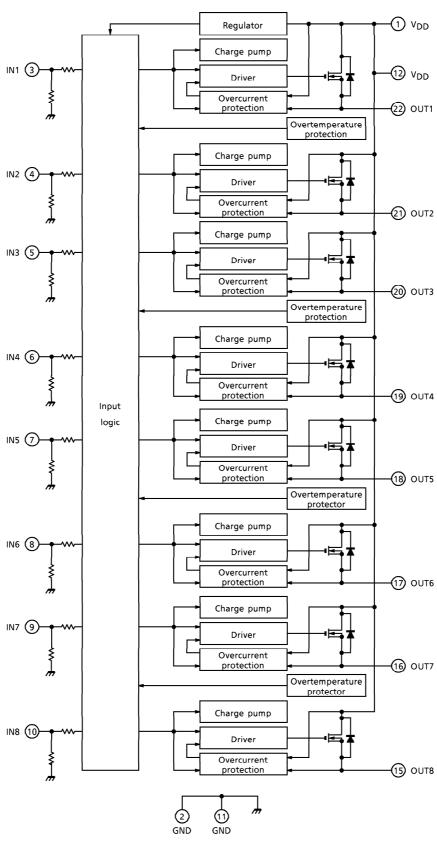
 The information contained herein is subject to change without notice.

MARKARARA

SSOP24-P-300-1.00B

Weight: 0.29 g (typ.)

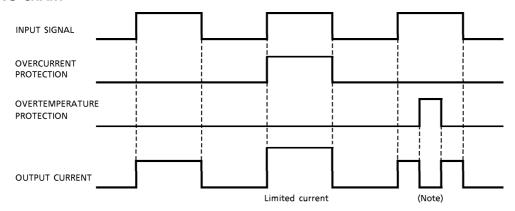
BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION					
1	V_{DD}	Power supply pin; in common with the pin no.12 internally.					
2	GND	GND pin; in common with the pin no.11 internally.					
3	IN1	Control input pin for channel 1 and built-in pull-down resistor (100 k Ω typ.)					
4	IN2	Control input pin for channel 2 and built-in pull-down resistor (100 k Ω typ.)					
5	IN3	Control input pin for channel 3 and built-in pull-down resistor (100 k Ω typ.)					
6	IN4	Control input pin for channel 4 and built-in pull-down resistor (100 k Ω typ.)					
7	IN5	Control input pin for channel 5 and built-in pull-down resistor (100 k Ω typ.)					
8	IN6	Control input pin for channel 6 and built-in pull-down resistor (100 k Ω typ.)					
9	IN7	Control input pin for channel 7 and built-in pull-down resistor (100 k Ω typ.)					
10	IN8	Control input pin for channel 8 and built-in pull-down resistor (100 k Ω typ.)					
11	GND	GND pin; in common with the pin no.2 internally.					
12	V_{DD}	Power supply pin; in common with the pin no.1 internally.					
13	N.C.	_					
14	N.C.	_					
15	OUT8	Output pin for channel 8					
16	OUT7	Output pin for channel 7					
17	OUT6	Output pin for channel 6					
18	OUT5	Output pin for channel 5					
19	OUT4	Output pin for channel 4					
20	OUT3	Output pin for channel 3					
21	OUT2	Output pin for channel 2					
22	OUT1	Output pin for channel 1					
23	N.C.	_					
24	N.C.	_					

TIMING CHART



(Note): The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

TRUTH TABLE

INPUT SIGNAL	OUTPUT SIGNAL	STATE
L	L	Normal
Н	Н	Nominal
L	L	Oversurrent protection
Н	Internally limited	Overcurrent protection
L	Ĺ	Overtemperature
Н	L	protection

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	
Supply Voltage	V_{DD}	45	V	
Input Voltage	VIN	-0.5~7	٧	
Drain-source Voltage	V _{DS}	60	V	
Output Current	lo	Internally Limited	Α	
Power Dissipation	D-	0.8	w	
(Operating All Channels, Ta = 25°C)	PT	1.5 (Note)		
Single Pulse Avalanche Energy	EAS	10	mJ	
Operating Temperature	T _{opr}	- 40~85	°C	
Junction Temperature	Tj	150	°C	
Storage Temperature	T _{stg}	- 55∼150	°C	

THERMAL CHARACTERISTIC

CHARACTERISTIC	SYMBOL	RATING	UNIT
Thermal Resistance Junction to Ambient	Σ Β	156.3	°C/W
(Operating All Channels, Ta = 25°C)	Σ R $_{th}$ (j-a)	83.4 (Note)	C / VV

(Note) : $60 \text{ mm} \times 60 \text{ mm} \times 1.6 \text{ t}$ when a device is mounted on a glass epoxy PCB. (DC)

CHARACTE	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Operating Supply Voltage		V_{DD}	—	_	8	_	40	V
Supply Current		l _{DD}	_	V _{DD} = 40 V, V _{IN} = 0 V	_	_	5	mA
Innet Maltana	"L" level	V _{IL}	_		_	_	1.5	· V
Input Voltage	"H" level	V _{IH}	_		3.5	_	_	
Input Current		Iμ	_	V _{DD} = 24 V, V _{IN} = 0 V	- 10	_	10	
		lн	_	V _{DD} = 24 V, V _{IN} = 5V	_	50	200	μA
Output On Resistance		R _{DS} (ON)	_	$V_{DD} = 12 \text{ V}, I_{O} = 0.5 \text{ A}$	_	0.9	1.2	Ω
Output Leakage Current		loL	_	$V_{DD} = 40 \text{ V}, V_{IN} = 0 \text{ V}$	_	_	100	μΑ
Overcurrent Protection		Ις	_	_	1	_	3	Α
Overtemperature	Temperature	T _{SD}	_	_	_	160	_	°C
Protection	Hysteresis	∆T _{SD}	_	_	_	10	_	'
Switching Time		tON	1	V_{DD} = 12 V, R_L = 24 Ω	_	11	200	μ s
		tOFF	'		_	4	50	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 8~40 V, Ta = 25°C)

DESCRIPTION OF PROTECTOR CIRCUIT

(1) Overtemperature Protection

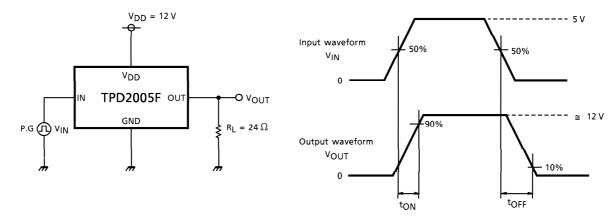
- Four overheating detector circuits are built in. One each for channels 1 and 2; channels 3 and 4; channels 5 and 6; and channels 7 and 8. The circuit logic is that, when any of the four detectors detects overheating, the circuit turns the output of both channels off (for example, channels 1 and 2).
- The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

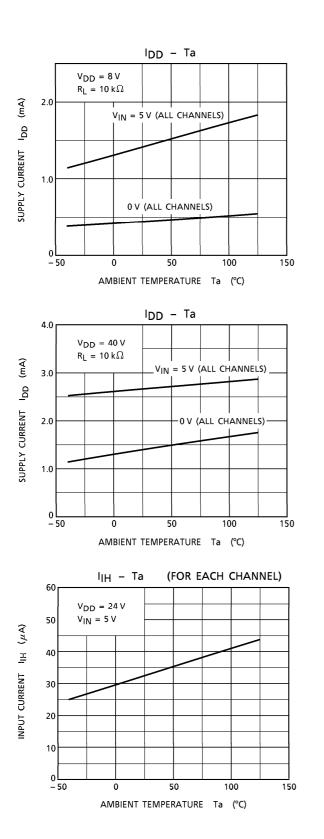
(2) Overcurrent Protection

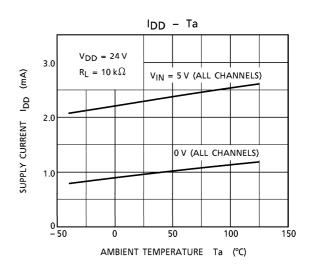
• When overcurrent is detected, the overcurrent limiter function limits the output current. Normal operation is restored when the load current drops below the overcurrent detection value.

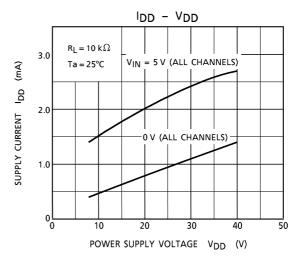
TEST CIRCUIT

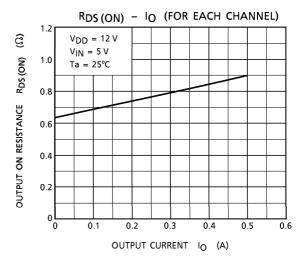
Switching Time

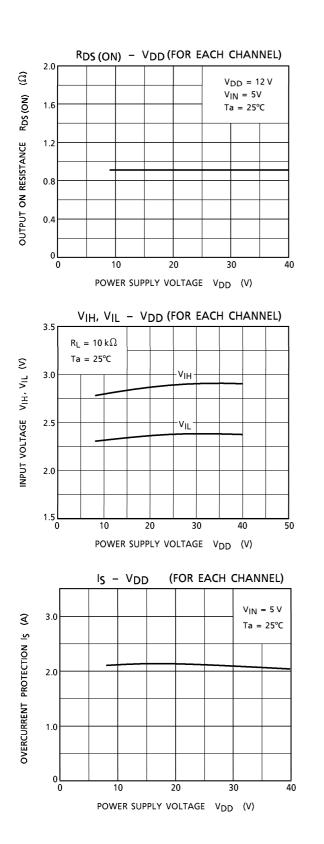


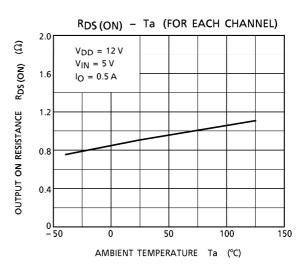


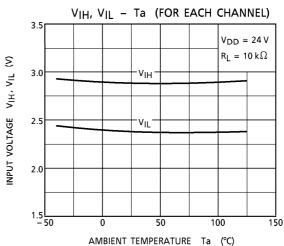


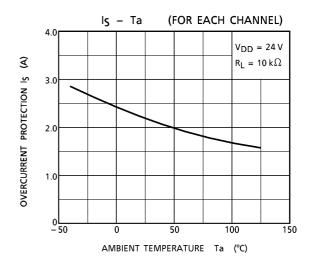


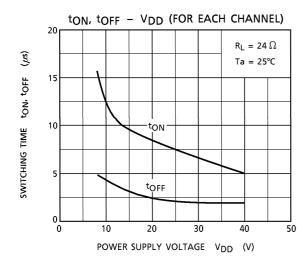


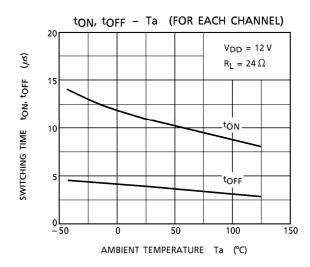


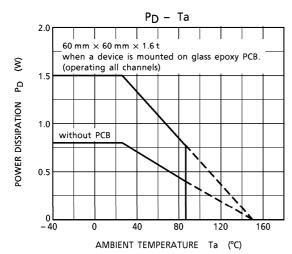


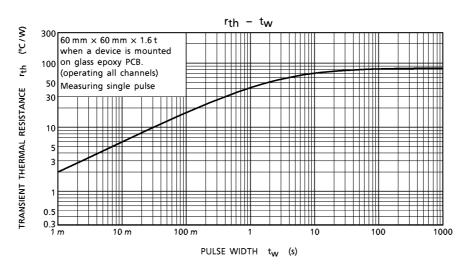












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CAUTION ON USAGE

1. As protection against reverse connection of batteries is not provided, take protective measures using external circuits.

2. As a negative bias protector circuit is not built into the output pins, if negative bias is applied to the output pins, be sure to connect a freewheel diode between OUT and GND.

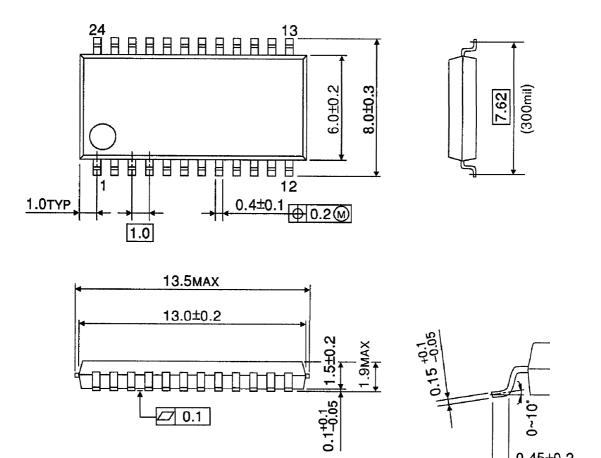
MOISTURE-PROOF PACKING

After the pack is opened, use the devices in a 30°C, 60% RH environment, and within the 48 hours. Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.

Tape packing quantity: 500 devices/reel (EL) or 2000 devices/reel (EL1)

PACKAGE DIMENSIONS

SSOP24-P-300-1.00B Unit: mm



Weight: 0.29 g (typ.)

0.45±0.2