STLC7550

LOW POWER LOW VOLTAGE ANALOG FRONT END

- GENERAL PURPOSE SIGNAL PROCESSING ANALOG FRONT END (AFE)
- TARGETED FOR V.34bis MODEM AND 56Kbps MODEM APPLICATIONS
- 16-BIT OVERSAMPLING ΣΔ A/D AND D/A CONVERTERS
- 83dB SIGNAL TO NOISE RATIO FOR SAMPLING FREQUENCY UP TO 9.6kHz @ 3V
- 87dB DYNAMIC RANGE @ 3V
- FILTER BANDWIDTHS : 0.425 x THE SAMPLING FREQUENCY
- ON-CHIP REFERENCE VOLTAGE
- SINGLE POWER SUPPLY RANGE : 2.7 TO 5.5V
- LOW POWER CONSUMPTION LESS THAN 30mW OPERATING POWER 3V
- STAND-BY MODE POWER CONSUMPTION LESS THAN 3µW at 3V
- PROGRAMMING SAMPLING FREQUENCY
- MAX. SAMPLING FREQUENCY : 45kHz
- SYNCHRONOUS SERIAL INTERFACE FOR PROCESSOR DATAS EXCHANGE. MASTER OR SLAVE OPERATIONS
- 0.50µm CMOS PROCESS
- TQFP44 PACKAGE
- STLC7546 MODE OF OPERATION COMPATIBLE

DESCRIPTION

The STLC7550 is a single chip Analog Front-end (AFE) designed to implement modems up to 56Kbps.

It has been especially designed for host processing application in which the modulation software (V.34bis, 56Kbps) is performed by the main application processor : Pentium, Risc or DSP processors.

The main target of this device is stand alone appliances as Hand Held PC (HPC), Personnal Digital Assistants (PDA), Webphones, Network Computers, Set Top Boxes for Digital Television (Satellite and Cable).

To comply with such applications STLC7550 is powered nominally at 3V only.

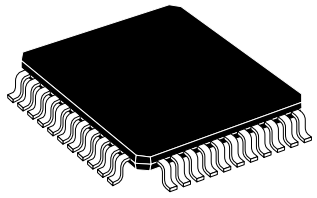
Maximum Power Dissipation 30mW is well suited for Battery operations.

In case of battery low, STLC7550 will continue to work even at a 2.7V level.

STLC7550 also provides clock generator for all sampling frequencies requested for V.34bis and 56Kbps applications.

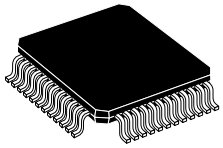
This new AFE can also be used for PC mother boards or add-on cards or stand alone MODEMs.

It can be used in a master mode or slave mode. The slave mode eases multi AFE architecture design in saving external logical glue.



TQFP44 (10 x 10 x 1.40 mm)
(Full Plastic Quad Flat Pack)

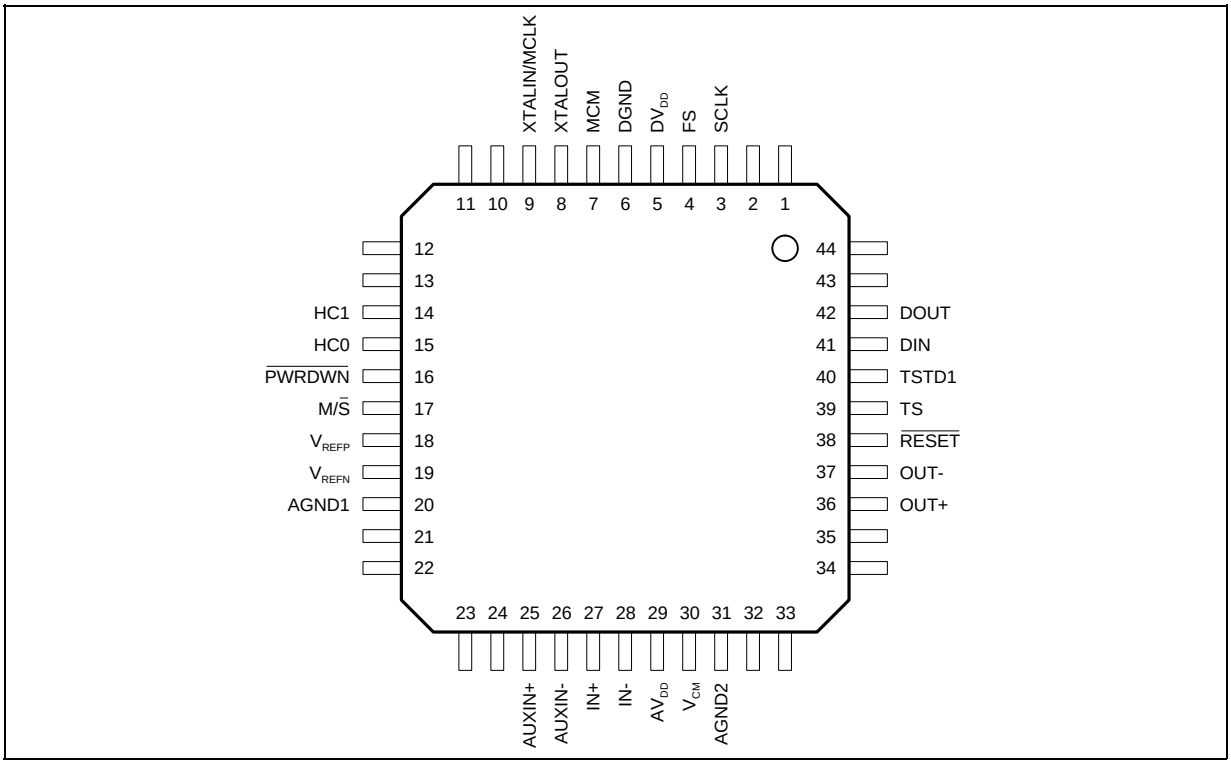
ORDER CODE : STLC7550TQFP



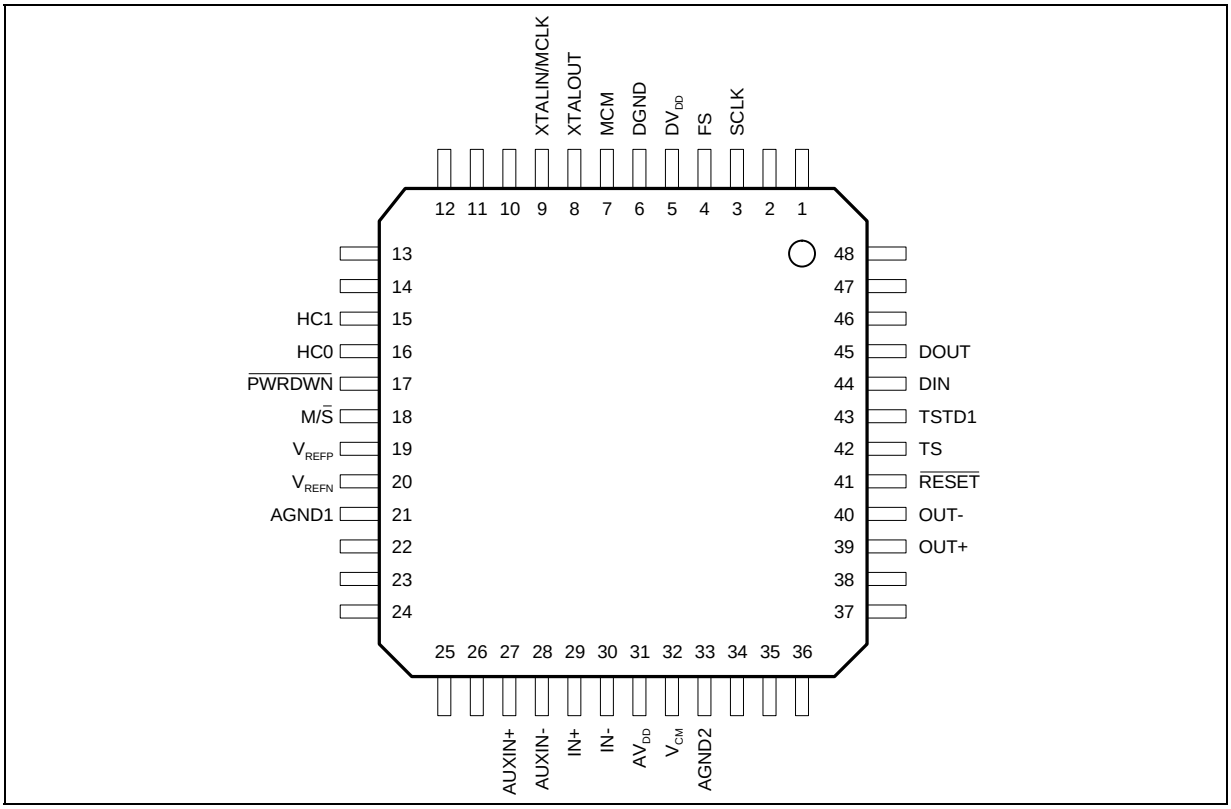
TQFP48 (7 x 7 x 1.40mm)
(Full Plastic Quad Flat Pack)

ORDER CODE : STLC7550TQF7

PIN CONNECTIONS (TQFP44)



PIN CONNECTIONS (TQFP48)



PIN LIST

Pin Number		Name	Type	Description
TQFP44	TQFP48			
1 - 2, 10 to 13, 21 to 24, 32 to 35, 43 - 44	1 - 2, 10 to 14, 22 to 26, 34 to 38, 46 to 48	NC	-	Not connected
3	3	SCLK	O	Shift Clock Output
4	4	FS	I/O	Frame Synchronization Input (slave)/Output (master)
5	5	DV_{DD}	I	Positive Digital Power Supply (2.7V TO 5.5V)
6	6	DGND	I	Digital Ground
7	7	MCM	I	Master Clock Mode
8	8	XTALOUT	O	Crystal Output
9	9	XTALIN/MCLK	I	Crystal Input (MCM = 1) / External Clock (MCM = 0)
14	15	HC1	I	Hardware Control Input
15	16	HC0	I	Hardware Control Input
16	17	$\overline{PWRDWN}$	I	Power down Input
17	18	$M/\overline{S}$	I	Master/Slave Mode Control Pin Input
18	19	V_{REFP}	O	16-bit D/A and A/D Positive Reference Voltage
19	20	V_{REFN}	O	16-bit D/A and A/D Negative Reference Voltage
20	21	AGND1	I	Analog Ground
25	27	AUXIN+	I	Non-inverting Input to Auxiliary Analog Input
26	28	AUXIN-	I	Inverting Input to Auxiliary Analog Input
27	29	IN+	I	Non-inverting Input to Analog Input Amplifier
28	30	IN-	I	Inverting Input to Analog Input Amplifier
29	31	AV_{DD}	I	Positive Analog Power Supply (2.7V to 5.5V)
30	32	V_{CM}	O	Common Mode Voltage Output (AV_{DD}/2)
31	33	AGND2	I	Analog Ground
36	39	OUT+	O	Non-inverting Smoothing Filter Output
37	40	OUT-	O	Inverting Smoothing Filter Output
38	41	$\overline{RESET}$	I	Reset Function to initialize the internal counters
39	42	TS	I	Timeslot Control Input
40	43	TSTD1	I/O	Digital Input/Output reserved for test
41	44	DIN	I	Serial Data Input
42	45	DOUT	O	Serial Data Output

7550-01.TBL

PIN DESCRIPTION

1 - POWER SUPPLY (5 pins)

1.1 - Analog V_{DD} Supply (AV_{DD})

This pin is the positive analog power supply voltage for the DAC and the ADC section.

It is not internally connected to digital V_{DD} supply (DV_{DD}).

In any case the voltage on this pin must be higher or equal to the voltage of the Digital power supply (DV_{DD}).

1.2 - Digital V_{DD} Supply (DV_{DD})

This pin is the positive digital power supply for DAC and ADC digital internal circuitry.

1.3 - Analog Ground (AGND1, AGND2)

These pins are the ground return of the analog DAC (ADC) section.

1.4 - Digital Ground (DGND)

This pin is the ground for DAC and ADC internal digital circuitry.

Notes : 1. To obtain published performance, the analog V_{DD} and Digital V_{DD} should be decoupled with respect to Analog Ground and Digital Ground, respectively. The decoupling is intended to isolate digital noise from the analog section ; decoupling capacitors should be as close as possible to the respective analog and digital supply pins.

2. All the ground pins must be tied together. In the following section, the ground and supply pins are referred to as GND and V_{DD}, respectively.

PIN DESCRIPTION (continued)

2 - HOST INTERFACE (10 pins)

2.1 - Data In (DIN)

In Data Mode, the data word is the input of the DAC channel. In software, the data word is followed by the control register word.

2.2 - Data Out (DOUT)

In Data Mode, the data word is the ADC conversion result. In software, the data word is followed by the register read.

2.3 - Frame Synchronization (FS)

In master mode, the frame synchronization signal is used to indicate that the device is ready to send and receive data. The data transfer begins on the falling edge of the frame-sync signal. The frame-sync is generated internally and goes low on the rising edge of SCLK in master mode. In slave mode the frame is generated externally.

2.4 - Serial Bit Clock (SCLK)

SCLK clocks the digital data into DIN and out of DOUT during the frame synchronization interval. The Serial bit clock is generated internally.

2.5 - Reset Function ($\overline{\text{RESET}}$)

The reset function is to initialize the internal counters and control register. A minimum low pulse of 100ns is required to reset the chip. This reset function initiates the serial data communications. The reset function will initialize all the registers to their default value and will put the device in a pre-programmed state. After a low-going pulse on RESET, the device registers will be initialized to provide an over-sampling ratio equal to 160, the serial interface will be in data mode, the DAC attenuation will be set to infinite, the ADC gain will be set to 0dB, the Differential input mode on the ADC converter will be selected, and the multiplexor will be set on the main inputs IN+ and IN-. After a reset condition, the first frame synchronization corresponds to the primary channel.

2.6 - Power Down ($\overline{\text{PWRDWN}}$)

The Power-Down input powers down the entire chip (< 50µW). When PWRDWN Pin is taken low, the device powers down such that the existing internally programmed state is maintained. When $\overline{\text{PWRDWN}}$ is driven high, full operation resumes after 1ms. If the PWRDWN input is not used, it should be tied to V_{DD}.

2.7 - Hardware Control (HC0, HC1)

These two pins are used for Hardware/Software Control of the device. The data on HC0 and HC1 will be latched on to the device on the rising edge of the Frame Synchronization Pulse. If these two pins are low, Software Control Mode is selected. When in Software Control Mode, the LSB of the 16-bit word will select the Data Mode (LSB = 0) or the Control Mode (LSB = 1). Other combinations of HC0/HC1 are for Hardware Control. These inputs should be tied low if not used.

2.8 - Master/Slave Control (M/$\overline{\text{S}}$)

When M/$\overline{\text{S}}$ is high, the device is in master mode and Fs is generated internally. When M/$\overline{\text{S}}$ is low, the device is in slave mode and Fs must be generated externally.

2.9 - Master Clock Mode (MCM)

When MCM is high, XTALIN is provided externally and must be equal to 36.864MHz. When MCM is low, XTALIN is provided externally and must be equal to oversampling frequency : Fs x Over (see Clock Block Diagram and §4 Modes of Operation).

2.10 - Timeslot Control (TS)

When TS = 0 the data are assigned to the first 16 bits after falling edge of FS (7546 mode) otherwise the data are bits 17 to 32.
The case M/S = 1 with TS = 1 is reserved for life-test (transmit gain fixed to 0dB).

3 - CLOCK SIGNALS (2 pins)

Depending on MCM value, these pins have different function.

3.1 - MCM = 1 (XTALIN, XTALOUT)

These pins must be tied to external crystal. For the value of crystal see Functional Description Chapter Part 3.

3.2 - MCM = 0 (MCLK, XTALOUT)

MCLK Pin must be connected to an external clock. XTALOUT is not used.

PIN DESCRIPTION (continued)

4 - ANALOG INTERFACE (9 pins)

4.1 - DAC and ADC Positive Reference Voltage Output (V_{REFP})

This pin provides the Positive Reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs, and its nominal value is 1.25V. V_{REFP} should be externally decoupled with respect to V_{CM}.

4.2 - DAC and ADC Negative Reference Voltage Output (V_{REFN})

This pin provides the Negative Reference Voltage used by the 16-bit converters, and should be externally decoupled with respect to V_{CM}.

4.3 - Common Mode Voltage Output (V_{CM})

This output pin is the common mode voltage (AV_{DD} - AGND)/2. This output must be decoupled with respect to GND.

4.4 - Non-inverting Smoothing Filter Output(OUT+)

This pin is the non-inverting output of the fully differential analog smoothing filter.

4.5 - Inverting Smoothing Filter Output (OUT-)

This pin is the inverting output of the fully differential analog smoothing filter. Outputs OUT+ and OUT- provide analog signals with maximum peak-to-peak amplitude 2 x V_{REF}, and must be followed by an external two pole smoothing filter. The external filter follows the internal single pole switch capacitor filter. The cutoff frequency of the external filter must be greater than two times the sampling frequency (FS), so that the combined frequency response of both the internal and external filters is flat in the passband . The attenuator of the last output stage can be programmed to 0dB, 6dB or infinite.

4.6 - Non-inverting Analog Input (IN+)

This pin is the differential non-inverting ADC input.

4.7 - Inverting Analog Input (IN-)

This pin is the differential inverting ADC input. These analog inputs (IN+, IN-) are presented to the Sigma-Delta modulator. The analog input peak-to-peak differential signal range must be less than 2 x V_{REF}, and must be preceded by an external single pole anti-aliasing filter. The cut-off frequency of the filter must be lower than one half the oversampling frequency. These filters should be set as close as possible to the IN+ and IN- pins. The gain of the first stage is programmable (see Table 3).

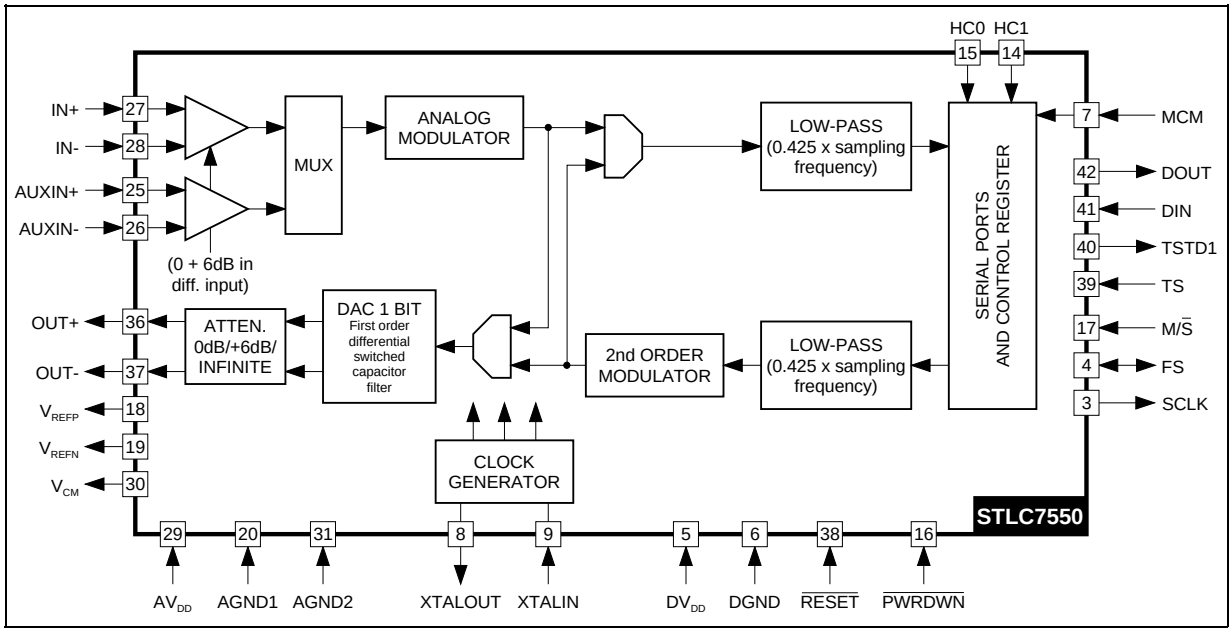
4.8 - Non-inverting Auxiliary Analog Input (AUX IN+)

This pin is the differential non-inverting auxiliary ADC input. The characteristics are same as the IN+ input.

4.9 - Inverting Auxiliary Analog Input (AUX IN-)

This pin is the differential inverting auxiliary ADC input. The characteristics are same as the IN- input. The input pair (IN+/IN- or AUX IN+/AUX IN-) are software selectable.

BLOCK DIAGRAM (TQFP44)



7550-02.EPS

FUNCTIONAL DESCRIPTION

1 - TRANSMIT D/A SECTION

The functions included in the Tx D/A section are detailed hereafter. 16-bit 2's complement data format is used in the DAC channel.

1.1 - Transmit Low Pass Filters

The transmit low pass filter is basically an interpolating filter including a sinx/x correction. It is a combination of Finite Impulse Response filter (FIR) and an Infinite Impulse Response filter (IIR). The digital signal from the serial interface gets interpolated by 2, 3, 4, 5 or 6 x Sampling Frequency (FS) through the IIR filter. The signal is further interpolated by 32 x FS x n (with n equal to 2, 3, 4, 5, 6) through the IIR and FIR filter. The low pass filter is followed by the DAC. The DAC is oversampled at 64, 96, 128, 160, 192 x FS. The oversampling ratio is user selectable.

1.2 - D/A Converter

The oversampled D/A converter includes a second order digital noise shaper, a one bit D/A converter and a single pole analog low-pass filter.

The attenuation of the last output stage can be programmed to 0dB, +6dB or infinite. The cut-off frequency of the single pole switch-capacitor low-pass filter is :

$$fc_{-3dB} = \frac{OCLK}{2 \cdot \pi \cdot 10}$$

with OCLK = Oversampling Clock frequency.

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components.
At least 79dB signal to noise plus distortion ratio can be obtained in the frequency band of 0.425 x 9.6kHz (with an oversampling ratio equal to 160).

2 - RECEIVE A/D SECTION

The different functions included in the ADC channel section are described below. 16-bit 2's complement data format is used in the ADC.

2.1 - A/D Converter

The oversampled A/D converter is based on a second order sigma-delta modulator. To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. Single-ended mode can also be used. The ADC is oversampled at 64, 96, 128, 160 or 192 x FS. The oversampling ratio is user selectable. At least -85dB SNDR can be expected in the 0.425 x 9.6kHz bandwidth with a -6dBr differential input signal and an oversampling ratio equal to 160.

2.2 - Receive Low Pass Filter

It is a decimation filter. The decimation is performed by two decimation digital filters : one decimation FIR filter and one decimation IIR filter.
The purpose of the FIR filter is to decimate 32 times the digital signal coming from the ADC modulator. The IIR is a cascade of 5 biquads. It provides the low-pass filtering needed to remove the noise remaining above half the sampling frequency. The output of the IIR will be processed by the DSP.

3 - CLOCK GENERATOR

The master clock, MCLK is provided by the user thanks to a crystal or external clock generator (see Figure 1).

The MCLK could be equal to 36.864MHz (MCM = 1). In that case thanks to the divider M x Q, the STLC7550 is able to generate all V.34bis and 56 Kbps sampling frequencies (see Table 1).
When MCM = 0, the MCLK must be equal to the oversampling frequency : Fs x OVER (7546 mode).

The ADC and DAC are oversampled at the OCLK frequency. OCLK is equal to the shift clock used in the serial interface.

The MCLK frequency should be :
MCLK = K x Sampling frequency

Combination of M, Q and oversampling ratios allows to generate several sampling frequencies.

Recommended values for classical modem applications are as follow :

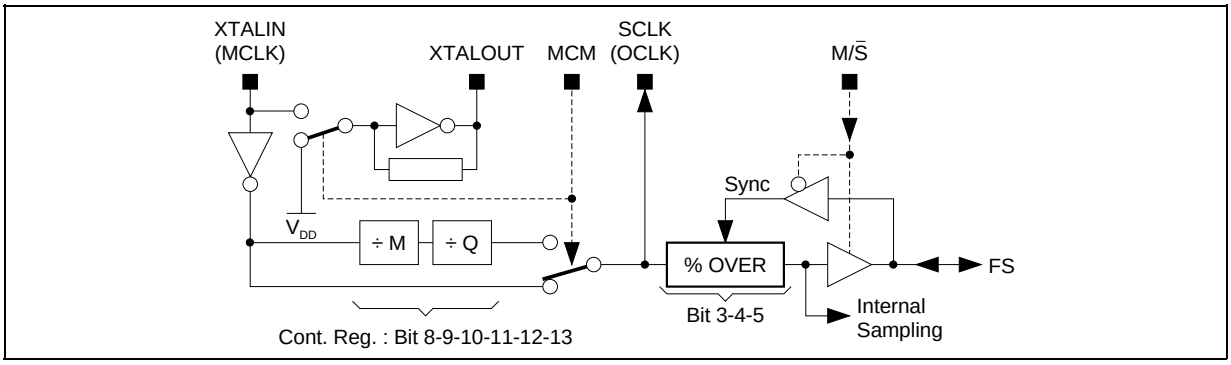
Table 1 : Sampling Frequencies Generation

F (kHz)	FQ = 36.864MHz (1)			FQ = 18.432MHz			FQ = 9.216MHz		
	M	Q	over	M	Q	over	M	Q	over
16.00	3	6	128	2	4.5	128	1	6	96
13.96	3	5.5	160	-	-	-	-	-	-
13.71	3	7	128	1	7	192	1	7	96
12.80	3	6	160	2	4.5	160	1	4.5	160
12.00	3	8	128	2	6	128	1	6	128
11.82	3	6.5	160	-	-	-	-	-	-
10.97	3	7	160	-	-	-	-	-	-
10.47	4	5.5	160	2	5.5	160	1	5.5	160
10.29	4	7	128	2	7	128	1	7	128
9.60	4	6	160	2	6	160	1	6	160
9.00	4	8	128	2	8	128	1	8	128
8.86	4	6.5	160	2	6.5	160	1	6.5	160
8.23	4	7	160	2	7	160	1	7	160
8.00	4	6	192	2	6	192	1	6	192
7.20	4	8	160	2	8	160	1	8	160

Note : 1. Recommended value.

FUNCTIONAL DESCRIPTION (continued)

Figure 1 : Clock Block Diagram



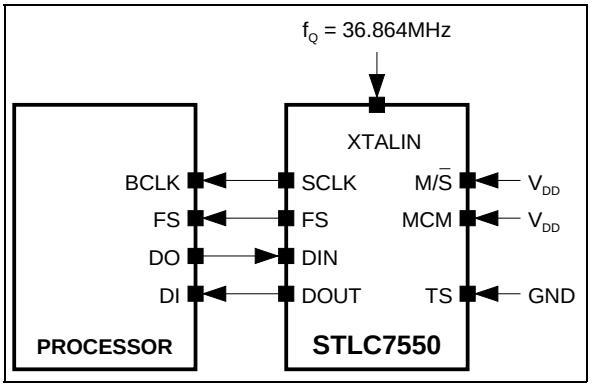
4 - MODES OF OPERATION

Thanks to MCM and M/$\overline{S}$ programmation pins we can get the following configuration.

Configuration 1 : MCM = 1, M/$\overline{S}$ = 1

The STLC7550 is in master mode and we have :
Fs = XTAL IN / (M x Q x OVER)
Fs and SCLK are output pins.

Figure 2 : Configuration 1



Configuration 2 : MCM = 1, M/$\overline{S}$ = 0

The STLC7550 is in slave mode. SCLK is provided by the STLC7550, the processor generates the Fs and controls the phase of the sampling frequency. Fs must be the result of a division of a number of cycles of SLCK (Fs = SCLK % OVER).

Configuration 3 : MCM = 0, M/$\overline{S}$ = 1

The STLC7550 is in master mode and the processor provides the XTAL IN = MCLK = OCLK. The STLC7550 generates the Fs from OCLK. In this mode the configuration 3 is equivalent to the STLC7546 mode.

Configuration 4 : MCM = 0, M/$\overline{S}$ = 0

The STLC7550 is in slave mode.

The configuration 4 is equivalent to configuration 3 but the Fs is generated and phase controlled by the processor.

Figure 3 : Configuration 2

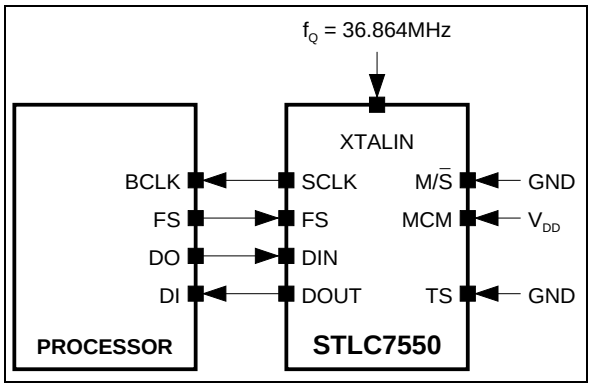
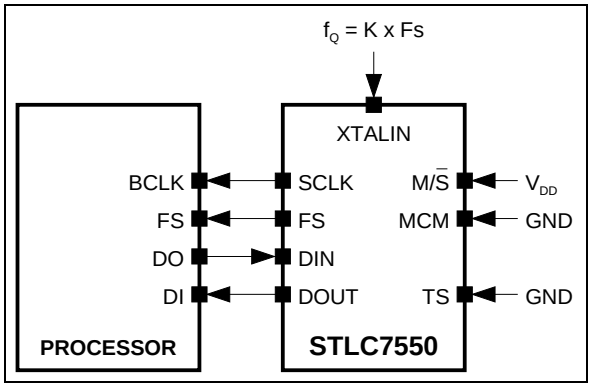


Figure 4 : Configuration 3 (7546 mode)



Configuration 5 : MCM = 1, M/$\overline{S}$ = 1 (master codec)
MCM = 0, M/$\overline{S}$ = 0 (slave codec)

This is dual codec application.
The master codec has his data in timeslot 0 and the slave codec has his data in timeslot 1 thanks to the programmation of TS.

FUNCTIONAL DESCRIPTION (continued)

Figure 5 : Configuration 4

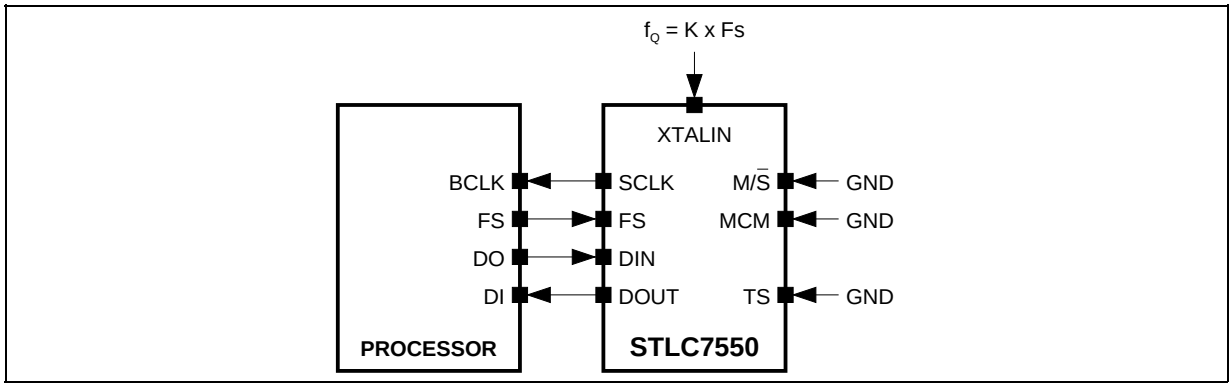
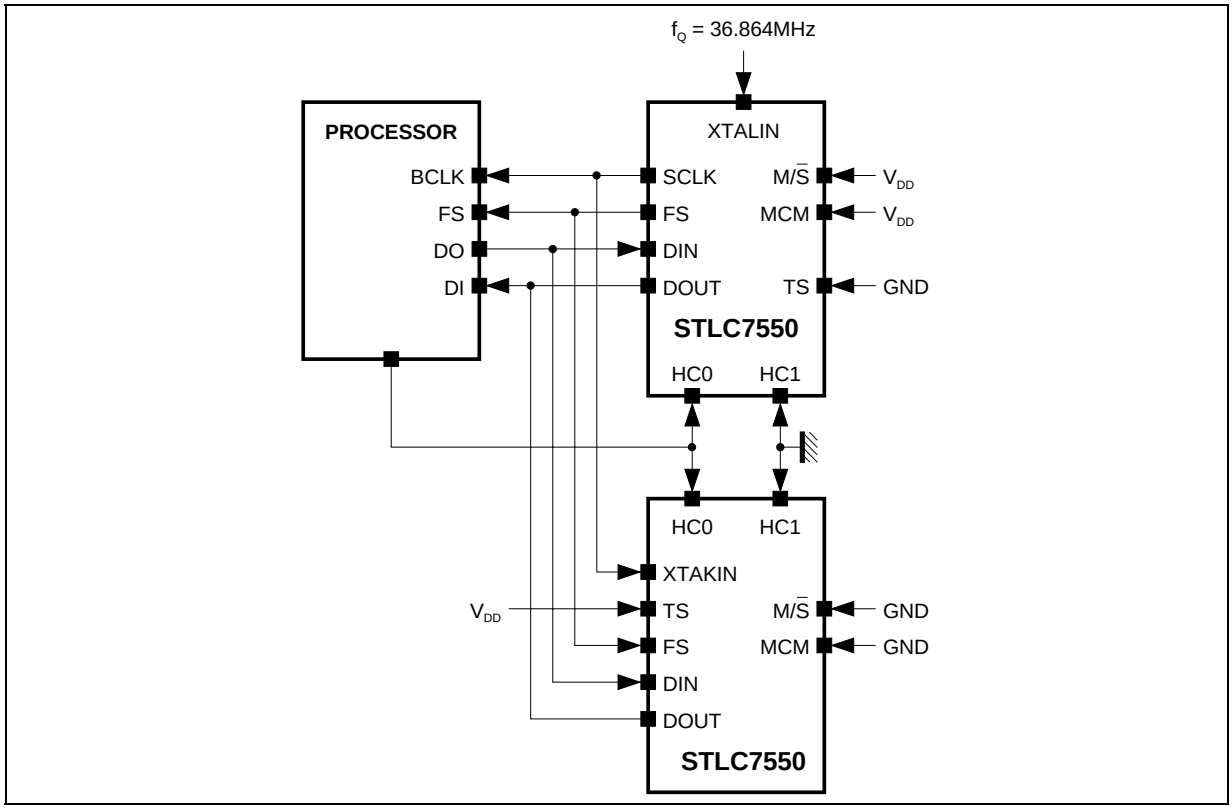


Figure 6 : Configuration 5



FUNCTIONAL DESCRIPTION (continued)

5 - HOST INTERFACE

The Host interface consist of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input.

Two modes of serial transfer are available :

- First : Software mode for 15-bit transmit data transfer and 16-bit receive data transfer
- Second : hardware mode for 16-bit data transfer.

Both modes are selected by the Hardware Control pins (HC0, HC1).

The data to the device, input/output are MSB-first in 2's complement format (see Table 2).

When Control Mode is selected, the device will internally generate an additional Frame Synchronization Pulse (Secondary Frame Synchronization Pulse) at the midpoint of the original Frame Period. If the device is in slave mode the additional frame sync (secondary frame sync pulse) must be generated by the processor. The Original Frame Synchronization Pulse will also be referred to as the Primary Frame Synchronization Pulse.

Table 2 : Mode Selection

HC1	HC0	LSB	Useful Data	Secondary FSYNC	Description
0	0	0	15bits	No	Software Mode for Data Transfer only.
0	0	1	15bits (+16bits reg.)	Yes	Software Mode for Data Transfer + Control Register Transfer.
0	1	X	16bits	No	Hardware Mode for Data Transfer only.
1	X	X	16bits (+16bits reg.)	Yes	Hardware Mode for Data Transfer + Control Register Transfer.

Figure 7 : Data Mode

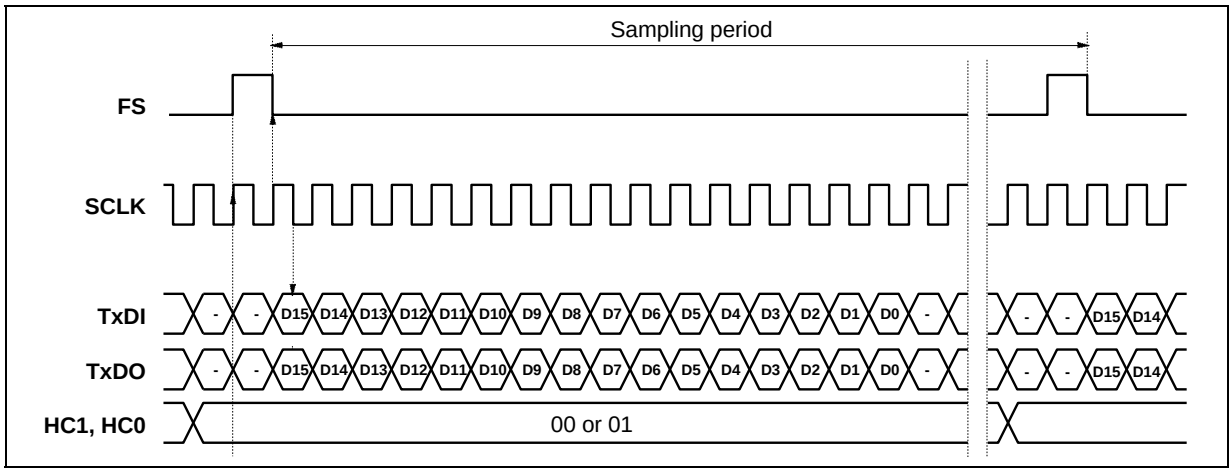
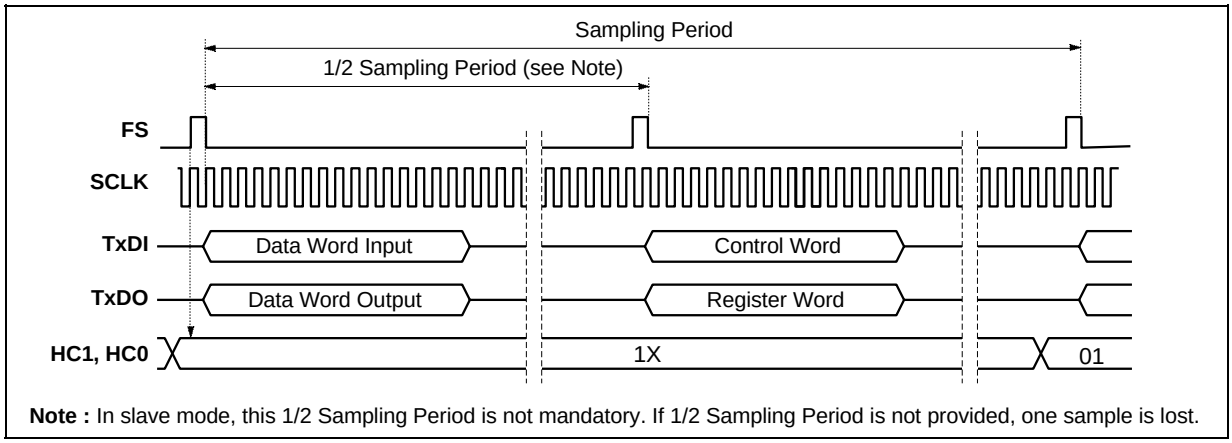


Figure 8 : Mixed Mode



Note : In slave mode, this 1/2 Sampling Period is not mandatory. If 1/2 Sampling Period is not provided, one sample is lost.

FUNCTIONAL DESCRIPTION (continued)

6 - CONTROL REGISTER

This section defines the control and device status information. The register programming occurs only during Secondary Frame Synchronization. After a reset condition, the device is always in data mode.

Table 3 : Bits Assignment

Bits	Name	Function	Reset Value
0	-	-	0
1	D1	Aux/Main Input	0
2	D2	Receive Gain	0
3	D3	Oversampling bit 0	0
4	D4	Oversampling bit 1	0
5	D5	Oversampling bit 2	0
6	D6	Attenuator transmit bit 0	0
7	D7	Attenuator transmit bit1	0
8	M	M Divider	1
9	Q0	Q0 Divider	1
10	Q1	Q1 Divider	0
11	Q2	Q2 Divider	0
12	T0	M Divider and Test mode bit 0	0
13	T1	M Divider and Test mode bit 1	0
14	TEST2	Test mode bit 2	0
15	TEST3	Test mode bit 3	0

Table 4 : Aux/Main Input

D1	Function
0	Main Receive Input
1	Auxiliary Receive Input

Table 5 : Receive Gain

D2	Function
DIFFERENTIAL INPUT	
0	0dB gain (commun mode fixed)
1	+6dB gain (commun mode non-fixed)
SINGLE ENDED (one input used, other at V_{CM})	
0	-6dB gain (see Note 1)
1	0dB gain

Note 1 : Not recommended case. Performances could be reduced.

Table 6 : Oversampling Ratio

D5	D4	D3	Function
0	0	0	160
0	0	1	192
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	64
1	1	0	96
1	1	1	128

Table 7 : Transmit Attenuation

D7	D6	Function
0	0	Infinite
0	1	Reserved
1	0	-6dB
1	1	0dB

Table 8 : Q Divider Clock Generator

D11	D10	D9	Function
0	0	0	Q divider = 5
0	0	1	Q divider = 6
0	1	0	Q divider = 7
0	1	1	Q divider = 8
1	0	0	Q divider = 4.5
1	0	1	Q divider = 5.5
1	1	0	Q divider = 6.5
1	1	1	Q divider = 7.5

Table 9 : M Divider Clock Generator

D13	D12	D8	Function
0	0	0	M divider = 3
0	0	1	M divider = 4
0	1	X	Reserved
1	0	X	Reserved
1	1	0	M divider = 1
1	1	1	M divider = 2

Table 10 : Reserved Mode

D15	D14	Function
X	X	Reserved for test

This two bits must be set to 0 for normal operation.

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, Electrical Characteristics are specified over the operating range.
Typical values are given for V_{DD} = 3V, T_{amb} = 25°C and for nominal Master clock frequency MCLK = 1.536MHz and oversampling ratio = 160.

Absolute Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3, 7.0	V
V_I,V_{IN}	Digital or Analog Input Voltage	-0.3, V_{DD}+0.3	V
I_I,I_{IN}	Digital or Analog Input Current	±1	mA
I_O	Digital Output Current	±20	mA
I_{OUT}	Analog Output Current	±10	mA
T_{oper}	Operating Temperature	0, 70	°C
T_{stg}	Storage Temperature	-40, 125	°C
P_{DMAX}	Maximum Power Dissipation	200	mW
ESD	Electrostatic Discharge	2000	V

Nominal DC Characteristics (V_{DD} = 3V ± 5%, GND = 0V, T_A = 0 to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Range	2.70	3	5.5	V
POWER SUPPLY AND COMMON MODE VOLTAGE					
SINGLE POWER SUPPLY (DV_{DD} = AV_{DD})					
I_{DDA}	Analog Supply Current		6		mA
I_{DDD}	Digital Supply Current		4		mA
I_{DD}-LP	Supply Current in Low Power Mode MCLK Stopped MCLK Running		1 200	10	µA µA
V_{CM}	Output Common Mode Voltage V_{CM} Output Voltage Load Current (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V
DIGITAL INTERFACE					
V_{IL}	Low Level Input Voltage	-0.3		0.5	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -600µA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 800µA)			0.3	V
ANALOG INTERFACE					
V_{REF}	Differential Reference Voltage Output V_{REF} = (V_{REFP} - V_{REFN})	1.15	1.25	1.35	V
Tempco (V_{REF})	V_{REF} Temperature Coefficient		200		ppm/°C
$V_{CMO\ IN}$	Input Common Mode Offset Voltage = [(IN+)+(IN-)]/2 -V_{CM}	-100		100	mV
$V_{DIF\ IN}$	Differential Input Voltage : [(IN+)-(IN-)] ≤ 2 x V_{REF}		2 x V_{REF}		Vpp
$V_{OFF\ IN}$	Differential Input DC Offset Voltage	-100		100	mV
$V_{CMO\ OUT}$	Output Common Mode Voltage Offset : (OUT+ + OUT-)/2 - V_{CM} (see Note 1)	-20		20	mV
$V_{DIF\ OUT}$	Differential Output Voltage : OUT+ - OUT- ≤ 2 x V_{REF}		2 x V_{REF}		V
$V_{OFF\ OUT}$	Differential Output DC Offset Voltage : (OUT+ - OUT-) (0000x)	-100		100	mV
R_{IN}	Input Resistance IN+, IN- (id. AUX IN)	100			kΩ
R_{OUT}	Output Resistance (OUT+, OUT-)		50		Ω
R_L	Load Resistance (OUT+, OUT-)	10			kΩ
C_L	Load Capacitance (OUT+, OUT-)			20	pF
$V_{ADO\ OUT}$	Output A/D Modulator Voltage Offset : IN+ = IN- = V_{CM}	-1000		+1000	LSB

Note : 1. Device is very sensitive to noise on V_{CM} Pin. V_{CM} output voltage load current must be DC (<10µA). in order to drive dynamic load, V_{CM} must be buffered. AC variation in V_{CM} current magnitude decrease A/D and D/A performance.

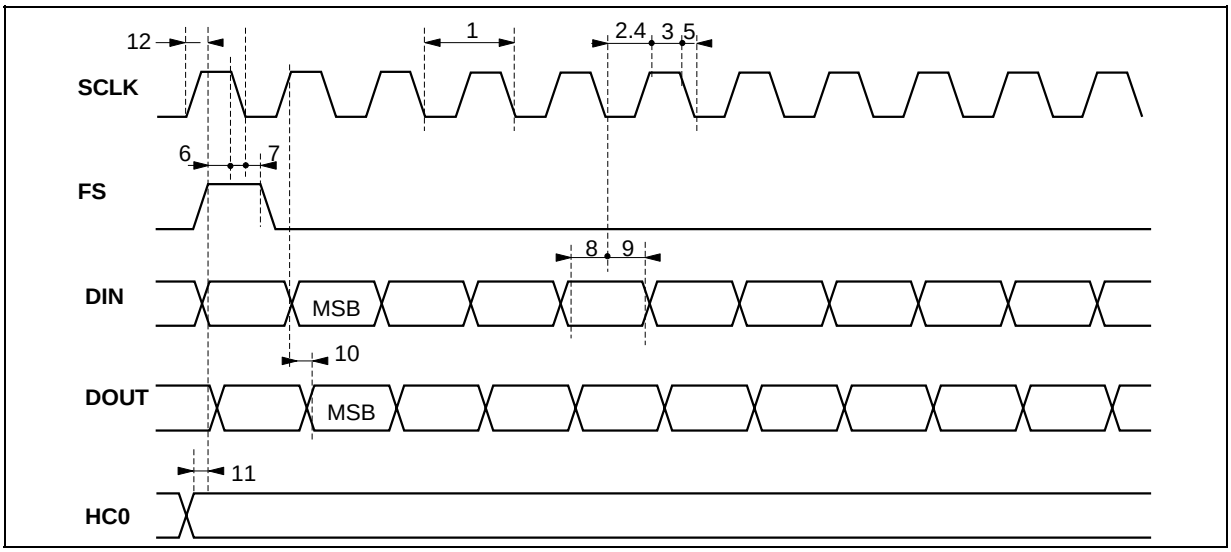
ELECTRICAL SPECIFICATIONS (continued)

Nominal AC Electrical Characteristics

(Reference level V_{IL} = 0.5V, V_{IH} = DV_{DD} - 0.5V, V_{OL} = 0.3V, V_{OH} = DV_{DD} - 0.5V, DV_{DD} = 3V, Output load = 50pF unless otherwise)

Symbol	N°	Parameter	Min.	Typ.	Max.	Unit
SERIAL CHANNEL TIMING (see Figure 9 for Parameter numbers)						
	1	SCLK Period	300			ns
	2	SCLK Width Low	150			ns
	3	SCLK Width High	150			ns
	4	SCLK Rise Time			10	ns
	5	SCLK Fall Time			10	ns
	6	FS Setup	100			ns
	7	FS Hold	100			ns
	8	DIN Setup	50			ns
	9	DIN Hold	0			ns
	10	DOUT Valid			20	ns
	11	HC0,HC1 Set-up	20			ns
	12		0		50	ns
MASTER CLOCK INTERFACE (MCLK) (MCM = 0)						
MCLK		Master Clock Input	0.92	1.54	2.8	MHz
		Master Clock Duty Cycle	45		55	%

Figure 9 : Serial Interface Timing Diagram



ELECTRICAL SPECIFICATIONS (continued)

Transmit Characteristics
Performance of the Tx channel

Typical values are given for AV_{DD} = 3V, T_{amb} = 25°C and for nominal master clock MCLK = 1.536MHz, differential mode and oversampling ratio = 160. Measurement band = 100Hz to 0.425 x Sampling frequency.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Gabs	Absolute Gain at 1kHz	-0.5	0	0.5	dB
Ripple	Ripple in Band : 0 to 0.425 x FS		±0.2		dB
THD	Total Harmonic Distortion (differential Tx signal : V_{OUT} = 1.25V_{PP}, f = 1kHz)	-85	-92		dB
DR	Dynamic Range (f = 1kHz) (measured over the full 0 to FS/2 with a -20dBr output signal and extrapolated to full scale) (see Note 2)		87		dB
CRxTx	Crosstalk (transmit channel to receive channel)		85		dB

Smoothing filter transfer characteristics

The cut-off frequency of the single pole switch-capacitor low-pass filter following the DAC is :

$$fc_{-3dB} = \frac{n \cdot 32 \cdot FS}{2 \cdot \pi \cdot 10}$$ with n = 2, 3, 4, 5, 6 (see paragraph Functional Description 1.2).

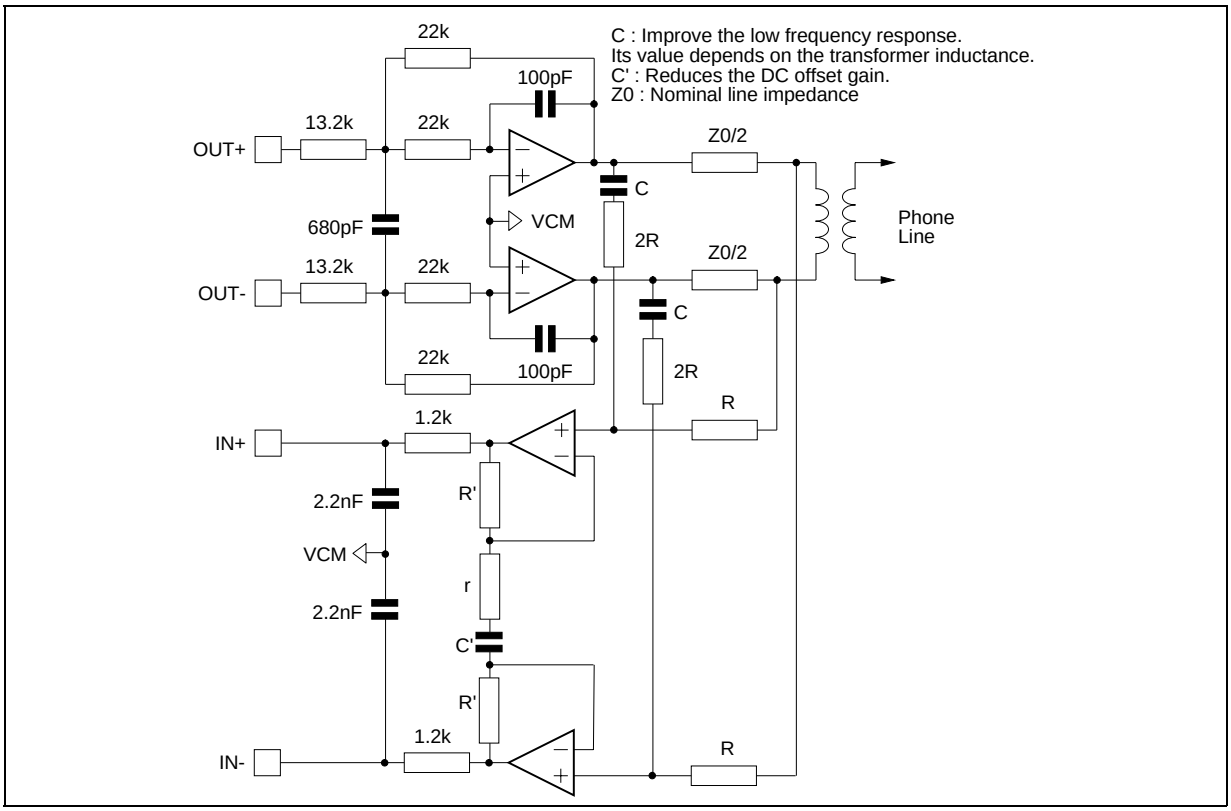
Receive Characteristics
Performance of the Rx channel

Typical values are given for AV_{DD} =3V, T_{amb} = 25°C and for nominal master clock MCLK = 1.536MHz, differential mode and oversampling ratio = 160. Measurement band = 100Hz to 0.425 x Sampling Frequency.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Gabs	Absolute Gain at 1kHz	-0.5	0	0.5	dB
Ripple	Ripple in Band : 0 to 0.425 x FS		±0.2		dB
THD	Total Harmonic Distortion (differential Rx signal : V_{IN} = 1.25V_{PP}, f = 1kHz)		-92		dB
DR	Dynamic Range (f = 1kHz) (measured over the full 0 to FS/2 with a -20dBr input and extrapolated to full scale) (see Note 2)		87		dB
PSRR	Power Supply Rejection Ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CTxRx	Crosstalk (transmit channel to receive channel)		85		dB

Note 2 : The dynamic range can be measured in bit with : $N_{bit} = \frac{DR - 1.76}{6.02}$ with DR in dB.

TYPICAL APPLICATION
Line Interface - Differential Duplexor
Figure 10



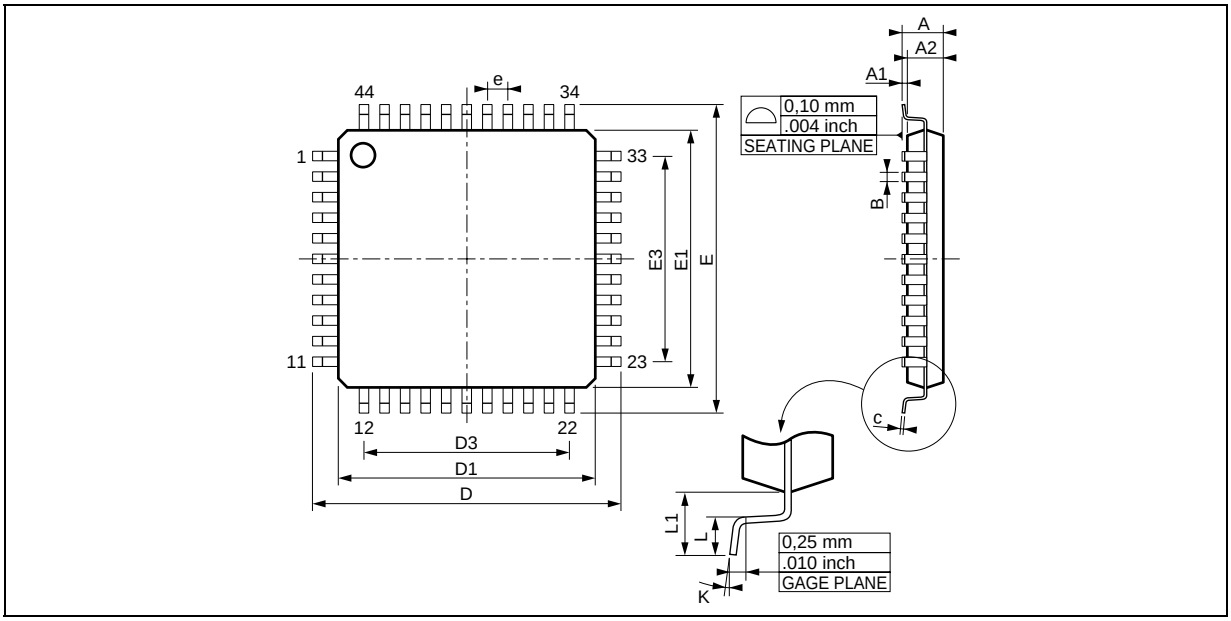
All capacitor, resistor and impedance values are provided for indication only. These values must be readjusted according to line transformer characteristics and also telecommunication regulations in force in individual countries.

Refer to Application Note AN930 for more detailed information. Contact your local representative.

DEFINITION AND TERMINOLOGY

Data Transfer Interval	The time during which data is transfered from D_{OUT} and to D_{IN}. This interval is 16 shift clocks provides by the chip.
Signal Data	This refers to the input signal and all the converted representations through the ADC channel and the DAC channel.
Data Mode	This refers to the data transfer. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Control Mode	This refers to the digital control data transfer into DIN and the register read data from D_{OUT}. The control mode interval occurs when requested by hardware or software.
Frame Sync.	Frame sync refers only to the falling edge of the signal which initiates the data transfer interval. The primary frame sync starts the Data Mode and the secondary frame sync starts the Control Mode.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame sync signals.
ADC Channel	This term refers to all signal processing circuits between the analog input and the digital conversion result at D_{OUT}.
DAC Channel	This term refers to all signal processing circuits between the digital data word applied to D_{IN} and the differential output analog signal available at OUT+ and OUT- pins.
OverSampling Ratio	This term refer to the ratio between the master clock MCLK corresponding to the oversampling frequency and the sampling frequency FS.
Resolution	The number of bits in the input words to the DAC, and the output words in the ADC.
Dynamic Range	The S/(N+D) with a 1kHz, -20dBr input signal and extrapolated to full scale. Use of a small input signal reduces the harmonic distortion components of the noise to insignificance. Units in dB or in N_{bit} as explained before.
Signal-to-(Noise+Distortion)	S/(THD+N) is the ratio of the rms of the input signal to the rms of all other spectral components within the measurement bandwidth (0.425 x Sampling Frequency). Units in dB.
Crosstalk	The amount of 1kHz signal present on the output of the grounded input channel with 1kHz 0dB signal present on the other channel. Units in dB.
Power Supply Rejection Ratio	PSRR. The amount of 1kHz signal present on the output of the grounded input channel with 1kHz 200mV_{PP} signal present on the power supply.

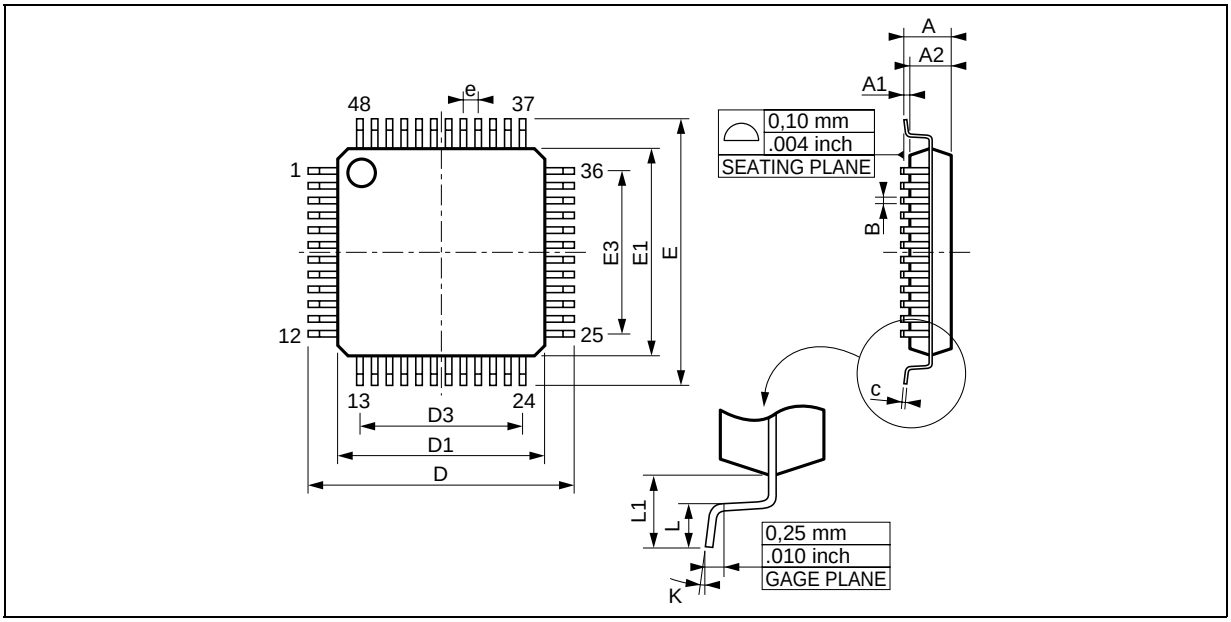
PACKAGE MECHANICAL DATA (continued)
44 PINS - PLASTIC QUAD FLAT PACK (THIN)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.40	0.012	0.015	0.016
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

4Y.TBL

PACKAGE MECHANICAL DATA (continued)
48 PINS - PLASTIC QUAD FLAT PACK (THIN)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

5B.TBL