PRELIMINARY

1/4 DUTY LCD DRIVER WITH KEY SCAN

■ GENERAL DESCRIPTION

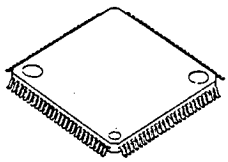
The NJU6436 is a 1/4 duty LCD driver for segment type LCD panel with key scanning, Ir receiving and LED driving function.

The LCD driver consists of 4-common and 60-segment drives up to 240 segments and LED driver drives 1 LED which can use like as power on indicator.

The key scan function scanning up to 30 keys of the 6 x 5 matrix and the Ir receiving function recover the input wave shape. The key scanning data and Ir receiving data are transferred to the MPU serially.

The NJU6436 incorporate all of the function required front panel, therefore it is easy to apply car mounted audio, general audio and other products which have a display and key input on the front panel.

■ PACKAGE OUTLINE

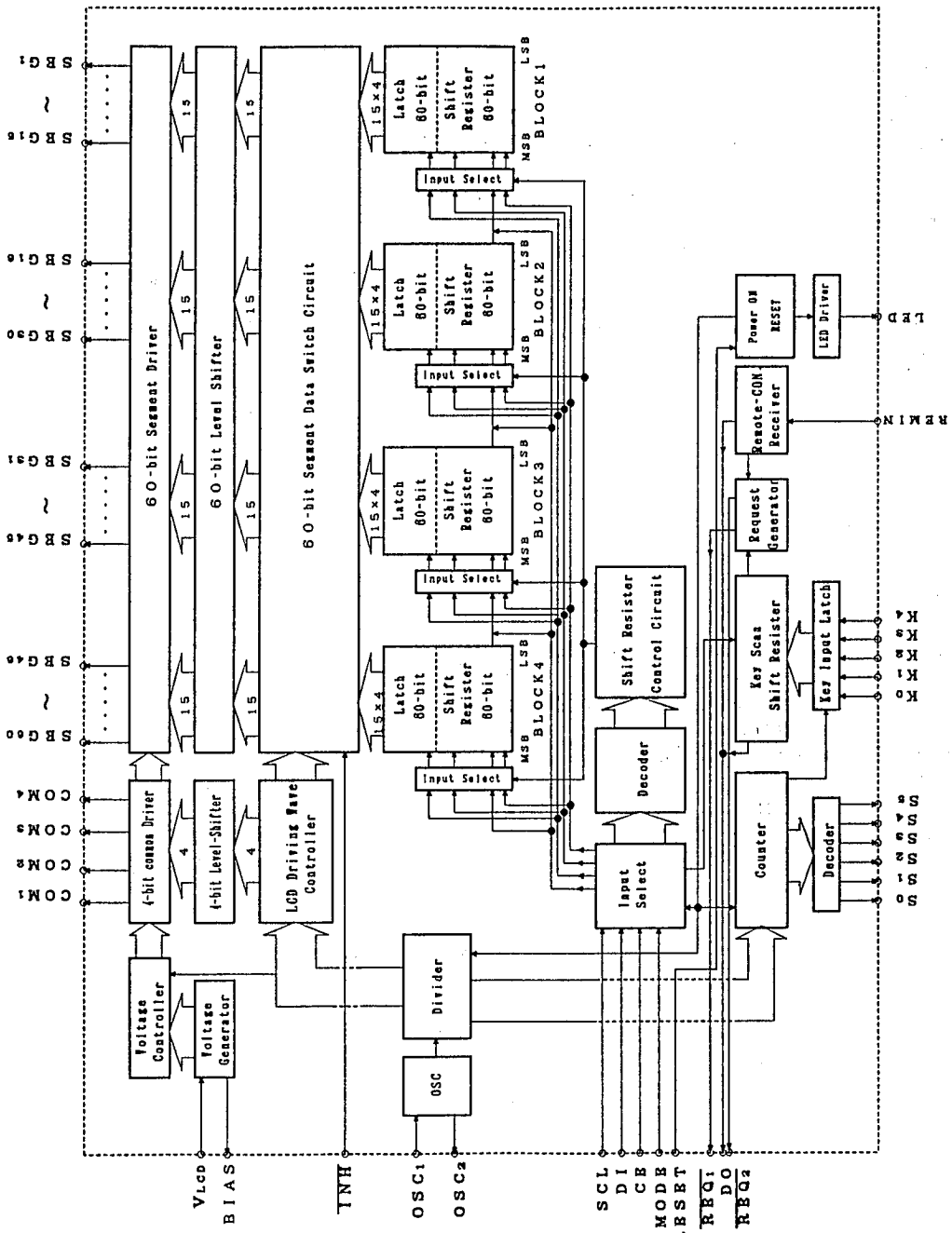


NJU6436F

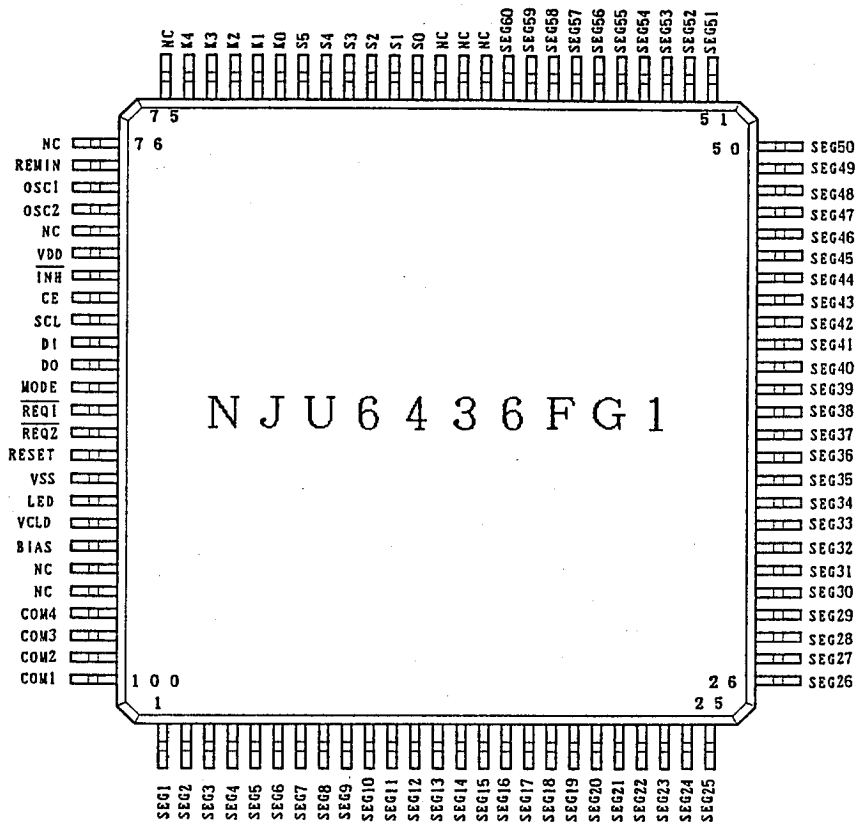
■ FEATURES

- 60-Segment Drivers
- Duty Ratio 1/4 Duty (Up to 240 Segments)
- 30 Key Scan Function (6 x 5 Matrix)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Power-On Initialization
- Display Off Function ($\overline{INH}$ Terminal)
- LED Drive Function
- Ir Receiving Function
- Operating Voltage --- 5V±10%
- Package Outline --- QFP 100
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

NO.	SYMBOL	FUNCTION
1~60	$SEG_1 \sim SEG_{60}$	LCD Segment Output Terminal
64~69	$S_0 \sim S_5$	Key Scanning Signal Output Terminal
70~74	$K_0 \sim K_4$	Key Scanning Input Terminal (Built-in Pull-down Resistance)
77	REMIN	Ir receiver input Terminal Input the Ir receiver output. This terminal must be "L" level when no use.
78, 79	OSC_1 , OSC_2	CR Oscillating Terminal (External R Connecting) For external clock operation, the clock should be input on OSC1.
81	V_{DD}	Power Supply (+5V)
91	V_{SS}	Power Supply (0V)
82	$\overline{INH}$	Display-Off Control Terminal Display is turned off : Display data is retained in the shift-register. "H" : Display-On "L" : Display-Off
83	CE	Chip Enable Terminal "H" : LCD display data Input , Mode setting code Input "L" : Key data output mode Fall Edge : LCD display data Latch , Mode setting code Latch
84	SCL	Serial Data Transmission Clock Terminal Shift clock used for transferring display data and mode setting code to internal shift register, and used as Key data output shift clock.
85	DI	Serial Data Input Terminal Data input timing : Rise edge of SCL clock
86	DO	Serial Data Output Terminal Key data and Ir input-data output. Data output timing : Rise edge of SCL clock
87	MODE	Select the Display Data or Mode Setting code Terminal "H" : Mode setting code input "L" : LCD Display data input
88	$\overline{REQ_1}$	Request Signal Output Terminal (Key Data Read Request)
89	$\overline{REQ_2}$	Request Signal Output Terminal (Ir Receiver Data Read Request)
90	RESET	Reset Terminal (Built-in Pull-down Resistance) "H" : Reset operation (Shift-register all clear, key scan circuit initialize) "L" or OPEN : Normal operation
92	LED	LED Direct driving Terminal Turns on during the NJU6436 is turned on except reset period. LED On : "L" output LED Off : Hi-impedance
93	V_{LCD}	Power Supply for LCD Driving
94	BIAS	Adjusting Terminal for output current of Voltage Follower
97~100	$COM_4 \sim COM_1$	LCD Common Output Terminal
61~63, 75,76,80,95,96	NC	Non Connection (Normally open)

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■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

Oscillation by connecting external resistance.
This circuits supply the basical clock signal to other circuits like as common and segment driver and key scan circuits.

(1-2) Divider Circuit

This circuit divide the oscillator frequency and generate the common and segment output timing signals.

(1-3) Input Control Circuit

This circuit select the LCD display data and mode setting code according to the condition of MODE terminal.

(1-4) Shift-Register Circuit(60-bit) and Latch Circuit(60-bit)

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.
The CE terminal signal latches the display data at the falling edge.

(1-5) Segment Data switch Circuit and Segment Driver

Set the segment display data according to the common timing and output through level shifter and output buffer.

(1-6) Level Shifter Circuit

Logic driving voltage is converted to LCD driving voltage.

(1-7) LCD Common Driver

Output the common driving signal for LCD.

(1-8) LCD Bias Level Generator

This circuit generate the LCD bias voltage.

(1-9) Key Scan Counter

This circuits generate key scanning timing. When the key input, the data in the counter is transferd to the key scan shift register.

(1-10) Key Scan Decoder

Decoding the counter output and generate the key scanning signal.

(1-11) Key Input Latch

Latch the key input data.
This circuit detect two times same key input for a chatter free operation.

(1-12) Key Scan Shift Register

Output the data sent from counter and key input latch data to the MPU serially through the DO terminal.

(1-13) Request Signal Generator Circuit

When detect some key input by the key scanning, this circuits output the "L" level signal to the controller as a "read out request signal"($\overline{REQ_1}$).
The "L" level output of $\overline{REQ_1}$ is released when the key scan control code send the "End of read out".
When the data input from the REMIN, the "read out request signal" $\overline{REQ_2}$ is output "L" level as a "read out request signal" by synchronizing the rise edge of the input data.
It is also released when the mode setting code send the "End of read out".

(1-14) LED Driving Circuit

The LED connected between LED terminal and V_{DD} terminal is turned on during the power turns on of the NJU6436 except reset period.

(2) Data Input Format

• Two kind of data is input to the NJU6436.
① Mode Setting Data
② LCD Display Data

Normally, the shift register control code of mode setting and the display data are pare always. First, setting the transferred register by the shift register control code, Second, input the display data. Start the key scan, Stop the key scan and key data output are controlled by the key scan control code .
All of display data and mode setting data are input synchronized by the rise edge of the clock signal.

• Two kind of data is output from the NJU6436.
③ Key Data
④ Output signal of Ir Receiver

Key data outputs the key matrix scan data.
Key scan is stopped when power is supplied, reset signal is input to the reset terminal and software reset operation is executed. The key scan starts when the key input status change or "key scan start mode" of the key scan control code is input.

Key scan operation is stoped by either of the "key scan stop mode" of key scan control code, and reset signal inputs to the reset terminal.

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After the key scan operation, the NJU6436 output the data read out request signal($\overline{REQ_1}$) to the controller.
Then the " key data output mode" of key scan control code is input to the NJU6436, the input key data is transferred to the transfer register and output to the data output terminal "DO" by synchronizing with rise edge of shift clock. (key data is 8 bit format.)
Key data read out signal($\overline{REQ_1}$) is released by the "End of read out" of key scan control code input to the NJU6436.

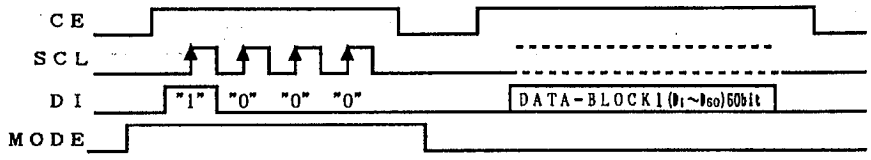
Ir receiver output data input from the Ir receiver input terminal "REMIN" output to the data output terminal "DO" through internal buffer.
The NJU6436 output the read out request signal ($\overline{REQ_2}$="L") by synchronize with the rise edge of the data. The read out request signal of ($\overline{REQ_2}$) is released by the "End of read out" mode input same as key data read out.

(2-1)Input Data Correspond to Segment Status

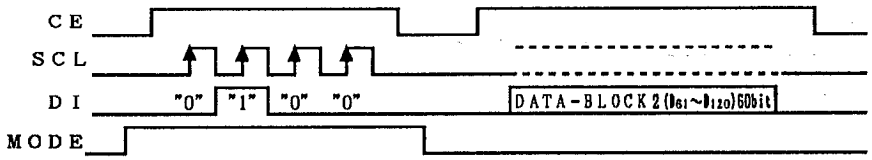
Data Dxxx	Segment Status
"H"	ON
"L"	OFF

(2-2)Write to Shift-register Example

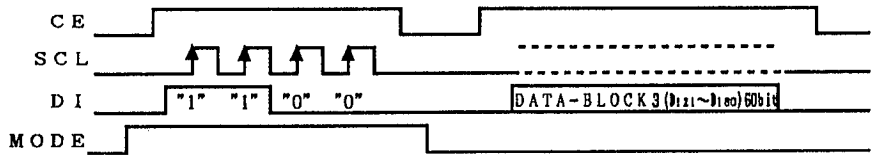
Example 1(Code 1): Write to Shift-register 1(1 to 60-bit)



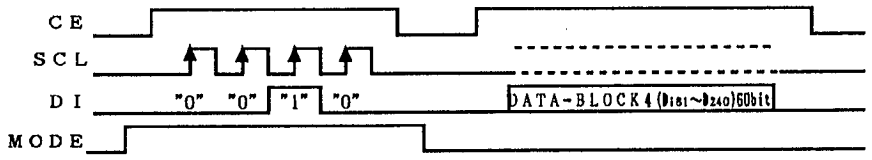
Example 2(Code 2): Write to Shift-register 2(61 to 120-bit)



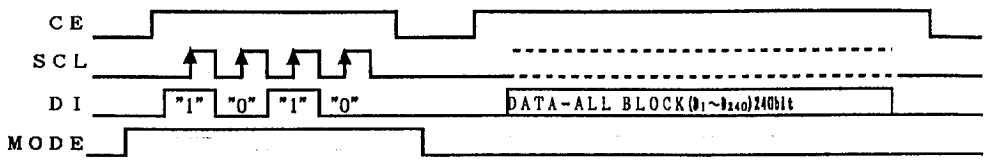
Example 3(Code 3): Write to Shift-register 3(121 to 180-bit)



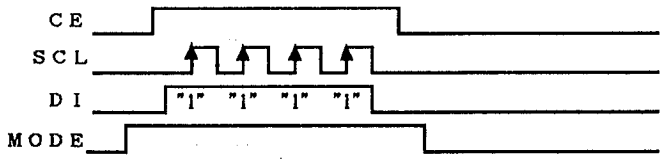
Example 4(Code 4): Write to Shift-register 4(181 to 240-bit)



Example 5(Code 5): Write to Shift-register 5(1 to 240-bit)



Example 6(Code F): Soft-Reset



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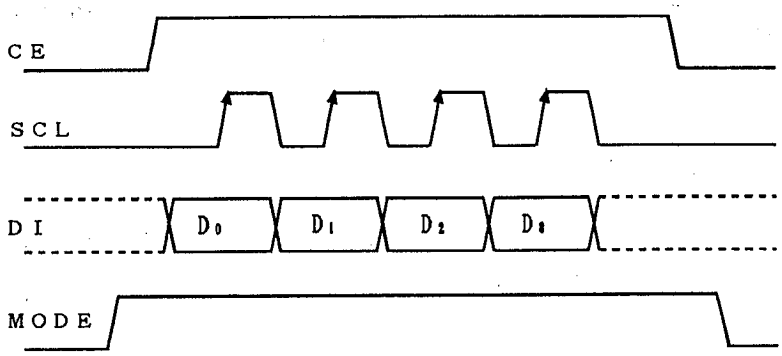
(2-3)Mode Set Up

Data transferred shift register selection, key scan control and software reset are performed by writing the 4 bit data to the NJU6436 in CE="H" and MODE="H" state.

< Input Timing Chart >



< Mode Setting Table >

CE Term.	MODE Term.	Mode setting code	D3~D0	Mode Set Up
"H"	"H"		0000 (0)	End of Read out (Key data and Ir receiver output data) Release the read out request and start the key scan.
		Shift-register control code	0001 (1)	Select the shift-register BLOCK1
			0010 (2)	Select the shift-register BLOCK2
			0011 (3)	Select the shift-register BLOCK3
			0100 (4)	Select the shift-register BLOCK4
			0101 (5)	Select the all shift-register (BLOCK1~4)
			0110 (6)	NO OPERATION
			0111 (7)	NO OPERATION
		Key scan control code	1000 (8)	Key data output Key data set into the transfer register and prepare the key data transmit.
			1001 (9)	Key scan start Key scan start from the halt state.
			1010 (A)	Key scan stop and key data output Newly key input data set into the transfer register and stop the key scan. Note;Read out request signal is not released
			1011 (B)	Key scan initialize Stop the key scan and release the read out request signal.
			1100 (C)	NO OPERATION
			1101 (D)	NO OPERATION
			1110 (E)	NO OPERATION
			1111 (F)	Software reset ・Shift-register all clear (data="0") ・Key scan initialize

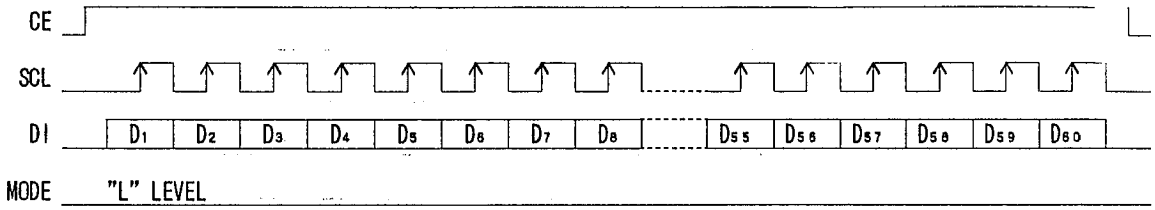
Note) The decoder is 4 bit format data through type. Though 8 bit data is also available to input at the mode setting, in that time front 4 bit is valid from the fall edge of CE signal.

(2-4)Block Data and Whole Data transfer

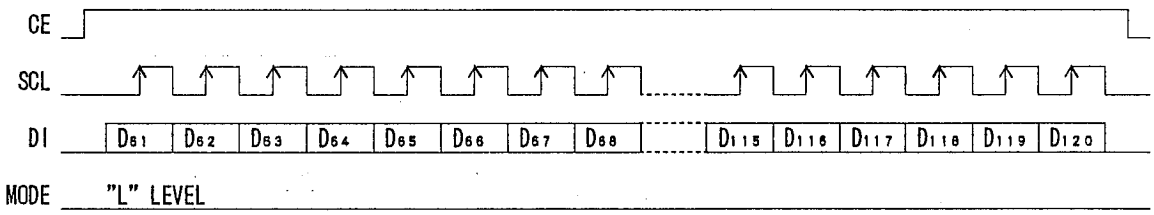
a. Block Data(60-bit) transfer

Each 60 bits data transfer to each shift register block 1 to 4 respectively.
When the input data is over than 60 bit, front 60 bit from fall edge of "CE" signal is valid.
In case of the input data is less than 60 bit, the previous data is remaining on the register.
So that 60 or over than 60 bit data input must be required.

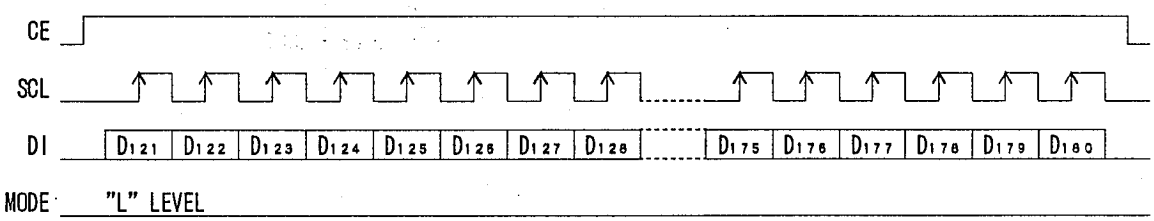
Data Block 1 : from SEG_1, COM_1 to SEG_{15}, COM_4



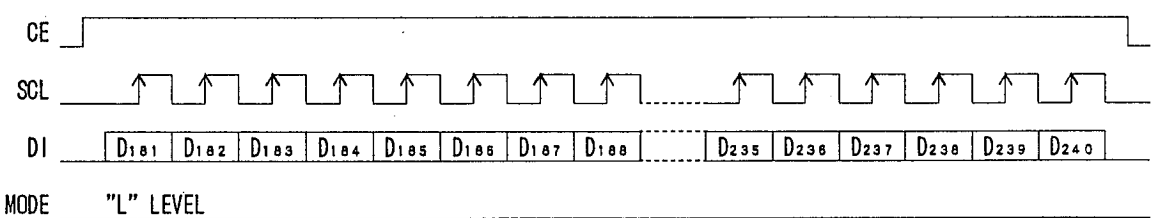
Data Block 2 : from SEG_{16}, COM_1 to SEG_{30}, COM_4



Data Block 3 : from SEG_{31}, COM_1 to SEG_{45}, COM_4



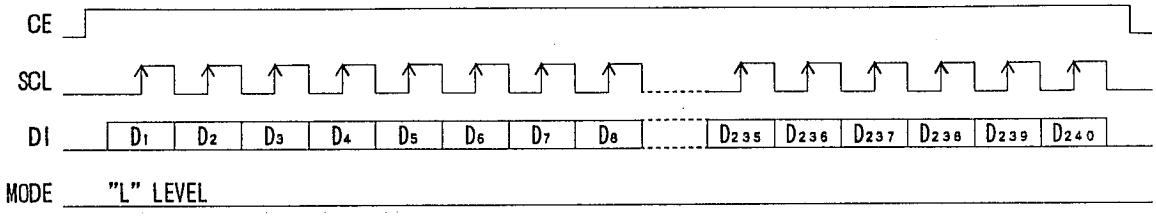
Data Block 4 : from SEG_{46}, COM_1 to SEG_{60}, COM_4



b. Whole Data(240-bit) transfer

Whole 240 bits data transfer to the shift register block 1 to 4 once a time.
When the input data is over than 240 bit, front 240 bit from fall edge of "CE" signal is valid.
In case of the input data is less than 240 bit, the previous data is remaining on the register.
So that 240 or over than 240 bit data input must be required.

from shift-register 1 to shift-register 4



(2-5) Display Data Correspond to Segment and Common Terminals

Mode	Data	Segment	COM_1	COM_2	COM_3	COM_4	Data Block
Mode 1	D_1 D_2 D_3 D_4	SEG_1	○	○	○	○	Data Block 1
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{57} D_{58} D_{59} D_{60}	SEG_{15}	○	○	○	○	
Mode 2	D_{61} D_{62} D_{63} D_{64}	SEG_{16}	○	○	○	○	Data Block 2
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{117} D_{118} D_{119} D_{120}	SEG_{30}	○	○	○	○	
Mode 3	D_{121} D_{122} D_{123} D_{124}	SEG_{31}	○	○	○	○	Data Block 3
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{177} D_{178} D_{179} D_{180}	SEG_{45}	○	○	○	○	
Mode 4	D_{181} D_{182} D_{183} D_{184}	SEG_{46}	○	○	○	○	Data Block 4
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{237} D_{238} D_{239} D_{240}	SEG_{60}	○	○	○	○	

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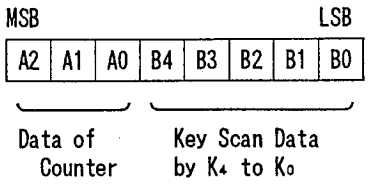
(3) Key Input Data Output Format

(3-1) Data Format



Key Scan Signal Correspond to Counter Data is as follows:

Terminal	Key Scan Signal	Counter Data A2	A1	A0
S_0		0	0	0
S_1		0	0	1
S_2		0	1	0
S_3		0	1	1
S_4		1	0	0
S_5		1	0	1
		Divide	Cycle	Frequency
Search Pulse Width	→←1024/fosc≒7.88mSec	$\frac{1}{1024}$	7.88mS	———
Key Scan One cycle	←—6144/fosc—→ ≒47.26mSec	$\frac{1}{6144}$	47.26 mS	21.15 Hz
Key Read MIN. Time	←———12288/fosc≒94.52mSec———→	$\frac{1}{12288}$	94.52 mS	10.58 Hz

(f osc=130kHz)

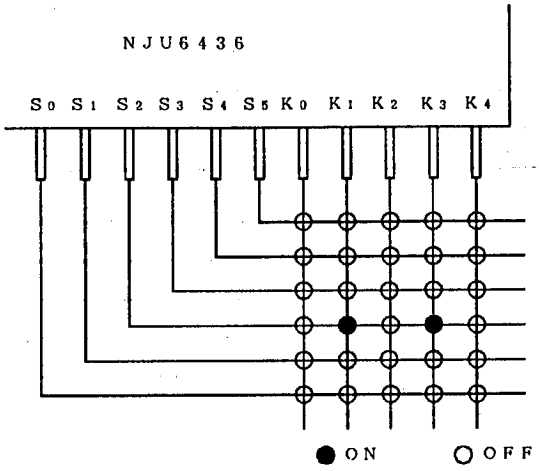
Less than 47.26mSec key input is neglected due to the two times key input for the chatter free operation.

The 5 bit data of B4 to B0 correspond to the key input terminal K4 to K0, when some key is pressed the data "1" correspond to the key input line, input to the register.

The data of A2 to A0 and B4 to B0 indicate the key data input.

(3-2) Key Roll Over Input.

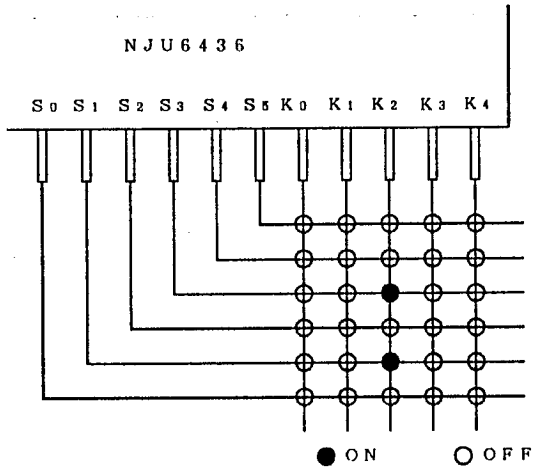
・When the roll over input occur, following data are input.
< Roll over on same Sx line >



When two key connected K1 and K3 pressed at once, the data "1" input to the B3 and B1.

MSB							LSB
0	1	0	0	1	0	1	0
A2	A1	A0	B4	B3	B2	B1	B0

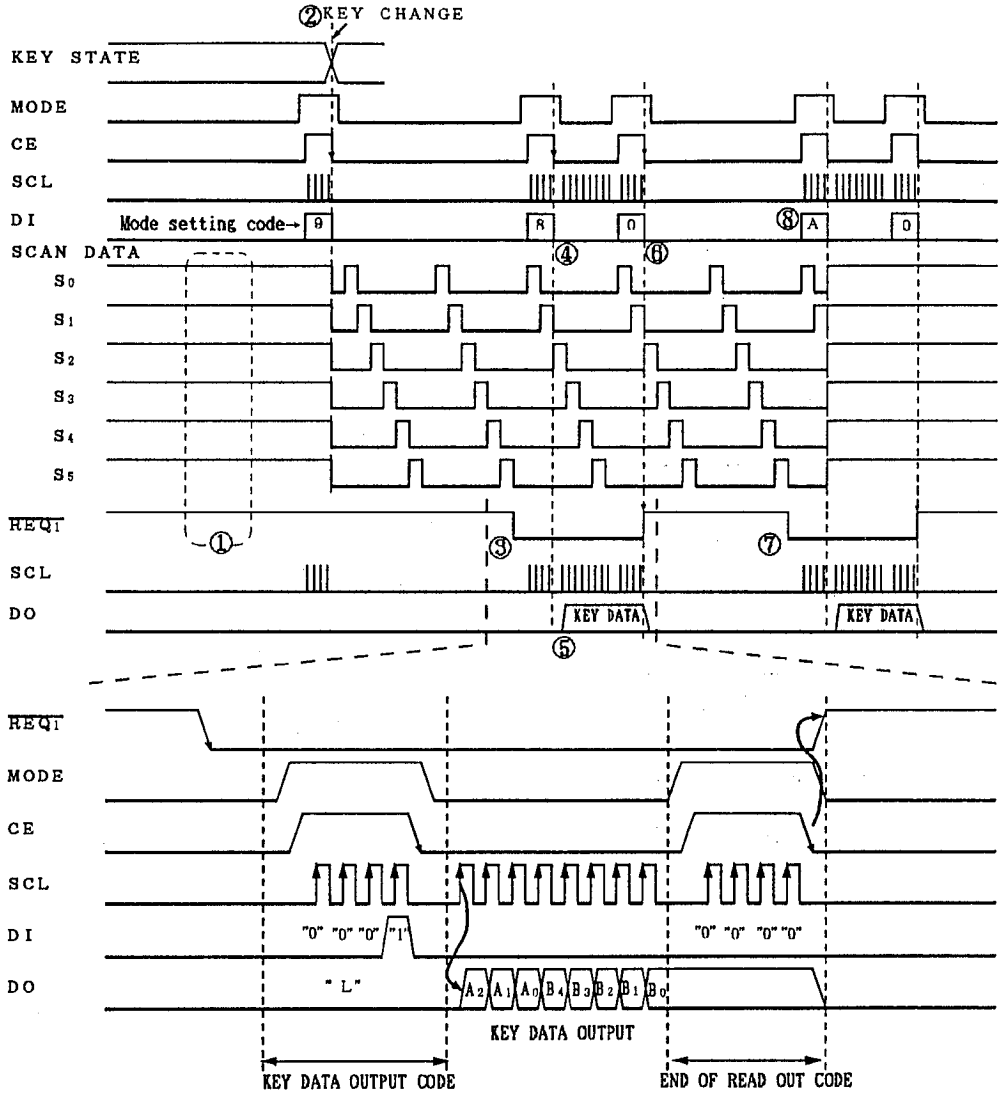
・Permit the following roll over.
< Roll over on same Kx line >
In this case, there are following priority.
$S_5 > S_4 > S_3 > S_2 > S_1 > S_0$
If this kind of roll over occur, the low priority input is ignore.



In case of above input, the key input of S1 is ignored.

MSB							LSB
0	1	1	0	0	1	0	0
A2	A1	A0	B4	B3	B2	B1	B0

(3-3) Key Scan Timing Chart



【 Operation Explanation 】

① Before key scanning, all of Sx terminal output the "H" to detect the some key input.

② Key scan operation start when recognize the key input or setting the key scan.
Note) The key input is detected by Kx input level, so the change of key input of same Kx line roll over can not recognize.

③ When key input, the NJU6436 output the read out request signal to the controller ($\overline{REQ_1}$="L"). In this time, the "DO" output change to the key data output terminal.

④ When key data output is setting by the mode selection, the input key data transferred to the transfer register.

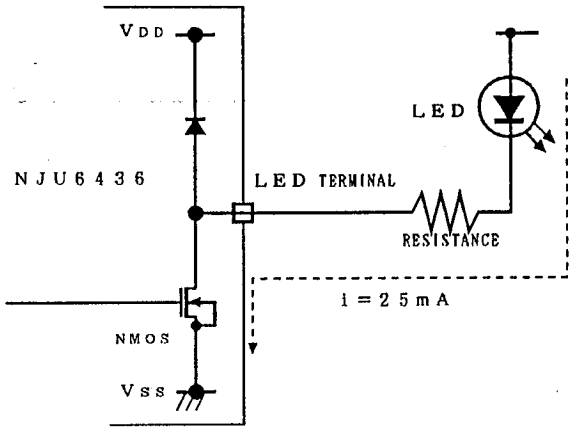
⑤ Key data of 8 bit output by synchronize with the rise edge of clock signal after the mode setting.

⑥~⑦ Select the end of read out by the mode setting, the key scan register reset then start the key scan again.

⑧ "Key scan stop and key data output" or "key scan initialize" key scan stop is selected by the key scan control code input. In this time, the key scan is stopped and all of S_0 to S_5 put on "H".

(4) LED Driving Circuit

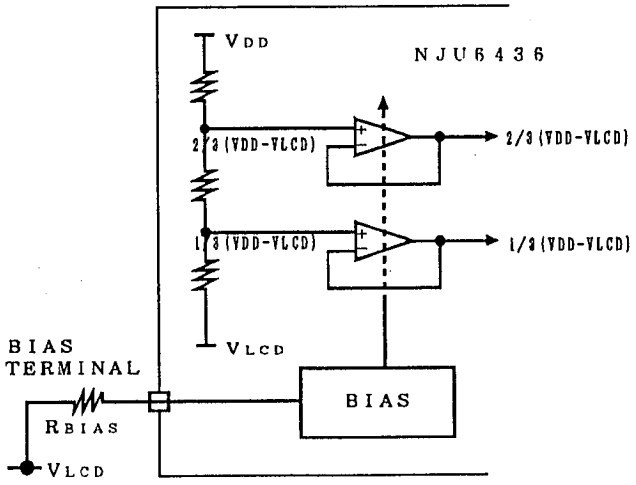
Connecting the LED between LED terminal and V_{DD} terminal, the LED turns on during the power of NJU6436 turns on except reset period.



Operating voltage current can adjust by insert the protection resistor between LED and LED terminal.

Note) Protection resistor must be connect to the LED to avoid over than the maximum ratings of voltage and current between Anode and Cathode of the LED. No protection resistor may occur the damage of LED output buffer and LED.

(5) LCD Driving Voltage / Bias current Adjustment Terminal



Power block is consist of 3 blocks of bias, bleeder and buffer amplifire as show above.

The output current of buffer amplifire can adjust by changing the current flow on bias circuit which controlled by external resistance connected to the BIAS terminal.

■ ABSOLUTE MAXIMUM RATINGS (V_{SS}=0V, Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage (1)	V_{DD}	- 0.3 ～ + 7.0	V
Operating Voltage (2)	V_{LCD}	V_{DD}-13.5 ～ V_{DD}+0.3	V
Input Voltage	V_{IN} (1)	- 0.3 ～ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ～ + 85	℃
Storage Temperature	Tstg	- 40 ～ + 125	℃

Note 1) All Input Terminals

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■ ELECTRICAL CHARACTERISTICS

• DC Characteristics ($Ta=25℃, V_{DD}=5.0V, V_{SS}=0V, V_{DD}\sim V_{LCD}=13.5V$)

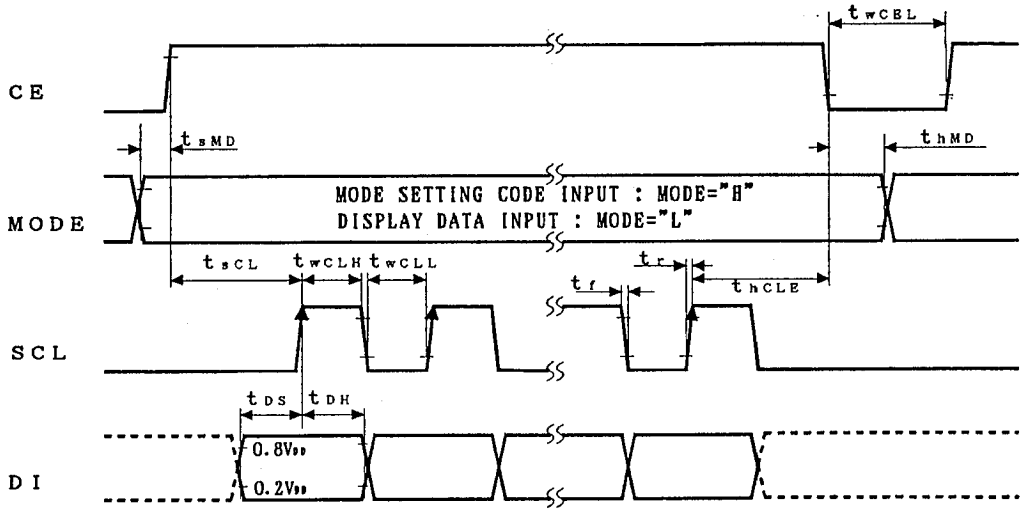
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}	V_{DD} Terminal	4.5	5.0	5.5	V
LCD driving Voltage	V_{LCD}	V_{LCD} Terminal	V_{DD}-13.5		V_{SS}	V
"H" Input Voltage	V_{IH}	RESET,SCL,DI,CE,REMIN, $\overline{INH}$,$K_0\sim K_4$,MODE Terminals	$0.8V_{DD}$		V_{DD}	V
"L" Input Voltage	V_{IL}	RESET,SCL,DI,CE,REMIN, $\overline{INH}$,$K_0\sim K_4$,MODE Terminals	V_{SS}		$0.2V_{DD}$	V
"H" Input Current	I_{IH}	SCL,DI,CE,REMIN,MODE, $\overline{INH}$ Terminals $VI=V_{DD}$			5	μA
"L" Input Current	I_{IL}	RESET,SCL,DI,CE,REMIN, $\overline{INH}$,$K_0\sim K_4$,MODE Terminals $VI=V_{SS}$			5	μA
"H" Output Voltage (1)	$V_{OH(1)}$	I_{OH}=-10μA $SEG_1\sim SEG_{60}$ Terminals	VDD-1.0			V
"H" Output Voltage (2)	$V_{OH(2)}$	I_{OH}=-100μA $COM_1\sim COM_4$ Terminals	VDD-0.6			V
"H" Output Voltage (3)	$V_{OH(3)}$	I_{OH}=-40μA $S_0\sim S_5$, DO, $\overline{REQ_1}$, $\overline{REQ_2}$ Terminals	VDD-0.8			V
"L" Output Voltage (1)	$V_{OL(1)}$	I_{OL}=10μA $SEG_1\sim SEG_{60}$ Terminals			V_{LCD}+1.0	V
"L" Output Voltage (2)	$V_{OL(2)}$	I_{OL}=100μA $COM_1\sim COM_4$ Terminals			V_{LCD}+0.6	V
"L" Output Voltage (3)	$V_{OL(3)}$	I_{OL}=400μA $S_0\sim S_5$, DO, $\overline{REQ_1}$, $\overline{REQ_2}$ Terminals			0.8	V
"L" Output Voltage (4)	$V_{OL(4)}$	I_{OL}=25mA LED Terminal			1.5	V
COM 1/3 Level Voltage	$V_{MC1/3}$	I_O=±5μA $COM_1\sim COM_4$ Terminals	$1\cdot(V_{DD}-V_{LCD})/3-0.6$	$1\cdot(V_{DD}-V_{LCD})/3$	$1\cdot(V_{DD}-V_{LCD})/3+0.6$	V
COM 2/3 Level Voltage	$V_{MC2/3}$	I_O=±5μA $COM_1\sim COM_4$ Terminals	$2\cdot(V_{DD}-V_{LCD})/3-0.6$	$2\cdot(V_{DD}-V_{LCD})/3$	$2\cdot(V_{DD}-V_{LCD})/3+0.6$	V
SEG 1/3 Level Voltage	$V_{MS1/3}$	I_O=±5μA $SEG_1\sim SEG_{60}$ Terminals	$1\cdot(V_{DD}-V_{LCD})/3-1.0$	$1\cdot(V_{DD}-V_{LCD})/3$	$1\cdot(V_{DD}-V_{LCD})/3+1.0$	V
SEG 2/3 Level Voltage	$V_{MS2/3}$	I_O=±5μA $SEG_1\sim SEG_{60}$ Terminals	$2\cdot(V_{DD}-V_{LCD})/3-1.0$	$2\cdot(V_{DD}-V_{LCD})/3$	$2\cdot(V_{DD}-V_{LCD})/3+1.0$	V
Oscillation Frequency	f_{osc}	OSC_1,OSC_2 Terminals R=1MΩ	15	20	25	kHz
		R=140KΩ	110	130	150	kHZ
		R=51KΩ	200	300	400	kHz
Operating Current (1)	I_{SS}	V_{SS} Terminal Except LCD output f_{OSC}=130kHz, C_L=50PF RESET,LED,$K_0\sim K_4$ Terminals Open Key-Scan No-Operation		50	100	μA
Operating Current (2)	I_{LCD}	V_{LCD} Terminal LCD output no-load f_{OSC}=130kHz RESET,LED,BIAS,$K_0\sim K_4$ Terminals Open		50	100	μA
Pull-Down Resistance Current	I_P	$K_0\sim K_4$,RESET Terminals $V_{IN}=V_{DD}$		10	20	μA

• AC Characteristics (Ta=25℃, V_{DD}=5.0V, V_{SS}=0V, V_{DD}~V_{LCD}=13.5V)

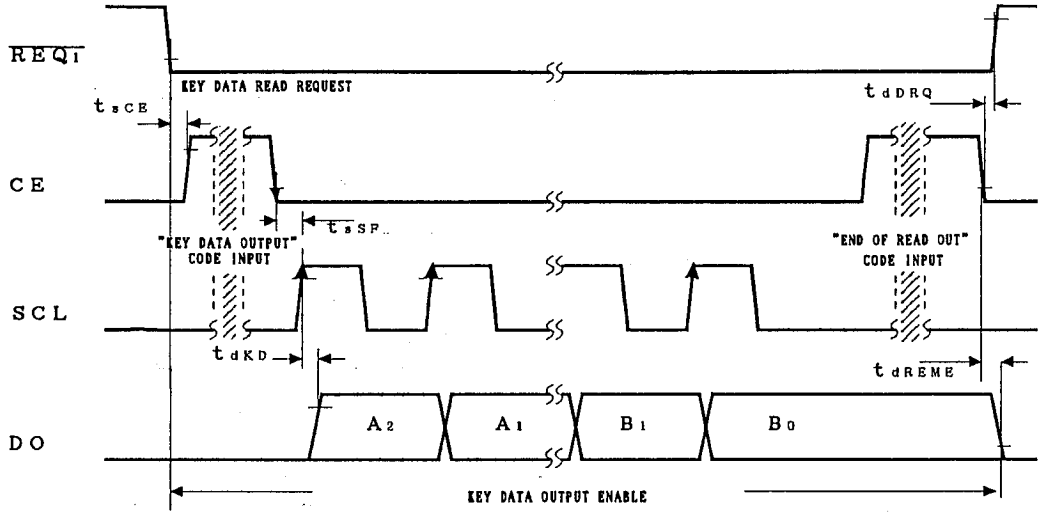
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{wCLL}	SCL Terminal	200			ns
"H" Clock Pulse Width	t_{wCLH}	SCL Terminal	200			ns
Data Set-up Time	t_{DS}	SCL,DI Terminals	200			ns
Data Hold Time	t_{DH}	SCL,DI Terminals	200			ns
CE→SCL Set-up Time	t_{sCL}	SCL,CE Terminals	200			ns
SCL→CE Hold Time	t_{hCLE}	SCL,CE Terminals	200			ns
MODE→CE Set-up Time	t_{sMD}	CE, MODE Terminals	200			ns
CE→MODE Hold Time	t_{hMD}	CE, MODE Terminals	200			ns
CE "L" Pulse Width	t_{wCEL}	CE Terminal	200			ns
$\overline{REQ_1}$→CE Set-up Time	t_{sCE}	$\overline{REQ_1}$,CE Terminals	200			ns
CE→SCL Set-up Time	t_{sSF}	CE,SCL Terminals	200			ns
Data Output Delay Time (1)	t_{dKD}	SCL,DO Terminals DO Load = 50PF			120	ns
CE→$\overline{REQ_1}$,$\overline{REQ_2}$ Delay Time	t_{dDRQ}	CE,$\overline{REQ_1}$,$\overline{REQ_2}$ Terminals $\overline{REQ_1}$,$\overline{REQ_2}$ Load = 50PF			120	ns
REMIN "L" Pulse Width	t_{wREML}	REMIN Terminal	200			ns
REMIN "H" Pulse Width	t_{wREMH}	REMIN Terminal	200			ns
Data Output Delay Time (2)	t_{dREM}	REMIN,DO Terminals DO Load = 50PF			120	ns
REMIN→$\overline{REQ_2}$ Delay Time	t_{dRMRQ}	REMIN,$\overline{REQ_2}$ Terminals DO Load = 50PF			120	ns

5

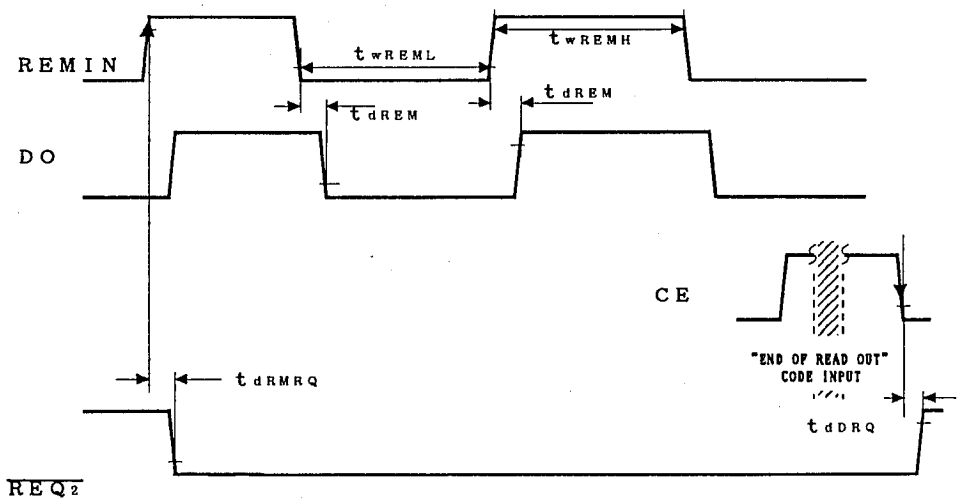
• Display Data Input / Mode Setting code input Timing Characteristics



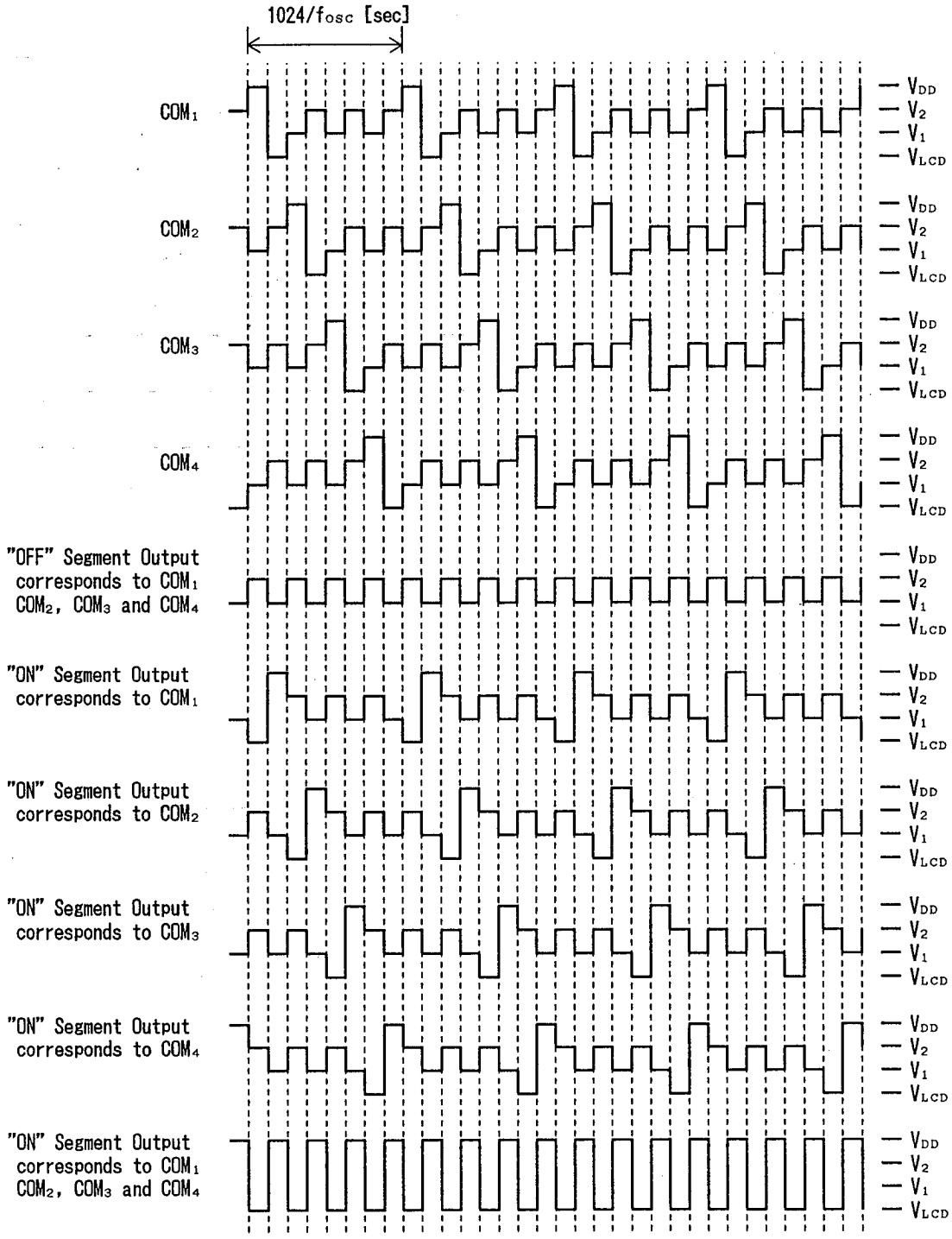
・ Key Data Output Timing Characteristics



・ REMIN Input Data and DO Output Data Timing Characteristics

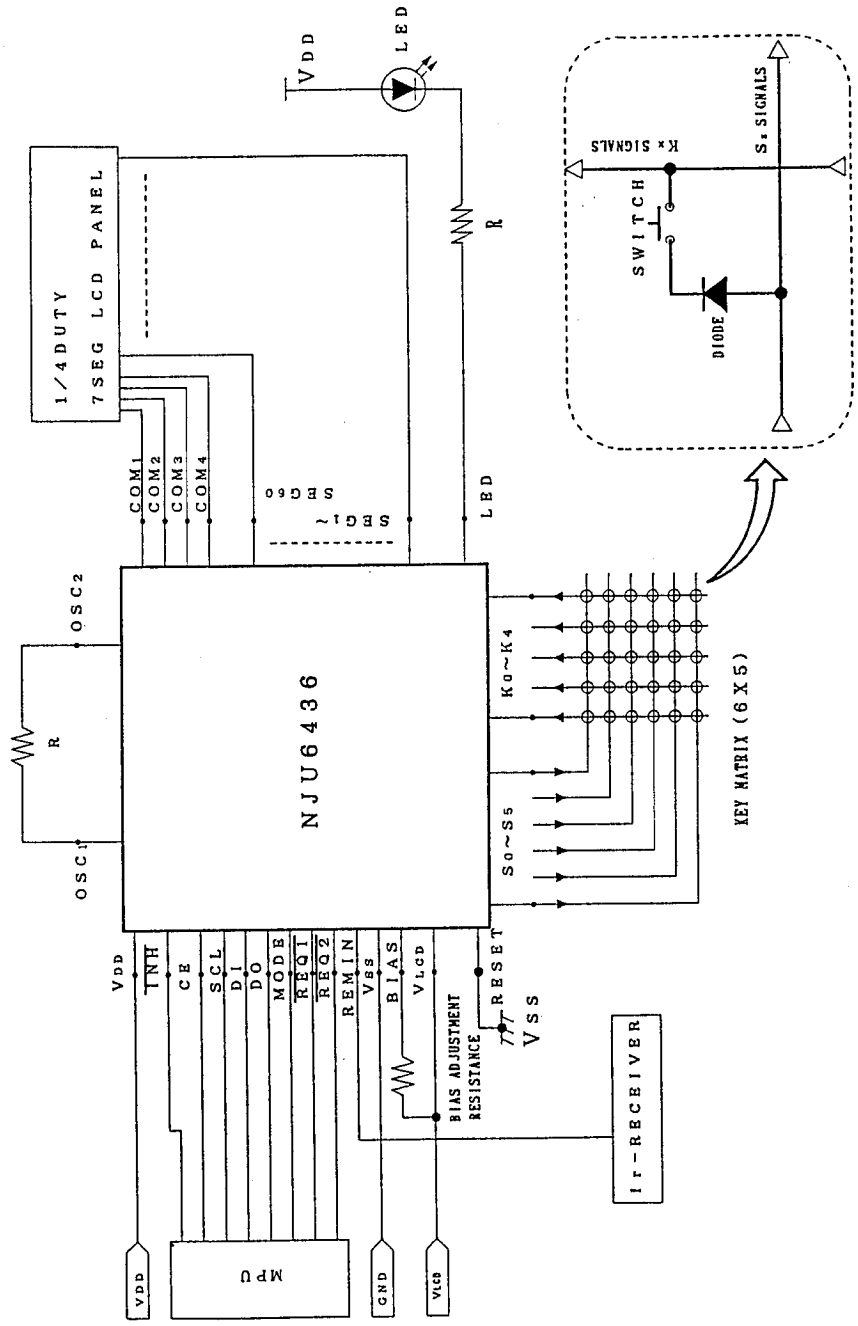


■ LCD Driving Waveform (1/4DUTY・1/3BIAS)



※ $V_1=1/3\cdot|V_{DD}-V_{LCD}|$、$V_2=2/3\cdot|V_{DD}-V_{LCD}|$

■ APPLICATION CIRCUITS



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