M5M5V208AKV/KR

PRELIMINARY

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Some parametric limits are subject to change

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V208A is a family of low voltage 2-Mbit static RAMs organized as 262,144-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5V208A is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

The M5M5V208A is packaged in 32-pin 8mm x 13.4mm STSOP packages. Two types of STSOPs are available, M5M5V208AKV (normal-lead-bend STSOP) and M5M5V208AKR (reverse-lead-bend STSOP). These two types STSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

FEATURES

- Single 2.7 ~ 3.6V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by $\overline{S1}$ & S2
- Data retention supply voltage=2.0V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current ••••••••••• 0.3µA(typ.)

PACKAGE

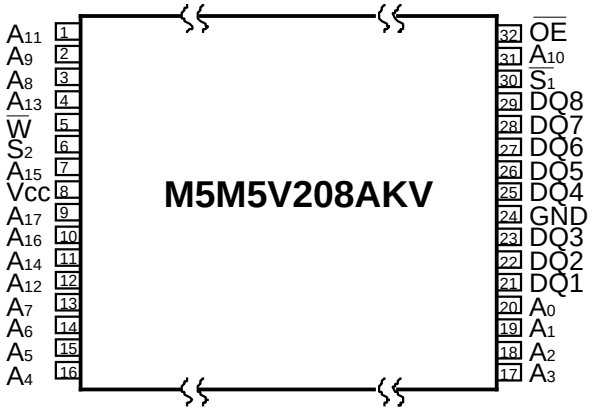
M5M5V208AKV,KR : 32pin 8 X 13.4 mm TSOP

PART NAME TABLE

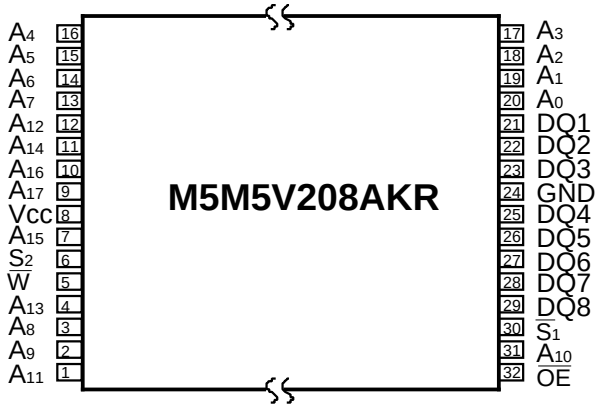
Version, Operating temperature	Part name (## stands for"KV"or"KR")	Power Supply	Access time max.	Stand-by current Icc(PD), Vcc=3.0V typical * 25°C	typical * 40°C	Ratings (max.) 25°C	Ratings (max.) 40°C	Ratings (max.) 70°C	Ratings (max.) 85°C	Active current Icc1 (3.0V, typ.)
Standard 0 ~ +70°C	M5M5V208A## -55L	2.7 ~ 3.6V	55ns	---	---	---	---	20µA	---	20mA (f=10MHz)
	M5M5V208A## -70L		70ns							
	M5M5V208A## -55H	2.7 ~ 3.6V	55ns	0.3µA	---	1µA	3µA	8µA	---	
	M5M5V208A## -70H		70ns							
W-version -20 ~ +85°C	M5M5V208A## -55LW	2.7 ~ 3.6V	55ns	---	---	---	---	20µA	50µA	
	M5M5V208A## -70LW		70ns							
	M5M5V208A## -55HW	2.7 ~ 3.6V	55ns	0.3µA	---	1µA	3µA	8µA	24µA	3mA (f=1MHz)
	M5M5V208A## -70HW		70ns							
I-version -40 ~ +85°C	M5M5V208A## -55LI	2.7 ~ 3.6V	55ns	---	---	---	---	20µA	50µA	
	M5M5V208A## -70LI		70ns							
	M5M5V208A## -55HI	2.7 ~ 3.6V	55ns	0.3µA	---	1µA	3µA	8µA	24µA	
	M5M5V208A## -70HI		70ns							

* "typical" parameter is sampled, not 100% tested.

PIN CONFIGURATION (TOP VIEW)



Outline 32P3K-B(KV)



Outline 32P3K-C(KR)

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FUNCTION

The operation mode of the M5M5V208A is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

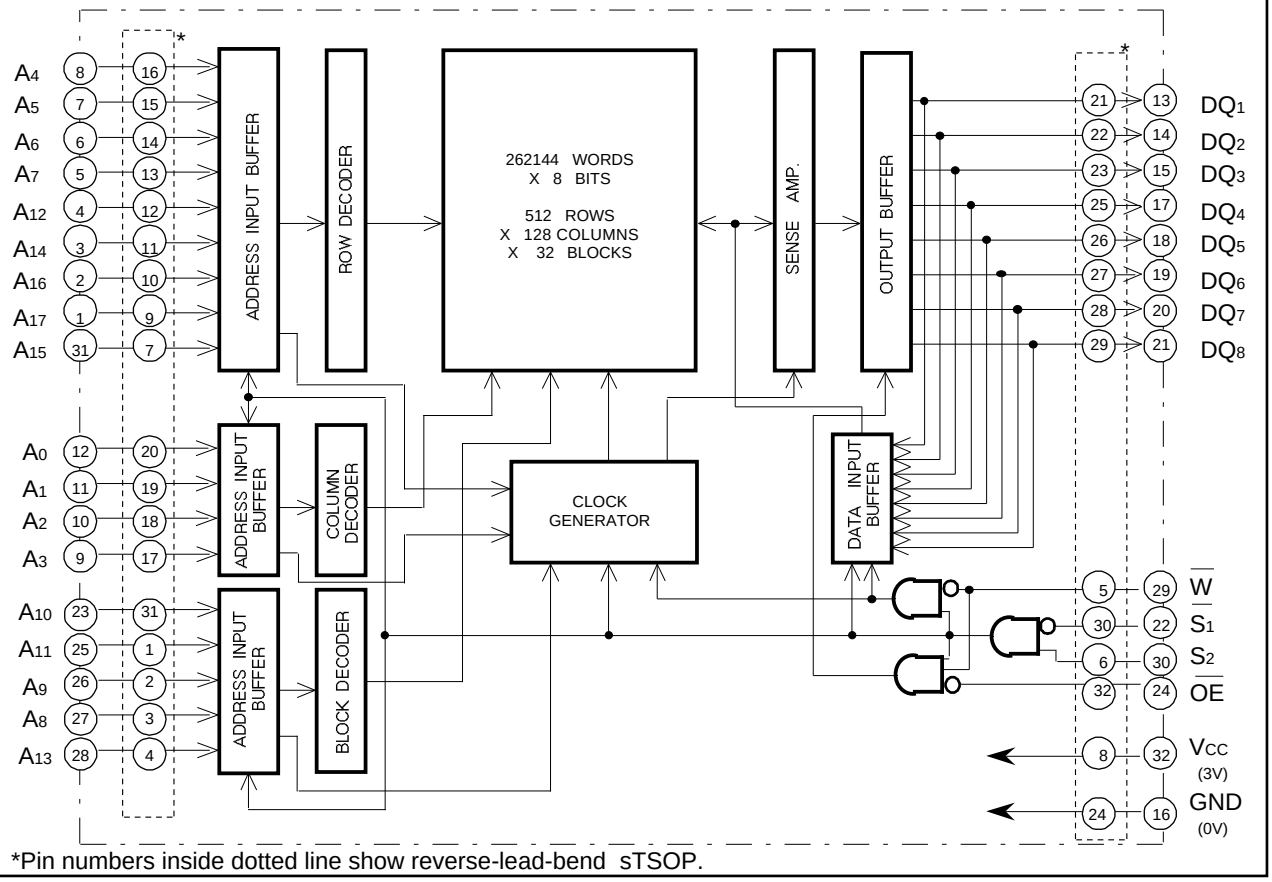
A read cycle is executed by setting $\overline{W}$ at a high level and OE at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L ,S_2 = H).

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ or S_2. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Standby
H	X	X	X	Non selection	High-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



*Pin numbers inside dotted line show reverse-lead-bend sTSOP.

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2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	- 0.5*~4.6	V
V_I	Input voltage		- 0.5* ~ Vcc + 0.5 (Max 4.6)	V
V_O	Output voltage		0 ~ Vcc	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature	Standard	0 ~ 70	°C
		W - Version	- 20 ~ 85	°C
		I - Version	- 40 ~ 85	°C
Tstr	Storage temperature		- 65 ~150	°C

* - 3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Vcc= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc +0.3V	V
V_{IL}	Low-level input voltage			- 0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH}= - 0.5mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}= - 0.05mA		Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0 ~ Vcc				±1	µA
I_O	Output current in off-state	$\overline{S_1}$=V_{IH} or S_2=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 ~ Vcc				±1	µA
Icc1	Active supply current (CMOS-level Input)	$\overline{S_1}$ ≤ 0.2V, S_2 ≥ Vcc-0.2V, other inputs ≤ 0.2V or ≥ Vcc-0.2V,output-open	f= 10MHz		20	25	mA
			f= 5MHz		10	13	
			f= 1MHz		3	5	
Icc2	Active supply current (TTL-level Input)	$\overline{S_1}$=V_{IL},S_2=V_{IH}, other inputs=V_{IH} or V_{IL} output-open	f= 10MHz		22	27	mA
			f= 5MHz		12	15	
			f= 1MHz		3	5	
Icc3	Stand-by current	1) S_2 ≤ 0.2V, other inputs=0 ~ Vcc or 2) $\overline{S_1}$ ≥ Vcc-0.2V, S_2 ≥ Vcc-0.2V other inputs=0 ~ Vcc	-L			60	µA
			-H ~+25°C		0.3	2	
			-HW ~+40°C			5	
			-HI ~+70°C			10	
			-HW / I ~+85°C			30	
Icc4	Stand-by current	$\overline{S_1}$=V_{IH} or S_2=V_{IL},other inputs=0 ~ Vcc				0.33	mA

* - 3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE

(Vcc= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			8	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is for Vcc = 3V, Ta = 25°C

AC ELECTRICAL CHARACTERISTICS

(Vcc= 2.7 ~ 3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Vcc ..... 2.7 ~ 3.6V
Input pulse level ..... V_{IH}=2.2V,V_{IL}=0.4V
Input rise and fall time 5ns
Reference level ..... V_{OH}=V_{OL}=1.5V
Output loads ..... Fig.1,CL=30pF
CL=5pF (for ten,tdis)
Transition is measured ±500mV from steady state voltage. (for ten,tdis)

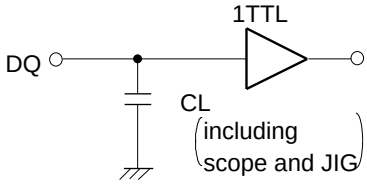

Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Unit
		-55L,H		-70L,H		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
t_a(A)	Address access time		55		70	ns
$t_a(S_1)$	Chip select 1 access time		55		70	ns
$t_a(S_2)$	Chip select 2 access time		55		70	ns
t_a(OE)	Output enable access time		30		35	ns
$t_{dis}(S_1)$	Output disable time after $\overline{S_1}$ high		20		25	ns
$t_{dis}(S_2)$	Output disable time after S_2 low		20		25	ns
t_{dis}(OE)	Output disable time after $\overline{OE}$ high		20		25	ns
$t_{en}(S_1)$	Output enable time after $\overline{S_1}$ low	10		10		ns
$t_{en}(S_2)$	Output enable time after S_2 high	10		10		ns
t_{en}(OE)	Output enable time after $\overline{OE}$ low	5		5		ns
t_v(A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		-55L,H		-55L,H		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
t_w(W)	Write pulse width	45		55		ns
t_{su}(A)	Address setup time	0		0		ns
t_{su}(A-WH)	Address setup time with respect to $\overline{W}$	50		65		ns
$t_{su}(S_1)$	Chip select 1 setup time	50		65		ns
$t_{su}(S_2)$	Chip select 2 setup time	50		65		ns
t_{su}(D)	Data setup time	25		30		ns
t_h(D)	Data hold time	0		0		ns
t_{rec}(W)	Write recovery time	0		0		ns
t_{dis}(W)	Output disable time from $\overline{W}$ low		20		25	ns
t_{dis}(OE)	Output disable time from $\overline{OE}$ high		20		25	ns
t_{en}(W)	Output enable time from $\overline{W}$ high	5		5		ns
t_{en}(OE)	Output enable time from $\overline{OE}$ low	5		5		ns

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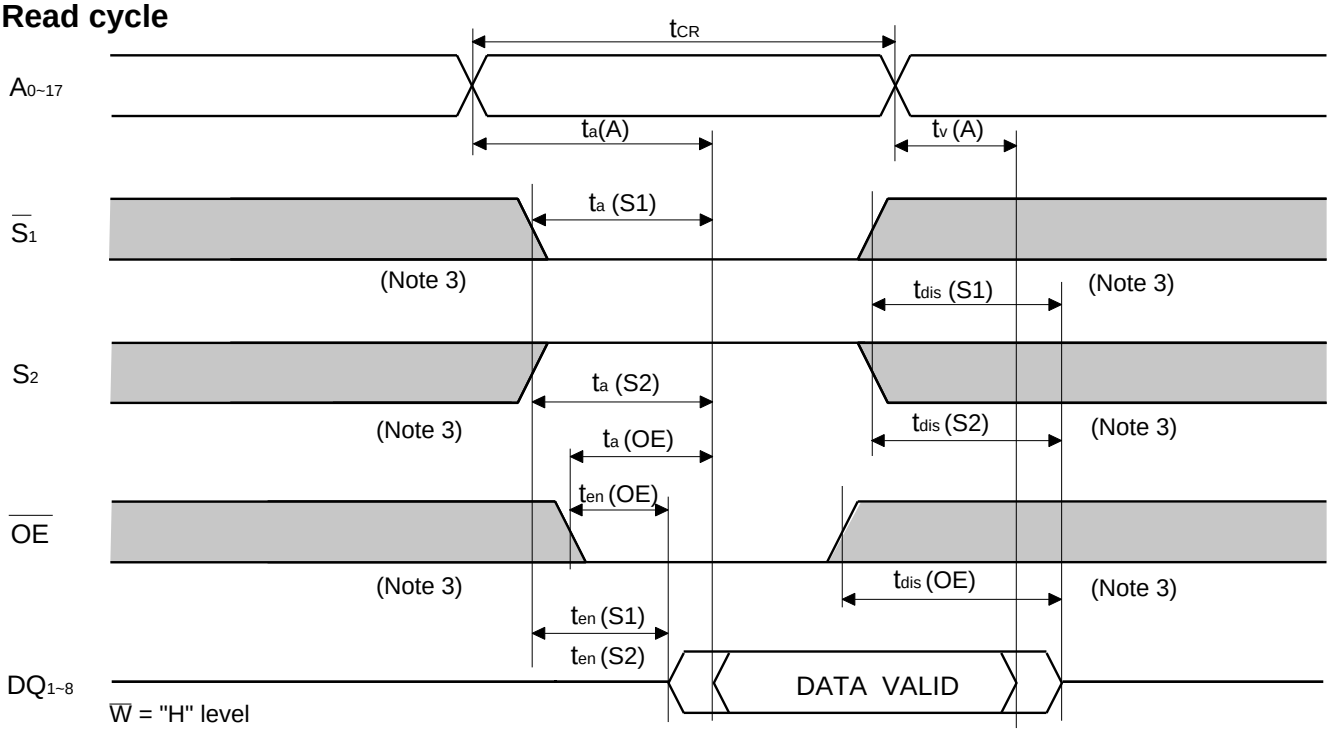
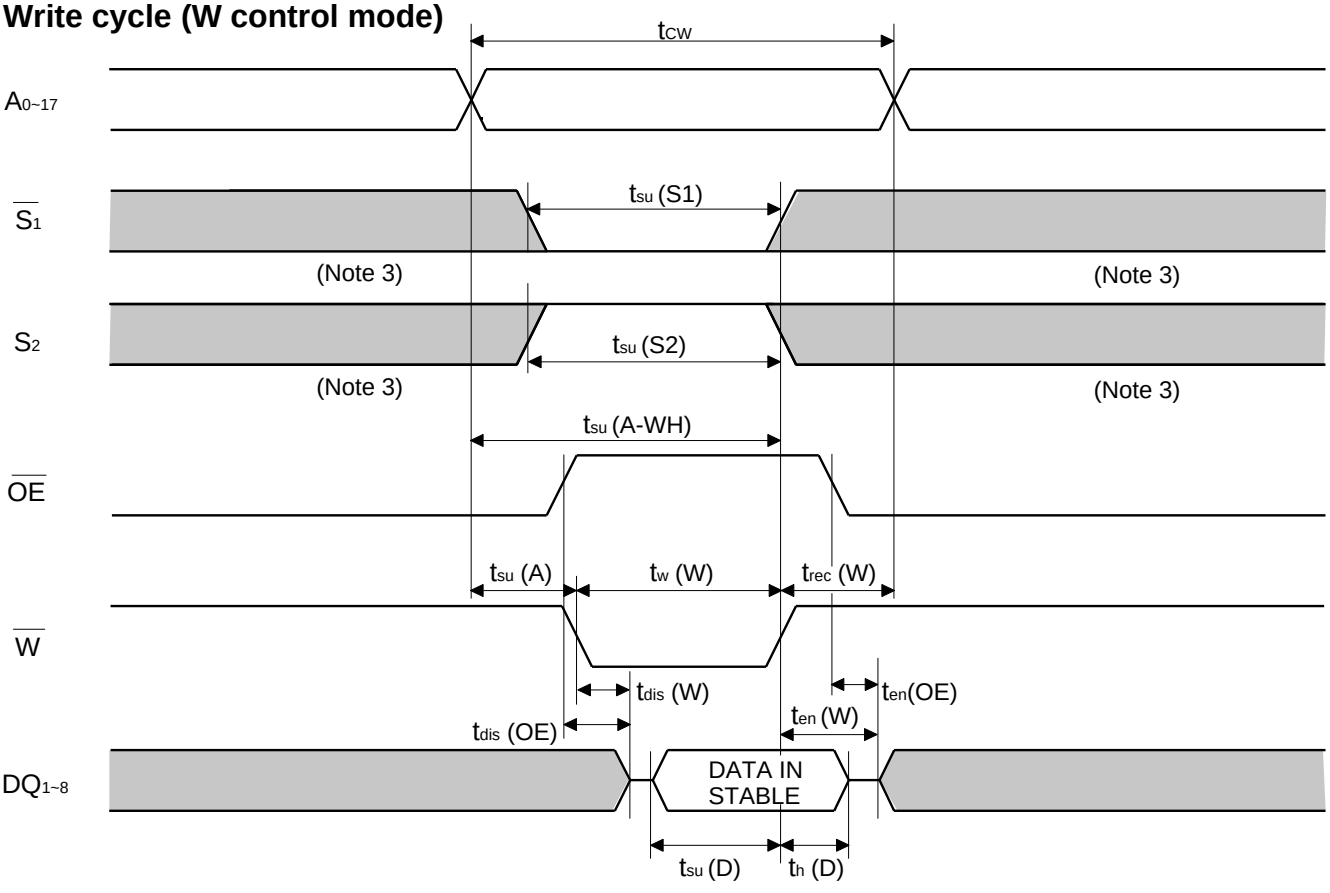
(4) TIMING DIAGRAMS

Read cycle

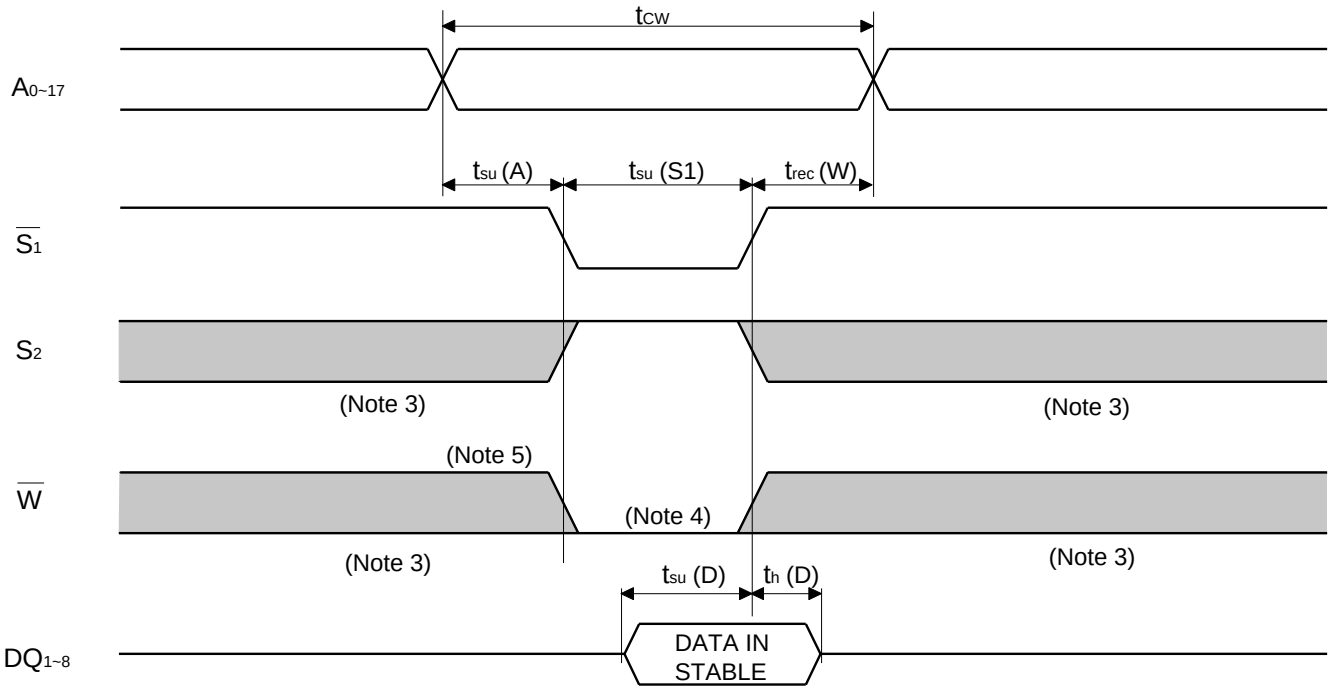


W = "H" level

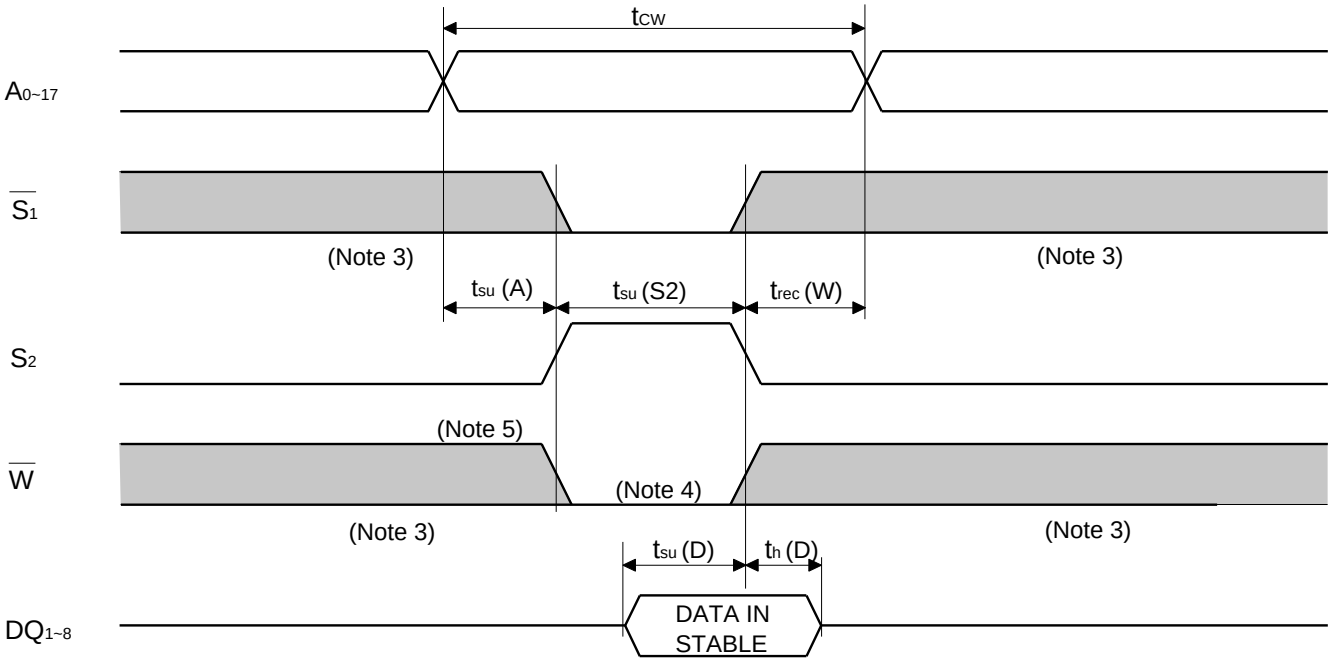
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S2 high overlaps $\overline{S1}$ and $\overline{W}$ low.
5: When the falling edge of W is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

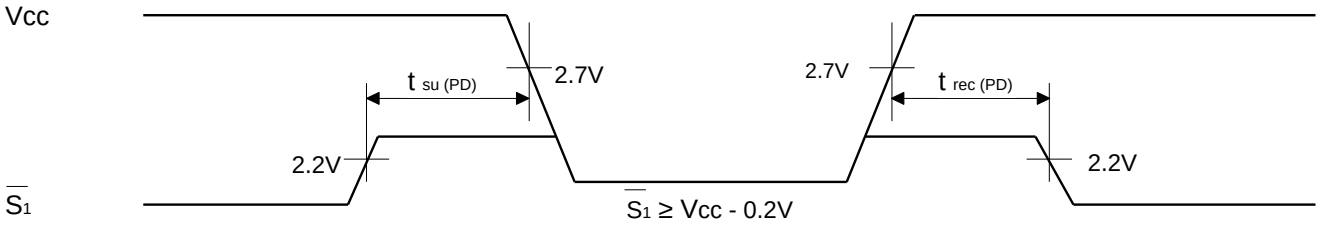
Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage				2			V
$V_{I\ (\overline{S1})}$	Chip select input $\overline{S_1}$				2.0			V
$V_{I\ (S2)}$	Chip select input S_2						0.2	V
$I_{CC\ (PD)}$	Power down supply current	Vcc=3.0V 1) $S_2 \le 0.2V$,other inputs=0 ~ Vcc or 2) $\overline{S_1} \ge Vcc-0.2V$, $S_2 \ge Vcc-0.2V$ other inputs=0 ~ Vcc	-L				50	µA
			-H	~+25°C		0.3	1	
			-HW	~+40°C			3	
			-HI	~+70°C			8	
			-HW / I	~+85°C			24	

(2) TIMING REQUIREMENTS

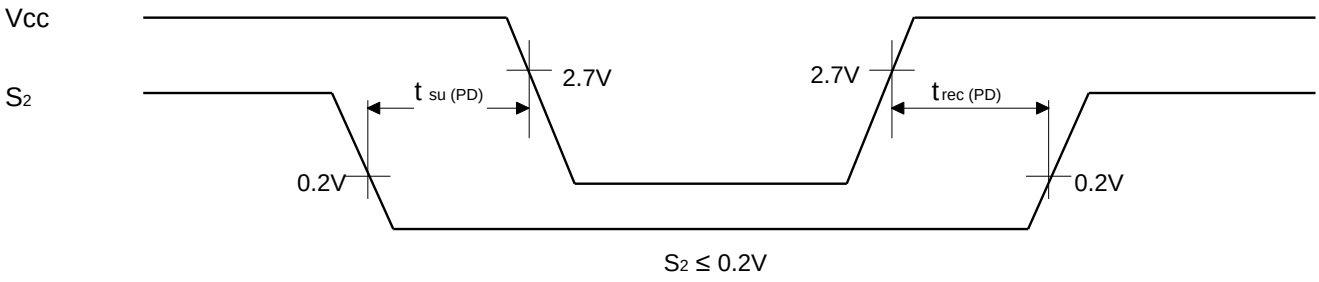
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode



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Revision History

Revision No.	History	Date	
A0.1E	The first edition	09.Nov.'98	Preliminary
A0.2E	The second edition	29.Nov.'99	Preliminary