



64K × 16 CMOS FLASH MEMORY

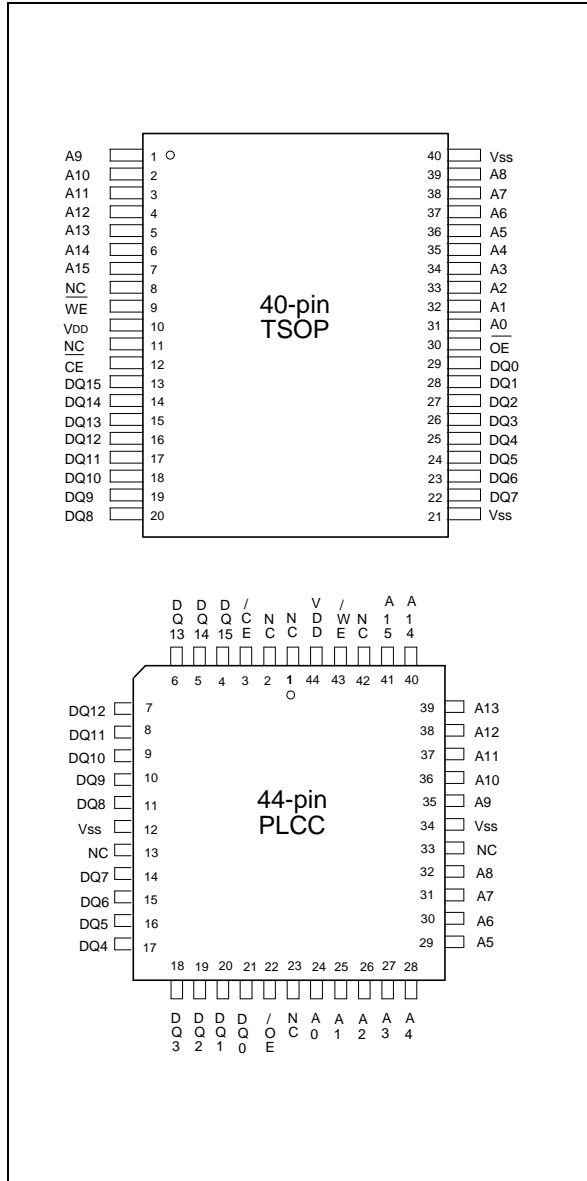
GENERAL DESCRIPTION

The W49F102 is a 1-megabit, 5-volt only CMOS flash memory organized as 64K × 16 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W49F102 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

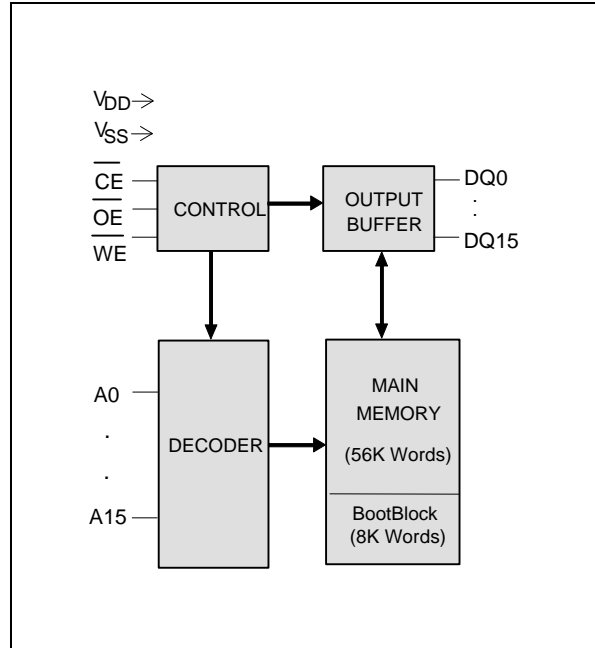
FEATURES

- Single 5-volt operations:
 - 5-volt Read
 - 5-volt Erase
 - 5-volt Program
- Fast Program operation:
 - Word-by-Word programming: 50 μS (max.)
- Fast Erase operation: 100 mS (typ.)
- Fast Read access time: 40/45 nS
- Endurance: 10K cycles (typ.)
- Ten-year data retention
- Hardware data protection
- 8K word Boot Block with Lockout protection
- Low power consumption
 - Active current: 25 mA (typ.)
 - Standby current: 20 μA (typ.)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 40-pin TSOP and 44-pin PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
VDD	Power Supply
VSS	Ground
NC	No Connection



FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49F102 is controlled by \overline{CE} and \overline{OE} , both of which have to be low for the host to obtain data from the outputs. \overline{CE} is used for device selection. When \overline{CE} is high, the chip is de-selected and only standby power will be consumed. \overline{OE} is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either \overline{CE} or \overline{OE} is high. Refer to the timing waveforms for further details.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words of the memory with the address range from 0000 hex to 1FFF hex.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function will only affect the main memory.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data is "FF hex," the boot block programming lockout feature is activated; if the output data is "FE hex," the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the main memory will be erased to FF(hex), and the data in the boot block will not be erased (remains same as before the chip erase operation). The entire memory array (main memory and boot block) will be erased to FF(hex). by the chip erase operation if the boot block programming lockout feature is not activated. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Main Memory Erase Operation

The main memory erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal main-memory erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.



Program Operation

The W49F102 is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0". The erase operation (changed entire data in main memory and/or boot block from "0" to "1" is needed before programming).

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will internally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (50 μ S max. - TBP) once completed and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49F102 is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A \overline{WE} pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming operation is inhibited when VDD is less than 2.5V typical.
- (3) Write Inhibit Mode: Forcing \overline{OE} low, \overline{CE} high, or \overline{WE} high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.
- (4) VDD power-on delay: When VDD has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ7 & DQ15)- Write Status Detection

The W49F102 includes a data polling feature to indicate the end of a program or erase cycle. When the W49F102 is in the internal program or erase cycle, any attempt to read DQ7 or DQ15 of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ7 or DQ15 will show the true data. Note that DQ7 or DQ15 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.

Toggle Bit (DQ6 & DQ14)- Write Status Detection

In addition to data polling, the W49F102 provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ6 or DQ14 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (00DAh). A read from address 0001H outputs the device code (002Fh). The product ID operation can be terminated by a three-word command sequence or an alternate one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing \overline{CE} and \overline{OE} low, \overline{WE} high, and raising A9 to 12 volts.



TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V ± 5%)

MODE	PINS				
	\overline{CE}	\overline{OE}	\overline{WE}	ADDRESS	DQ.
Read	VIL	VIL	VIH	A _{IN}	Dout
Write	VIL	VIH	VIL	A _{IN}	Din
Standby	VIH	X	X	X	High Z
Write Inhibit	X	VIL	X	X	High Z/DOUT
	X	X	VIH	X	High Z/DOUT
Output Disable	X	VIH	X	X	High Z
Product ID	VIL	VIL	VIH	A0 = VIL; A1–A15 = VIL; A9 = VHH	Manufacturer Code 00DA (Hex)
	VIL	VIL	VIH	A0 = VIH; A1–A15 = VIL; A9 = VHH	Device Code 002F (Hex)

TABLE OF COMMAND DEFINITION

Command Description	No. of Cycles	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
		Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data
Read	1	A _{IN} D _{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Main Memory Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 30
Word Program	4	5555 AA	2AAA 55	5555 A0	A _{IN} D _{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit ⁽¹⁾	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit ⁽¹⁾	1	XXXX F0					

Note: Address Format: A14–A0 (Hex); Data Format: DQ15–DQ8 (Don't Care); DQ7–DQ0 (Hex)

Either one of the two Product ID Exit commands can be used.

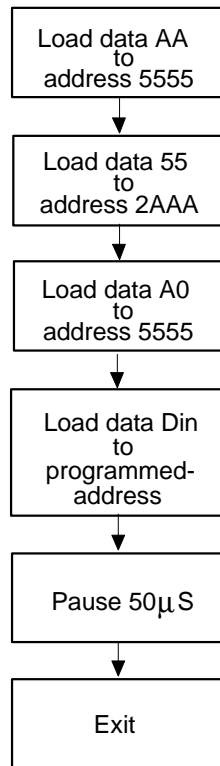


Command Codes for Word Program

WORD SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H
3 Write	Programmed-Address	Programmed-Data

Word Program Flow Chart

Word Program Command Flow



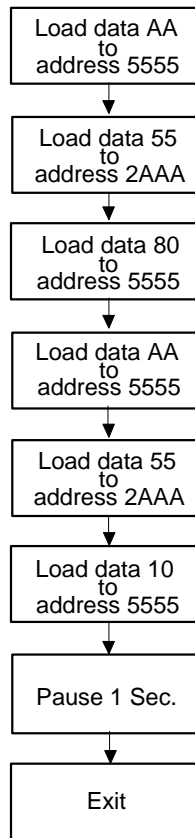
Notes for software program code:
 Data Format: DQ15–DQ0 (Hex); XX = Don't Care
 Address Format: A14–A0 (Hex)



Command Codes for Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	10H

Chip Erase Acquisition Flow



Notes for chip erase:

Data Format: DQ15-DQ8: Don't Care; DQ7-DQ0 (Hex)

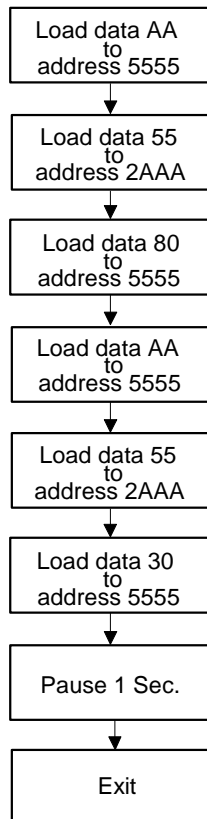
Address Format: A14-A0 (Hex)



Command Codes for Main Memory Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	30H

Main Memory Erase Acquisition Flow



Notes for chip erase:

Data Format: DQ15-DQ8: Don't Care; DQ7-DQ0 (Hex)

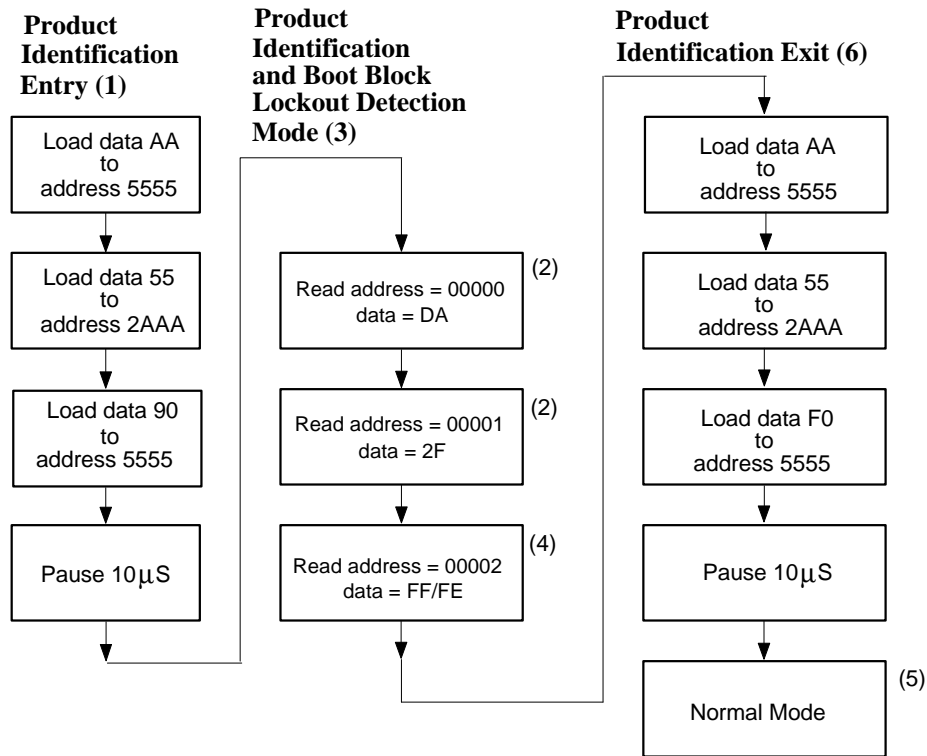
Address Format: A14-A0 (Hex)



Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT (6)	
	ADDRESS	DATA	ADDRESS	DATA
1 Write	5555	AA	5555H	AAH
2 Write	2AAA	55	2AAAH	55H
3 Write	5555	90	5555H	F0H
	Pause 10 μS		Pause 10 μS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

- (1) Data Format: DQ15-DQ8 (Don't Care), DQ7-DQ0 (Hex); Address Format: A14-A0 (Hex)
- (2) A1-A15 = VIL; manufacture code is read for A0 = VIL; device code is read for A0 = VIH.
- (3) The device does not remain in identification and boot block lockout detection mode if power down.
- (4) If the output data is "FF Hex," the boot block programming lockout feature is activated; if the output data "FE Hex," the lockout feature is inactivated and the block can be programmed.
- (5) The device returns to standard operation mode.
- (6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

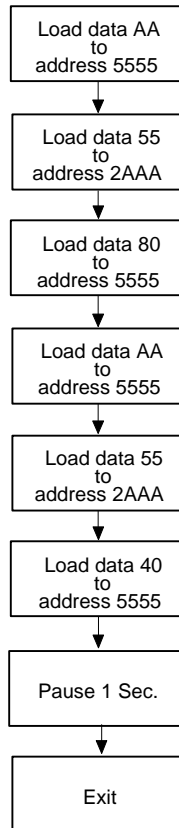


Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET	
	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	40H
Pause 1 Sec.		

Boot Block Lockout Enable Acquisition Flow

Boot Block Lockout Feature Set Flow



Notes for boot block lockout enable:
 Data Format: DQ15-DQ8 Don't Care), DQ7-DQ0 (Hex)
 Address Format: A14-A0 (Hex)



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to VSS Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except \overline{OE}	-0.5 to VDD +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to VDD +1.0	V
Voltage on \overline{OE} Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(VDD = 5.0V ±10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	ICC	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/Os open Address inputs = V_{IL}/V_{IH} , at f = 5 MHz	-	25	50	mA
Standby VDD Current (TTL input)	ISB1	$\overline{CE} = V_{IH}$, all I/Os open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby VDD Current (CMOS input)	ISB2	$\overline{CE} = V_{DD} - 0.3V$, all I/Os open Other inputs = $V_{DD} - 0.3V/V_{SS}$	-	20	100	μA
Input Leakage Current	ILI	VIN = VSS to VDD	-	-	10	μA
Output Leakage Current	ILO	VOUT = VSS to VDD	-	-	10	μA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.0	-	VDD +0.5	V
Output Low Voltage	VOL	IOL = 2.1 mA	-	-	0.45	V
Output High Voltage	VOH	IOH = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	μ S
Power-up to Write Operation	TPU. WRITE	5	mS

CAPACITANCE

($V_{DD} = 5.0V$, $T_A = 25^\circ C$, $f = 1$ MHz)

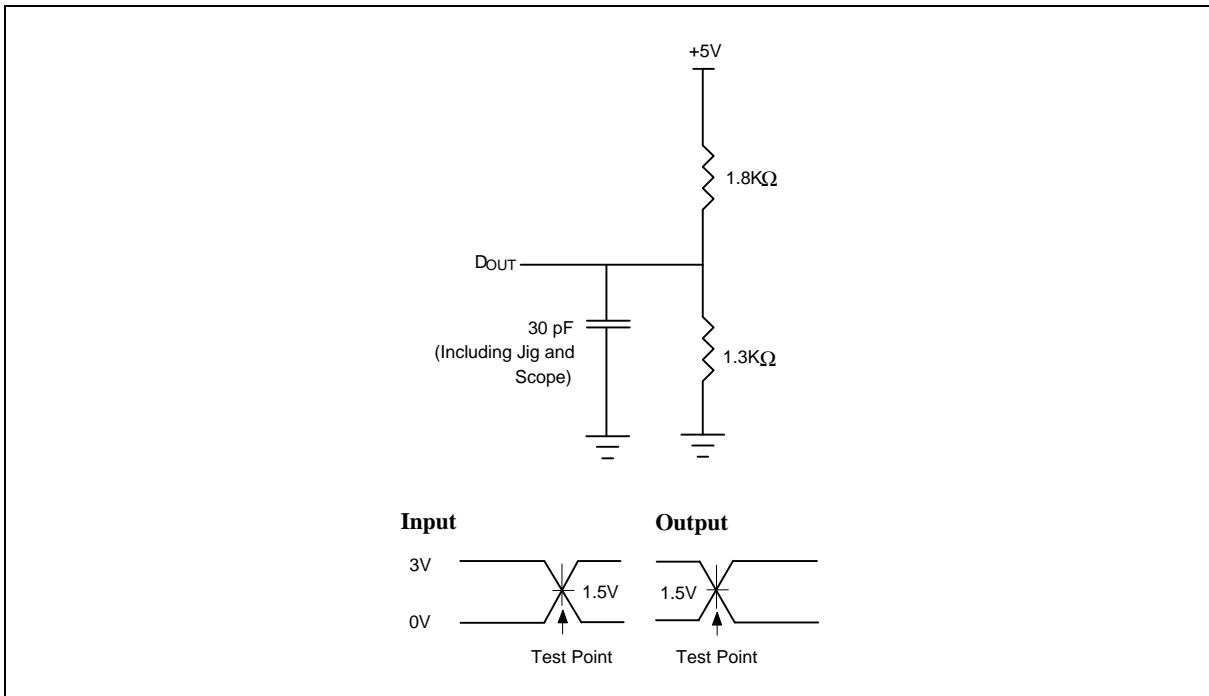
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	12	pf
Input Capacitance	C_{IN}	$V_{IN} = 0V$	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and $C_L = 30$ pF

AC Test Load and Waveform





AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 5.0V ±5 % for 35 nS; V_{DD} = 5.0V ±10 % for 40/45 nS, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49F102-40		W49F102-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	42	-	45	-	nS
Chip Enable Access Time	TCE	-	40	-	45	nS
Address Access Time	TAA	-	40	-	45	nS
Output Enable Access Time	TOE	-	20	-	25	nS
$\overline{\text{CE}}$ Low to Active Output	TCLZ	0	-	0	-	nS
$\overline{\text{OE}}$ Low to Active Output	TOLZ	0	-	0	-	nS
$\overline{\text{CE}}$ High to High-Z Output	TCHZ	-	15	-	20	nS
$\overline{\text{OE}}$ High to High-Z Output	TOHZ	-	15	-	20	nS
Output Hold from Address Change	TOH	0	-	0	-	nS

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	45	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Setup Time	TCS	0	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Hold Time	TCH	0	-	-	nS
$\overline{\text{OE}}$ High Setup Time	TOES	0	-	-	nS
$\overline{\text{OE}}$ High Hold Time	TOEH	0	-	-	nS
$\overline{\text{CE}}$ Pulse Width	TCP	50	-	-	nS
$\overline{\text{CE}}$ High Width	TCPH	50	-	-	nS
$\overline{\text{WE}}$ Pulse Width	TWP	45	-	-	nS
$\overline{\text{WE}}$ High Width	TWPH	45	-	-	nS
Data Setup Time	TDS	45	-	-	nS
Data Hold Time	TdH	0	-	-	nS
Word Programming Time	TBP	-	10	50	μS
Erase Cycle Time	TEC	-	0.1	1	Sec.

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.



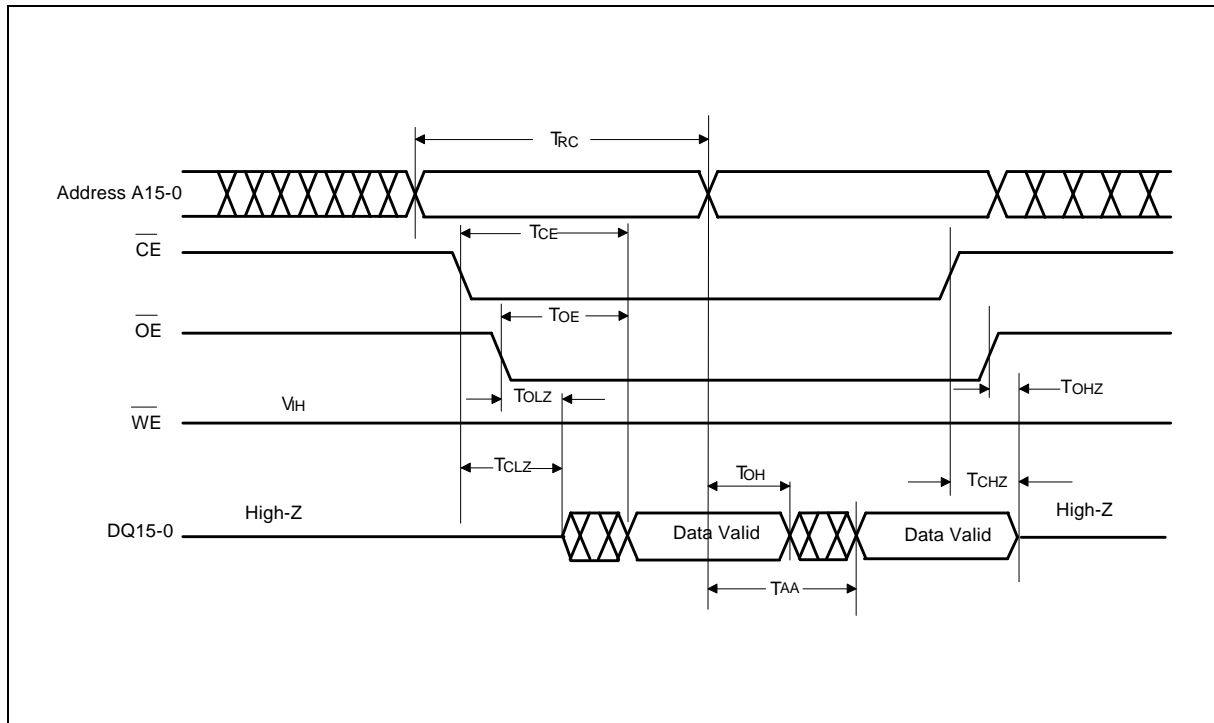
AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W49F102-40		W49F102-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
\overline{OE} to Data Polling Output Delay	TOEP	-	20	-	25	nS
\overline{CE} to Data Polling Output Delay	TCEP	-	40	-	45	nS
\overline{OE} to Toggle Bit Output Delay	TOET	-	20	-	25	nS
\overline{CE} to Toggle Bit Output Delay	TcET	-	40	-	45	nS

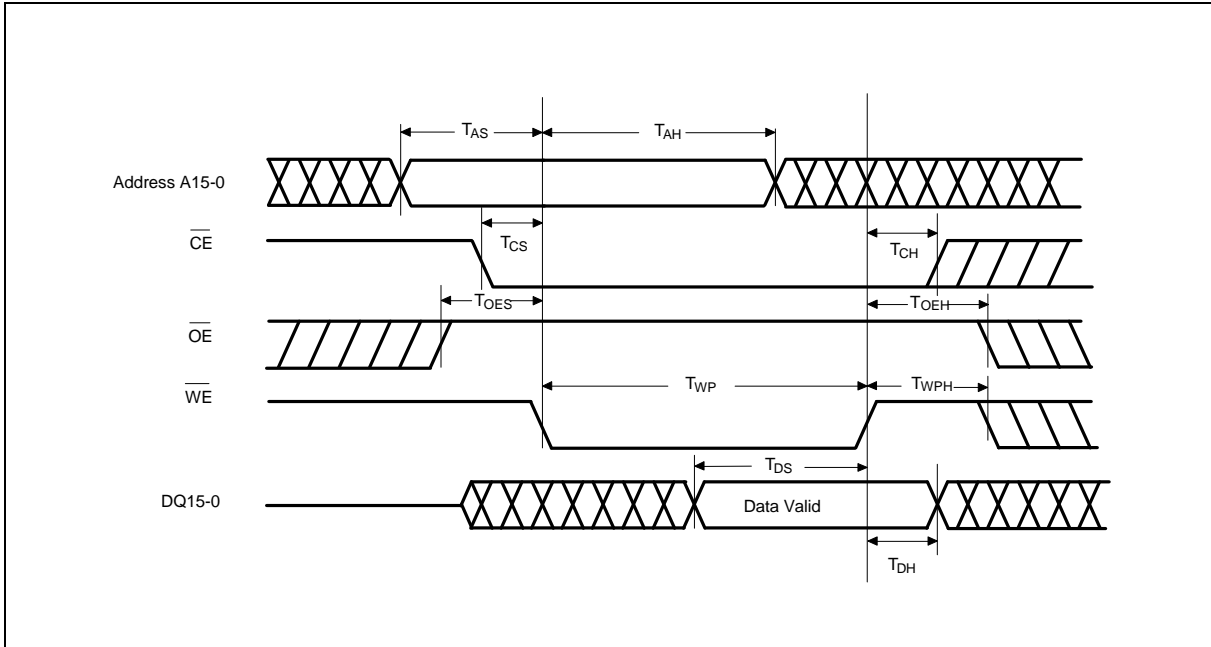
TIMING WAVEFORMS

Read Cycle Timing Diagram

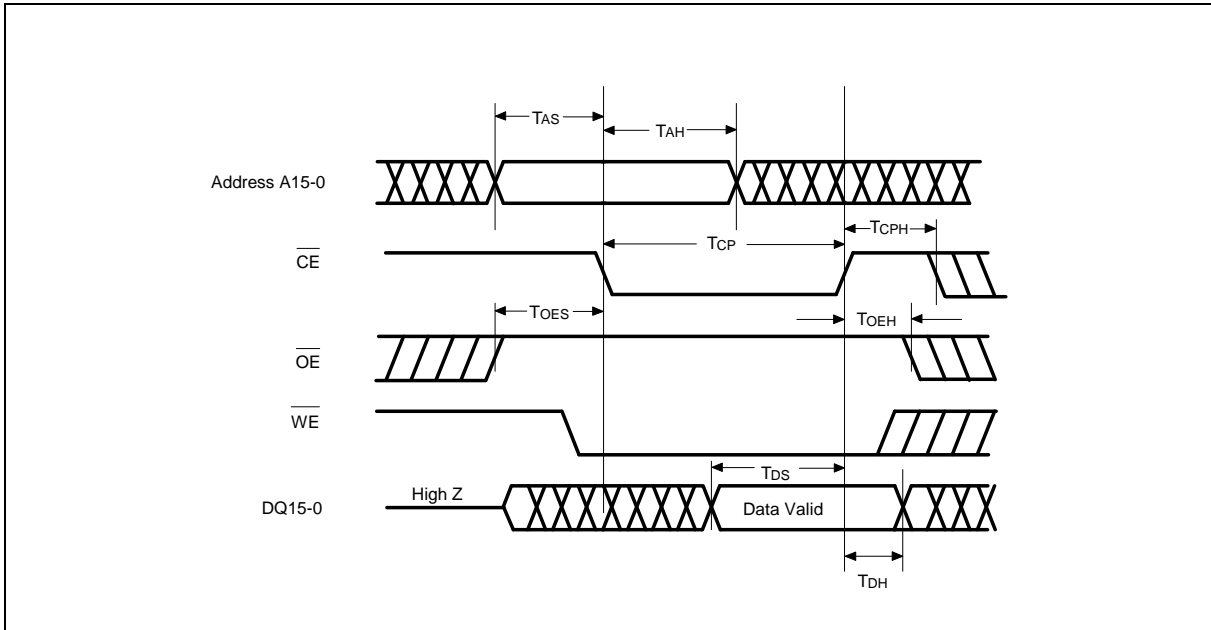


Timing Waveforms, continued

$\overline{\text{WE}}$ Controlled Command Write Cycle Timing Diagram

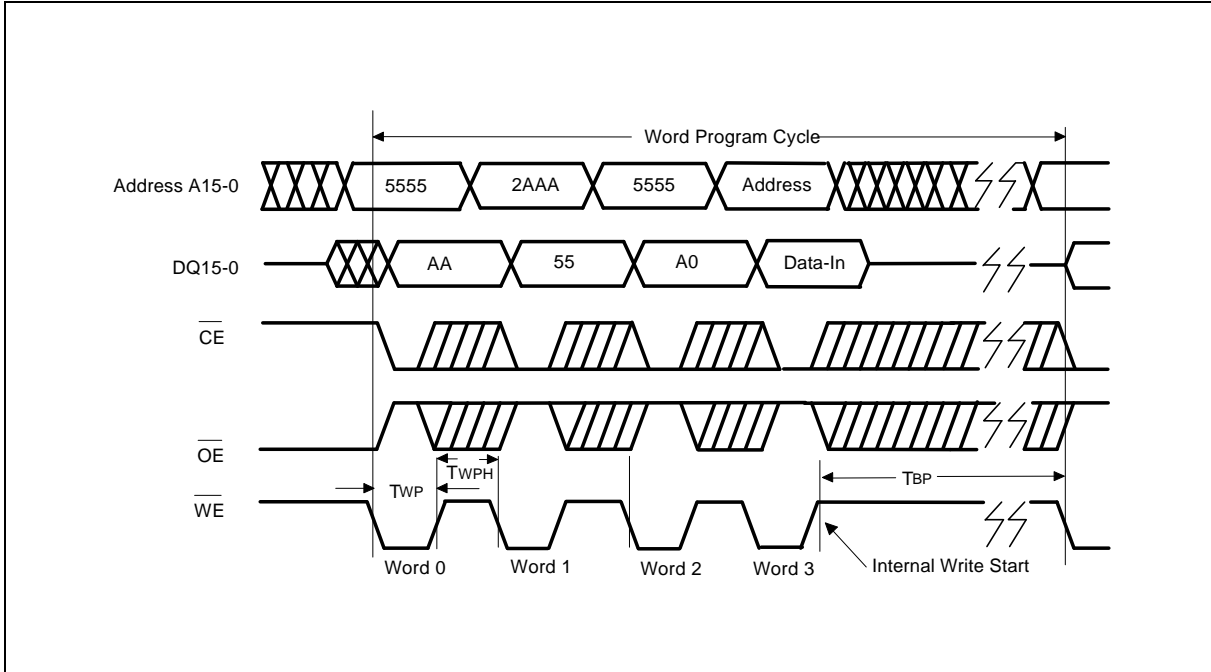


$\overline{\text{CE}}$ Controlled Command Write Cycle Timing Diagram

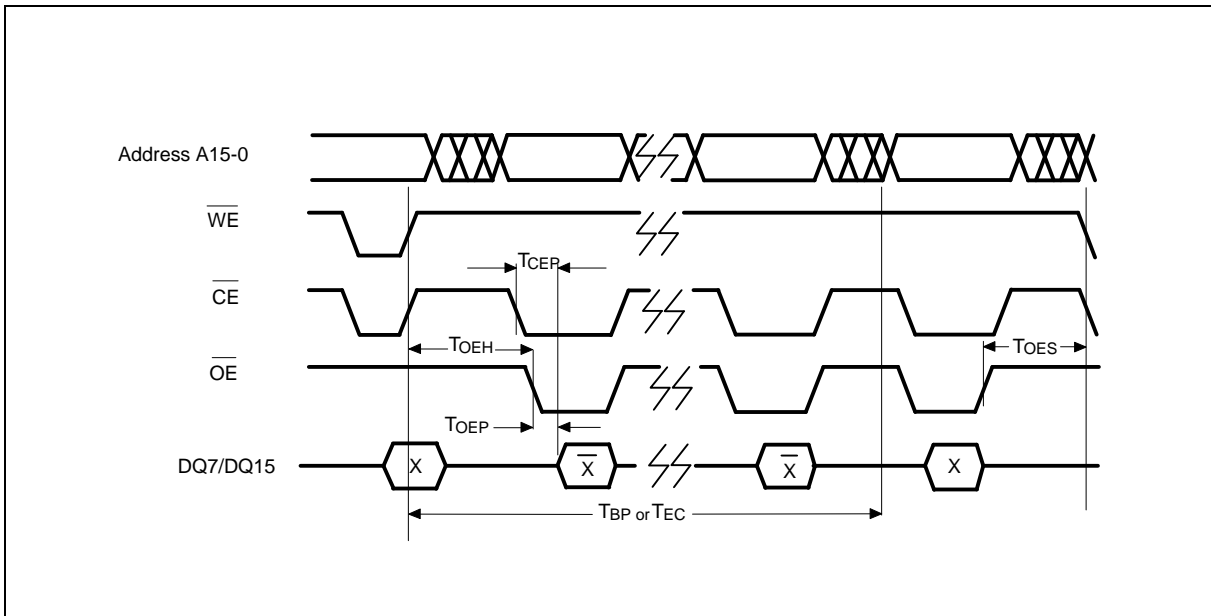


Timing Waveforms, continued

Program Cycle Timing Diagram

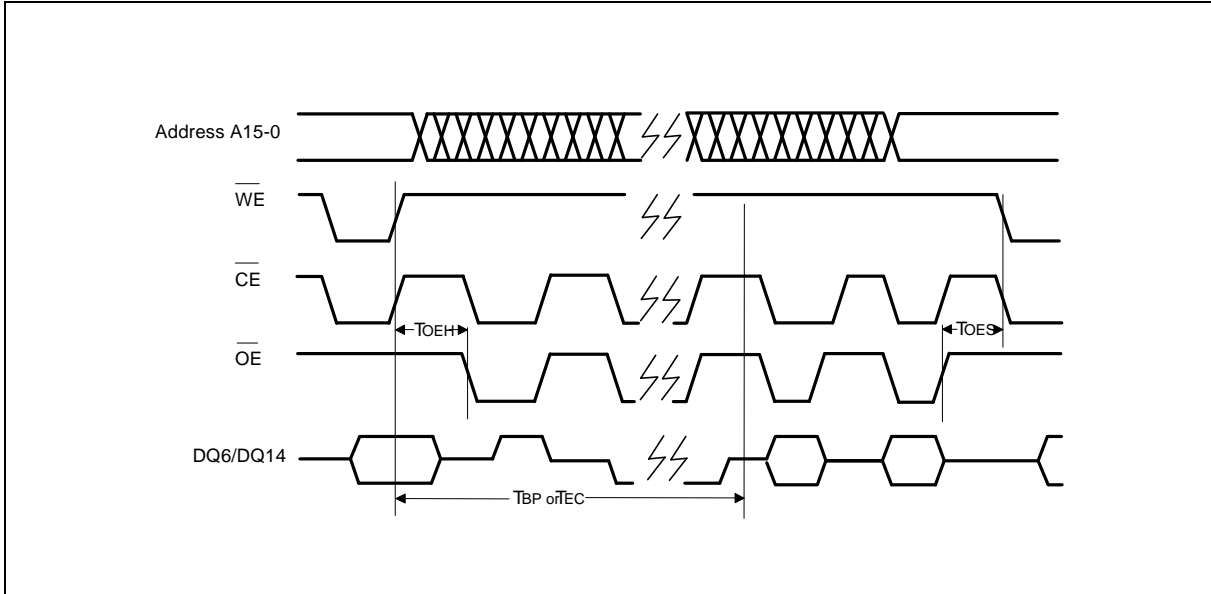


DATA Polling Timing Diagram

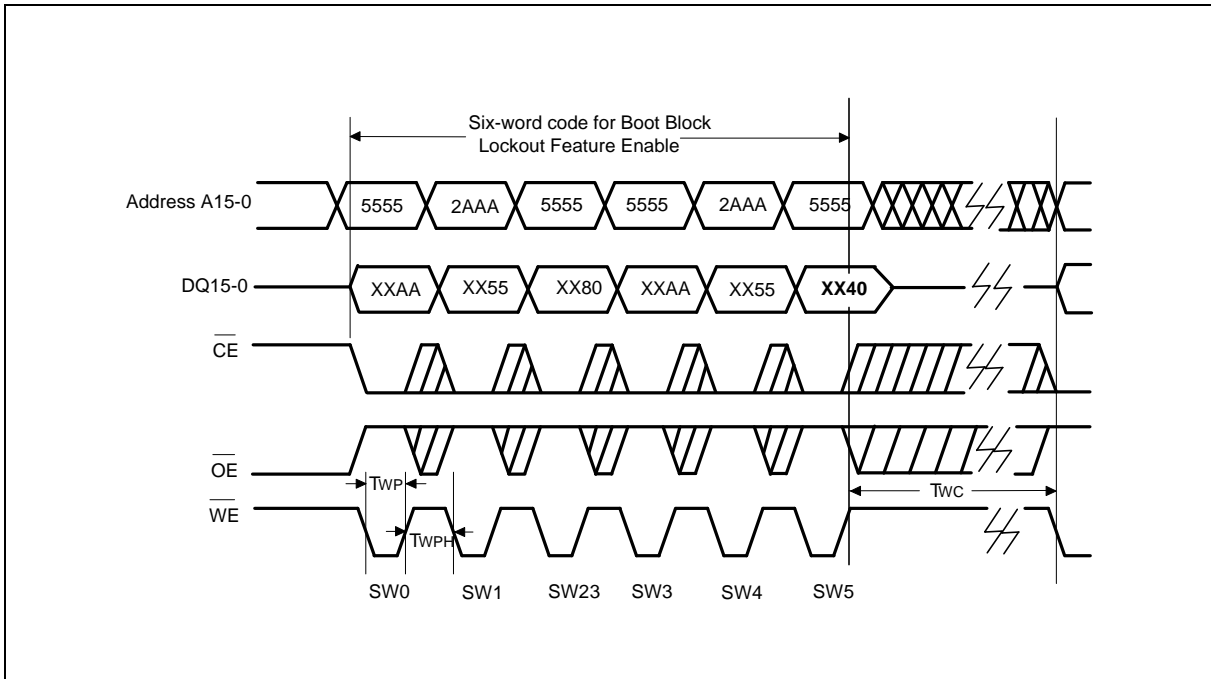


Timing Waveforms, continued

Toggle Bit Timing Diagram

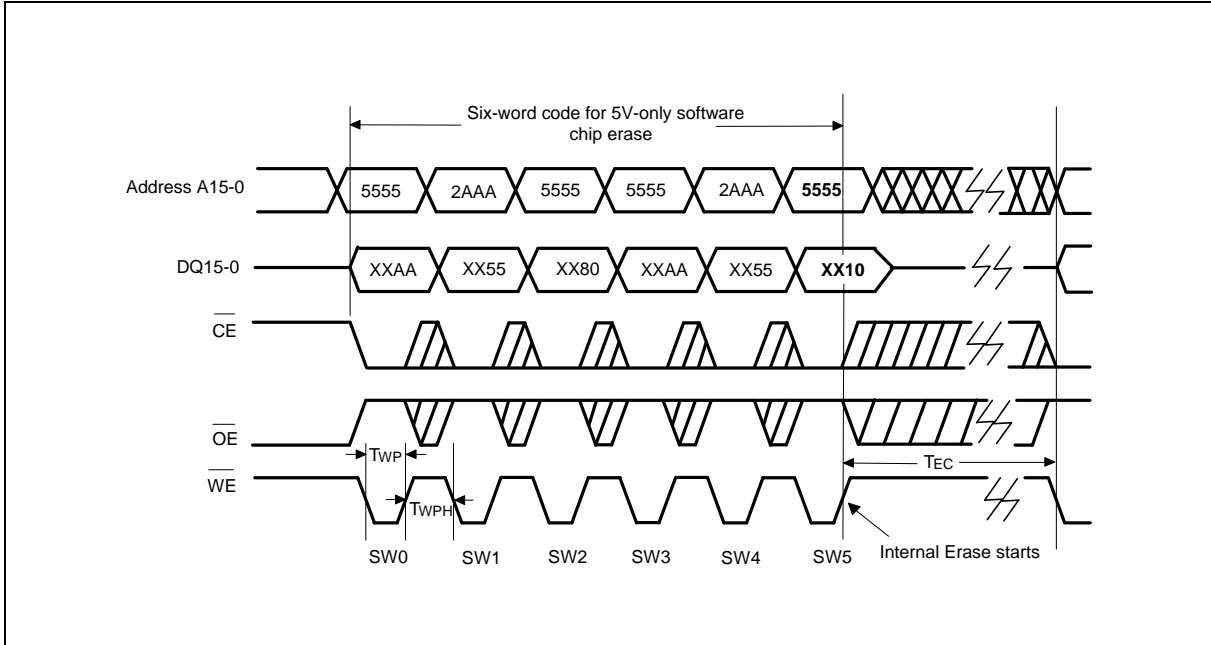


Boot Block Lockout Enable Timing Diagram

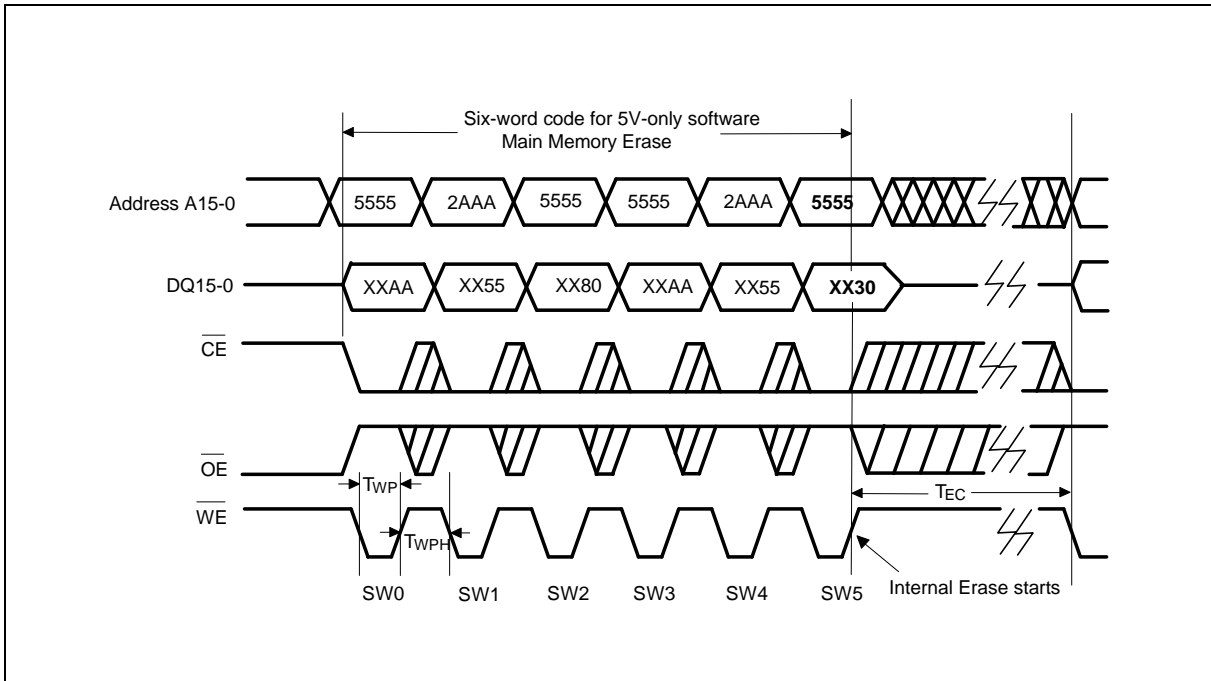


Timing Waveforms, continued

Chip Erase Timing Diagram



Main Memory Erase Timing Diagram





ORDERING INFORMATION

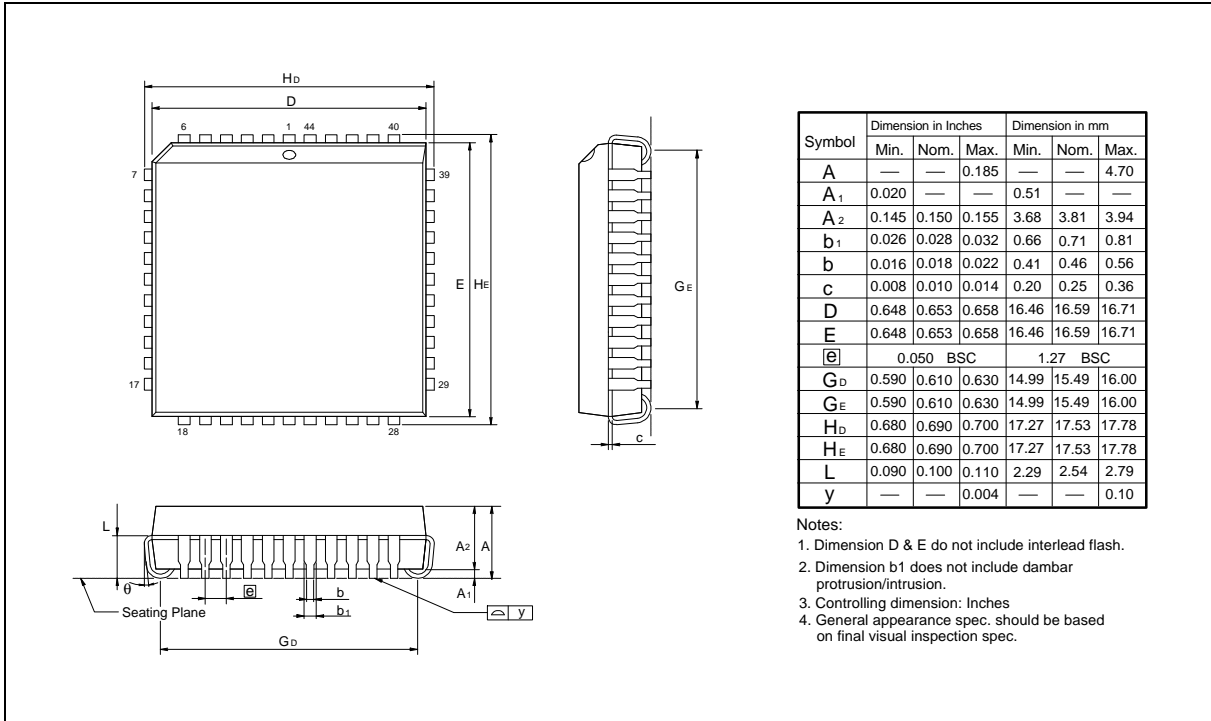
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V _{DD} CURRENT MAX. (mA)	PACKAGE	CYCLE
W49F102Q40	40	50	100 (CMOS)	40-pin TSOP (10 mm × 14 mm)	10K
W49F102Q45	45	50	100 (CMOS)	40-pin TSOP (10 mm × 14 mm)	10K
W49F102P40	40	50	100 (CMOS)	44-pin PLCC	10K
W49F102P45	45	50	100 (CMOS)	44-pin PLCC	10K

Notes:

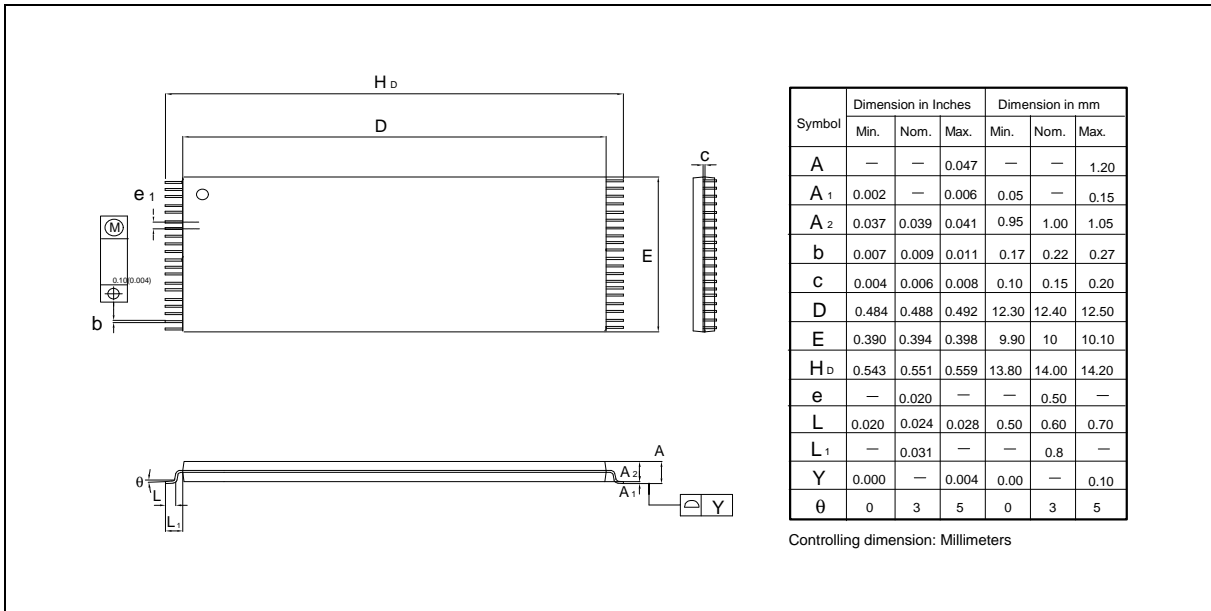
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

44-pin PLCC



40-pin TSOP (10 mm × 14 mm)





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 1999	-	Initial Issued
A2	Oct. 1999	13	Change Read Cycle Timing Parameter: VDD = 5.0V \pm 10% for 40, 45, 50, 55, 70 nS
A3	Oct. 2000	1, 11, 13, 14, 19	Delete 35, 50, 55, 70 nS bins
		13	TRC: 35 nS -> 40 nS; 40 nS -> 42 nS
			TAH: 50 nS -> 45 nS
			TWP & TWPH: 90 nS -> 45 nS
			TCP: 90 nS -> 50 nS
			Add in TcPH = 50 nS
		TDS: 50 nS -> 45 nS	
1, 21	Delete 1K cycling option		

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Note: All data and specifications are subject to change without notice.

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