

## Advance Information

# 512K x 8 Bit Static Random Access Memory

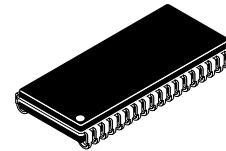
The MCM6946 is a 4,194,304-bit static random access memory organized as 524,288 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6946 is equipped with chip enable ( $\bar{E}$ ) and output enable ( $\bar{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high-impedance.

The MCM6946 is available in a 400 mil, 36-lead surface-mount SOJ package.

- Single 3.3 V – 5%, + 10% Power Supply
- Fast Access Time: 8/10/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Power Operation: 195/185/180/175 mA Maximum, Active AC
- Available in TSOP or SOJ Packages

## MCM6946



**YJ PACKAGE**  
400 MIL SOJ  
CASE 893-02



**TS PACKAGE**  
44-LEAD  
TSOP TYPE II  
CASE 924A-02

### PIN NAMES

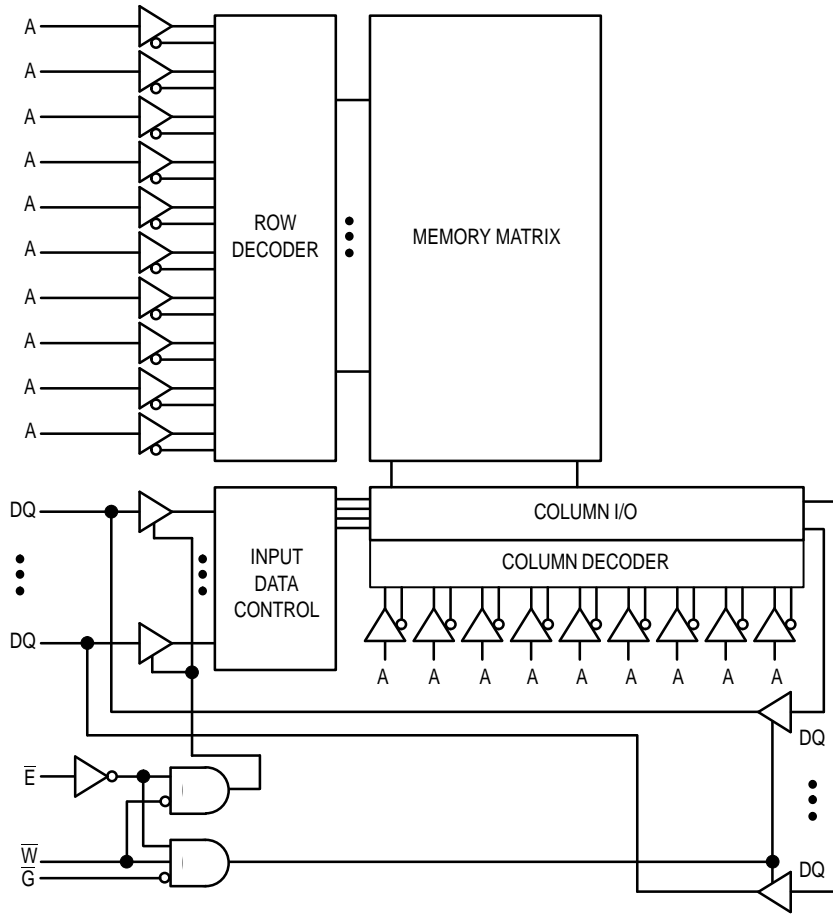
A0 – A18	.....	Address Inputs
$\bar{W}$	.....	Write Enable
$\bar{G}$	.....	Output Enable
$\bar{E}$	.....	Chip Enable
DQ	.....	Data Input/Output
NC	.....	No Connection
VCC	.....	+ 3.3 V Power Supply
VSS	.....	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 5  
3/31/98



# BLOCK DIAGRAM



## PIN ASSIGNMENTS

**400 MIL SOJ**

A	1 ●	36	NC
A	2	35	A
A	3	34	A
A	4	33	A
A	5	32	A
$\bar{E}$	6	31	$\bar{G}$
DQ	7	30	DQ
DQ	8	29	DQ
VCC	9	28	VSS
VSS	10	27	VCC
DQ	11	26	DQ
DQ	12	25	DQ
$\bar{W}$	13	24	A
A	14	23	A
A	15	22	A
A	16	21	A
A	17	20	A
A	18	19	NC

**TSOP TYPE II**

NC	1 ●	44	NC
NC	2	43	NC
A	3	42	NC
A	4	41	A
A	5	40	A
A	6	39	A
A	7	38	A
$\bar{E}$	8	37	$\bar{G}$
DQ	9	36	DQ
DQ	10	35	DQ
VDD	11	34	VSS
VSS	12	33	VDD
DQ	13	32	DQ
DQ	14	31	DQ
$\bar{W}$	15	30	A
A	16	29	A
A	17	28	A
A	18	27	A
A	19	26	A
A	20	25	NC
NC	21	24	NC
NC	22	23	NC

**TRUTH TABLE** (X = Don't Care)

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	$I_{SB1}, I_{SB2}$
L	H	H	Output Disabled	High-Z	—	$I_{CCA}$
L	L	H	Read	$D_{out}$	Read	$I_{CCA}$
L	X	L	Write	High-Z	Write	$I_{CCA}$

**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to $V_{SS}$	$V_{CC}$	- 0.5 to + 5.0	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}, V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	$\pm 20$	mA
Power Dissipation	$P_D$	1.0	W
Temperature Under Bias	$T_{bias}$	- 10 to + 85	$^{\circ}C$
Operating Temperature	$T_A$	0 to + 70	$^{\circ}C$
Storage Temperature — Plastic	$T_{stg}$	- 55 to + 150	$^{\circ}C$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**  
 ( $V_{CC} = 3.3\text{ V} - 5\%, + 10\%$ ,  $T_A = 0\text{ to } + 70^\circ\text{C}$ , Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	3.135	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	$-0.5^*$	—	0.8	V

\*  $V_{IL}(\text{min}) = -0.5\text{ V dc}$ ;  $V_{IL}(\text{min}) = -2.0\text{ V ac}$  (pulse width  $\leq 2.0\text{ ns}$ ).

\*\*  $V_{IH}(\text{max}) = V_{CC} + 0.3\text{ V dc}$ ;  $V_{IH}(\text{max}) = V_{CC} + 2.0\text{ V ac}$  (pulse width  $\leq 2.0\text{ ns}$ ).

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0\text{ to } V_{CC}$ )	$I_{kg}(I)$	—	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $\bar{E} = V_{IH}$ , $V_{out} = 0\text{ to } V_{CC}$ )	$I_{kg}(O)$	—	$\pm 1.0$	$\mu\text{A}$
Output Low Voltage ( $I_{OL} = + 8.0\text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = - 4.0\text{ mA}$ )	$V_{OH}$	2.4	—	V

**POWER SUPPLY CURRENTS**

Parameter	Symbol	0 to 70°C	Unit	
AC Active Supply Current ( $I_{out} = 0\text{ mA}$ , $V_{CC} = \text{Max}$ )	MCM6946-8: $t_{AVAV} = 8\text{ ns}$ MCM6946-10: $t_{AVAV} = 10\text{ ns}$ MCM6946-12: $t_{AVAV} = 12\text{ ns}$ MCM6946-15: $t_{AVAV} = 15\text{ ns}$	$I_{CC}$	195 185 180 175	mA
AC Standby Current ( $V_{CC} = \text{Max}$ , $\bar{E} = V_{IH}$ , No Other Restrictions on Other Inputs)	MCM6946-8: $t_{AVAV} = 8\text{ ns}$ MCM6946-10: $t_{AVAV} = 10\text{ ns}$ MCM6946-12: $t_{AVAV} = 12\text{ ns}$ MCM6946-15: $t_{AVAV} = 15\text{ ns}$	$I_{SB1}$	55 50 50 45	mA
CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2\text{ V}$ , $V_{in} \leq V_{SS} + 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$ ) ( $V_{CC} = \text{Max}$ , $f = 0\text{ MHz}$ )		$I_{SB2}$	20	mA

**CAPACITANCE** ( $f = 1.0\text{ MHz}$ ,  $dV = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	
Input Capacitance	All Inputs Except Clocks and DQs $C_{in}$ $C_{ck}$	4 5	6 8	pF	
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

**AC OPERATING CONDITIONS AND CHARACTERISTICS**  
 ( $V_{CC} = 3.3\text{ V} - 5\%, + 10\%$ ,  $T_A = 0\text{ to } + 70^\circ\text{C}$ , Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V      Output Timing Measurement Reference Level ..... 1.5 V  
 Input Rise/Fall Time ..... 2 ns      Output Load ..... See Figure 1  
 Input Timing Measurement Reference Level ..... 1.5 V

**READ CYCLE TIMING** (See Notes 1 and 2)

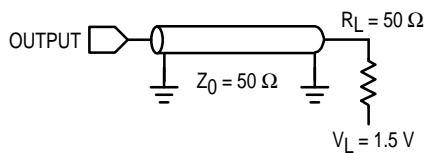
Parameter	Symbol	MCM6946-8		MCM6946-10		MCM6946-12		MCM6946-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	$t_{AVAV}$	8	—	10	—	12	—	15	—	ns	3
Address Access Time	$t_{AVQV}$	—	8	—	10	—	12	—	15	ns	
Enable Access Time	$t_{ELQV}$	—	8	—	10	—	12	—	15	ns	4
Output Enable Access Time	$t_{GLQV}$	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	$t_{AXQX}$	2	—	2	—	2	—	2	—	ns	
Enable Low to Output Active	$t_{ELQX}$	3	—	3	—	3	—	3	—	ns	5, 6, 7
Output Enable Low to Output Active	$t_{GLQX}$	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High-Z	$t_{EHQZ}$	0	4	0	5	0	6	0	7	ns	5, 6, 7
Output Enable High to Output High-Z	$t_{GHQZ}$	0	4	0	5	0	6	0	7	ns	5, 6, 7

**NOTES:**

- $\bar{W}$  is high for read cycle.
- Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
- All read cycle timings are referenced from the last valid address to the first transitioning address.
- Addresses valid prior to or coincident with  $\bar{E}$  going low.
- At any given voltage and temperature,  $t_{EHQZ}\text{ max} < t_{ELQX}\text{ min}$ , and  $t_{GHQZ}\text{ max} < t_{GLQX}\text{ min}$ , both for a given device and from device to device.
- Transition is measured  $\pm 200\text{ mV}$  from steady-state voltage.
- This parameter is sampled and not 100% tested.
- Device is continuously selected ( $\bar{E} \leq V_{IL}$ ,  $\bar{G} \leq V_{IL}$ ).

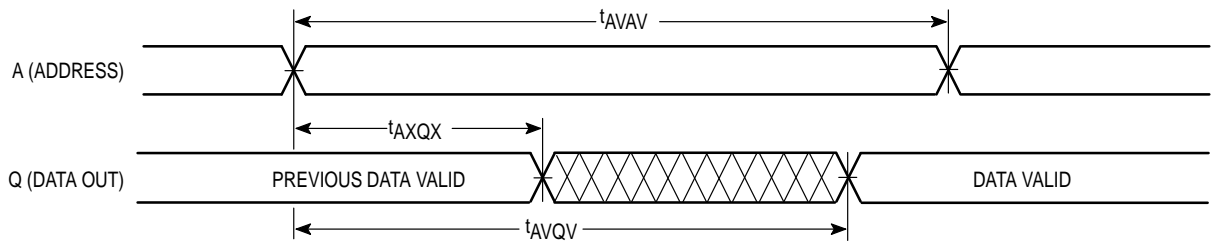
**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

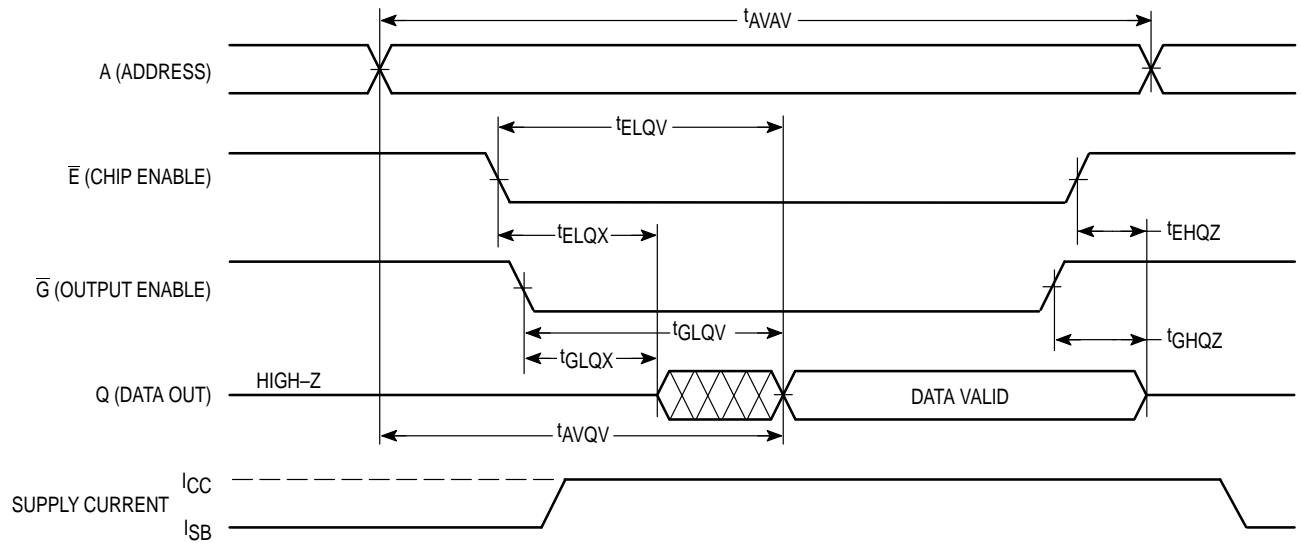


**Figure 1. AC Test Load**

**READ CYCLE 1 (See Note 8)**



**READ CYCLE 2 (See Note 4)**

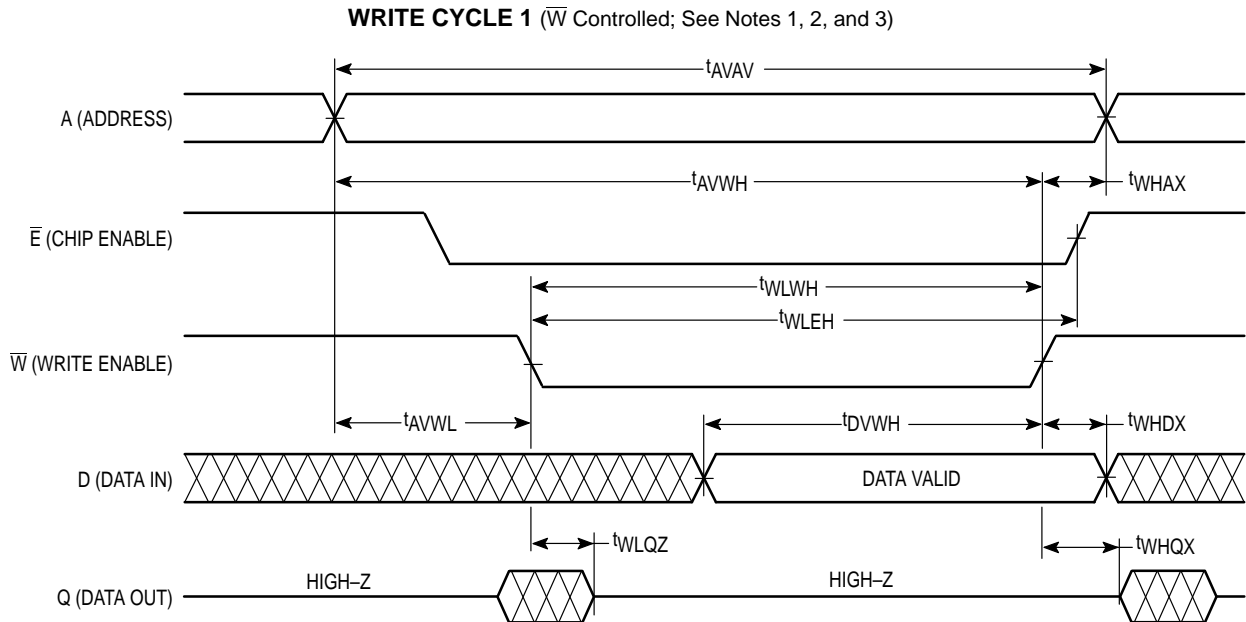


**WRITE CYCLE 1** ( $\overline{W}$  Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6946-8		MCM6946-10		MCM6946-12		MCM6946-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	$t_{AVWL}$	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write ( $\overline{G}$ High)	$t_{AVWH}$	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	$t_{WLWH}$	8	—	9	—	10	—	12	—	ns	
	$t_{WLEH}$										
Write Pulse Width ( $\overline{G}$ High)	$t_{WLWH}$	7	—	8	—	9	—	10	—	ns	
	$t_{WLEH}$										
Data Valid to End of Write	$t_{DVWH}$	5	—	5	—	6	—	7	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	4	0	5	0	6	0	7	ns	5, 6, 7
Write High to Output Active	$t_{WHQX}$	3	—	3	—	3	—	3	—	ns	5, 6, 7
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	0	—	ns	

**NOTES:**

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured  $\pm 200$  mV from steady-state voltage.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature,  $t_{WLQZ} \text{ max} < t_{WHQX} \text{ min}$ , both for a given device and from device to device.





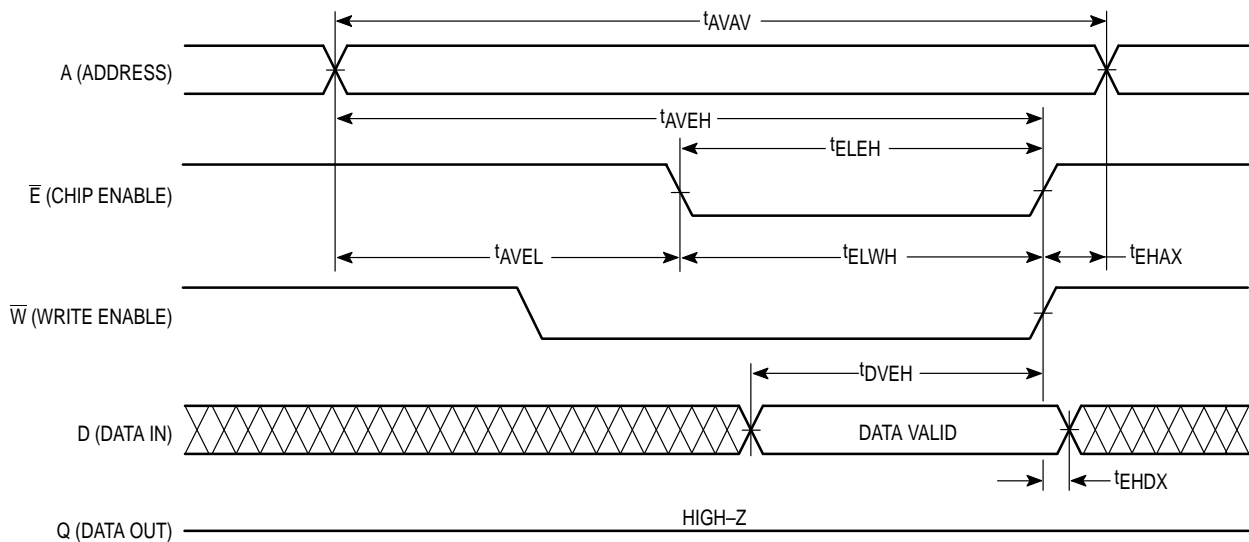
**WRITE CYCLE 2** ( $\bar{E}$  Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6946-8		MCM6946-10		MCM6946-12		MCM6946-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	$t_{AVEL}$	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	7	—	9	—	10	—	12	—	ns	
Address Valid to End of Write ( $\bar{G}$ High)	$t_{AVEH}$	7	—	8	—	9	—	10	—	ns	
Enable Pulse Width	$t_{ELEH}$ , $t_{ELWH}$	8	—	9	—	10	—	12	—	ns	5, 6
Enable Pulse Width ( $\bar{G}$ High)	$t_{ELEH}$ , $t_{ELWH}$	7	—	8	—	9	—	10	—	ns	5, 6
Data Valid to End of Write	$t_{DVEH}$	5	—	5	—	6	—	7	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	0	—	ns	

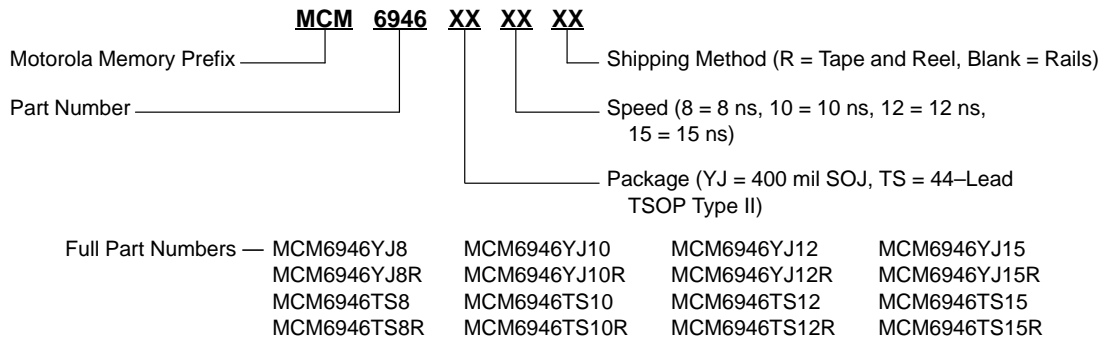
**NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance condition.
6. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high-impedance condition.

**WRITE CYCLE 2** ( $\bar{E}$  Controlled; See Notes 1, 2, and 3)

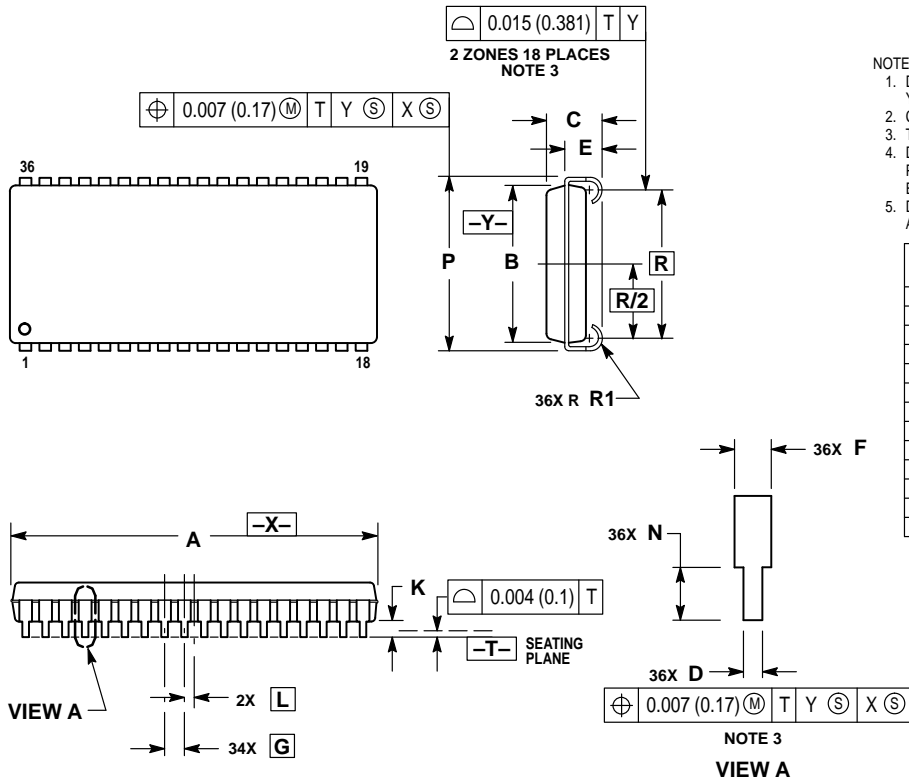


**ORDERING INFORMATION**  
(Order by Full Part Number)



# PACKAGE DIMENSIONS

YJ PACKAGE  
400 MIL SOJ  
CASE 893-02

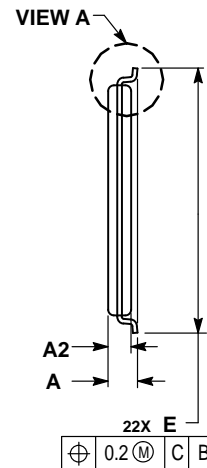
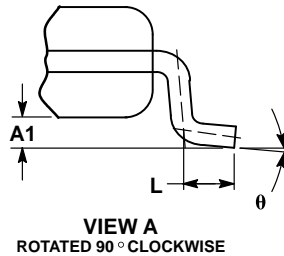
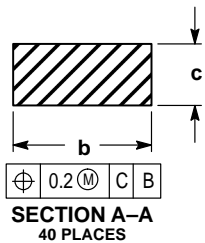
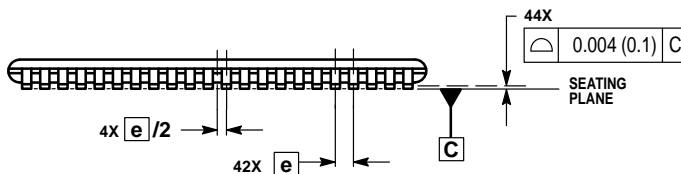
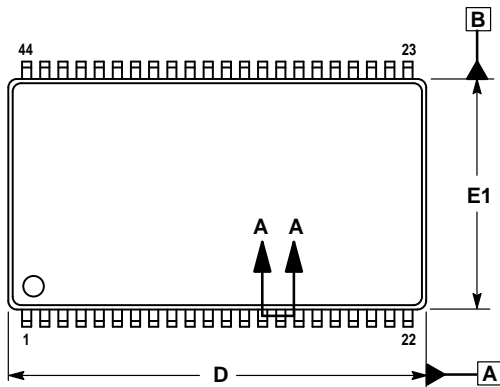


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.25	3.76
D	0.015	0.020	0.38	0.51
E	0.082	—	2.08	—
F	0.026	0.032	0.66	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.55	0.90	1.40
L	0.025 BSC		0.64 BSC	
N	0.035	0.045	0.90	1.14
P	0.435	0.445	11.05	11.30
R	0.370 BSC		9.40 BSC	
R1	0.030	0.040	0.76	1.02

**TS PACKAGE  
44-LEAD  
TSOP TYPE II  
CASE 924A-02**



**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.58.

DIM	MILLIMETERS	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.12	0.21
D	18.28	18.54
e	0.80 BSC	
E	11.56	11.96
E1	10.03	10.29
L	0.40	0.60
$\theta$	0°	5°

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