MAX1546ETL
Rev. A

RELIABILITY REPORT

FOR

MAX1546ETL

PLASTIC ENCAPSULATED DEVICES

May 8, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1546 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1546 is a dual-phase, Quick-PWM™, step-down controllers for Intel IMVP™ CPU core supplies. Dual-phase operation reduces input ripple current requirements and output voltage ripple while easing component selection and layout difficulties. The Quick-PWM control scheme provides instantaneous response to fast load-current steps. The MAX1546 includes active voltage positioning with adjustable gain and offset, reducing power dissipation and bulk output capacitance requirements.

The MAX1546 is intended for two different notebook CPU core applications: stepping down the battery directly or stepping down the 5V system supply to create the core voltage. The singlestage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at a higher switching frequency provides the minimum possible physical size.

The MAX1546 complies with the IMVP-V specifications. The switching regulator features soft-start and power-up sequencing. The MAX1546 also features independent four-level logic inputs for setting the suspend voltage (S0–S1). The MAX1546 includes output undervoltage protection, thermal protection, and voltage regulator power-OK (VROK) output. When any of these protection features detect a fault, the controller shuts down. Additionally, the MAX1546 includes overvoltage protection

The MAX1546 is available in low profile, 40-pin 6mm x 6mm thin QFN packages.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +30V
VCC to GND	-0.3V to +6V
VDD to PGND	-0.3V to +6V
SKIP, SUS, D0–D5 to GND	-0.3V to +6V
ILIM, FB, OFS, CCV, CCI, REF, OAIN+,OAIN- to GND	-0.3V to (VCC + 0.3V)
CMP, CSP, CMN, CSN, GNDS to GND	-0.3V to (VCC + 0.3V)
TON, TIME, VROK, S0–S1 to GND	-0.3V to (VCC + 0.3V)
SHDN to GND (Note 1)	-0.3V to +18V
DLM, DLS to PGND	-0.3V to (VDD + 0.3V)
BSTM, BSTS to GND	-0.3V to +36V
DHM to LXM	-0.3V to (VBSTM + 0.3V)
LXM to BSTM	-6V to +0.3V
DHS to LXS	-0.3V to (VBSTS + 0.3V)
LXS to BSTS	-6V to +0.3V
GND to PGND	-0.3V to +0.3V
REF Short-Circuit Duration	Continuous
Operating Temperature Range	-40°C to +100°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
40-Pin QFN (6 x 6)	1860mW
Derates above +70°C	
40-Pin QFN	23.2mW/°C

Note 1: SHDN may be forced to 12V for the purpose of debugging prototype boards using the no-fault test mode, which disables fault protection and overlapping operation.

II. Manufacturing Information

A. Description/Function:	Dual-Phase, Quick-PWM Controller for IMVP CPU Core Power Supplies
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	11,015
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Thailand and USA
F. Date of Initial Production:	January, 2003

III. Packaging Information

A. Package Type:	**40-Pin QFN (6x6)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0383
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	130 x 172 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6131) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PD38 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1546ETL

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

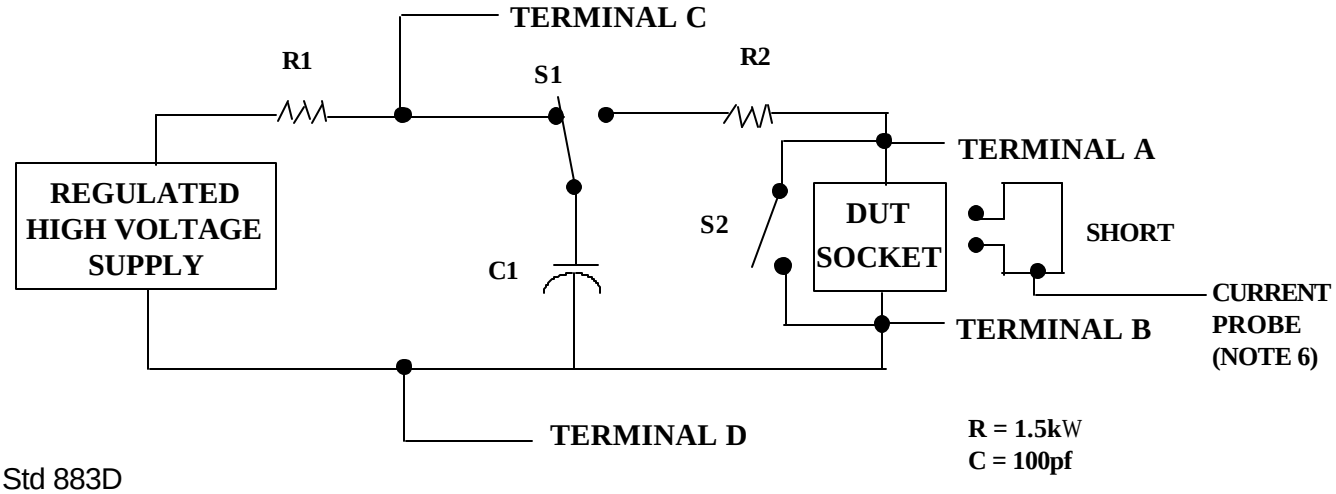
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

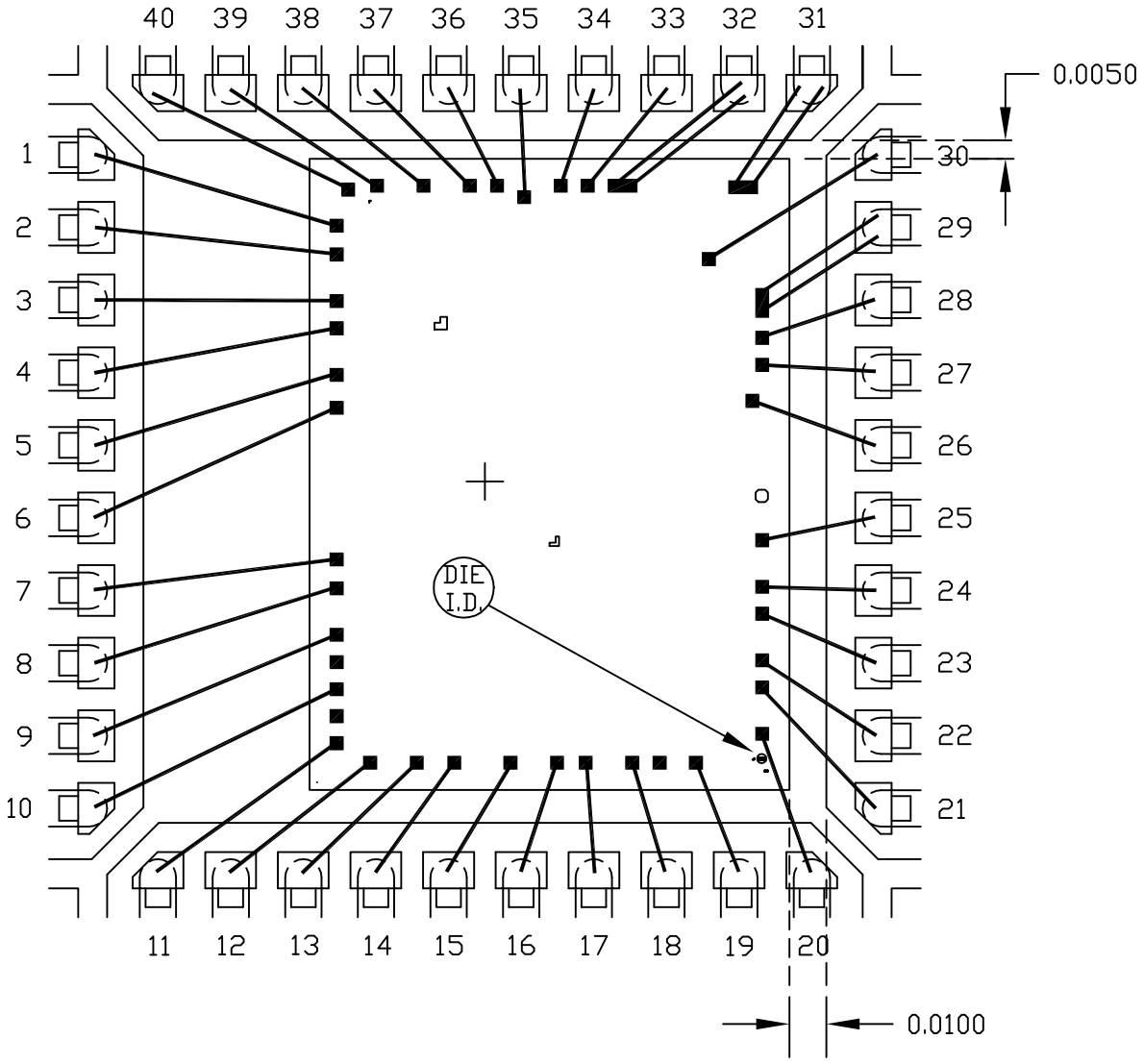
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

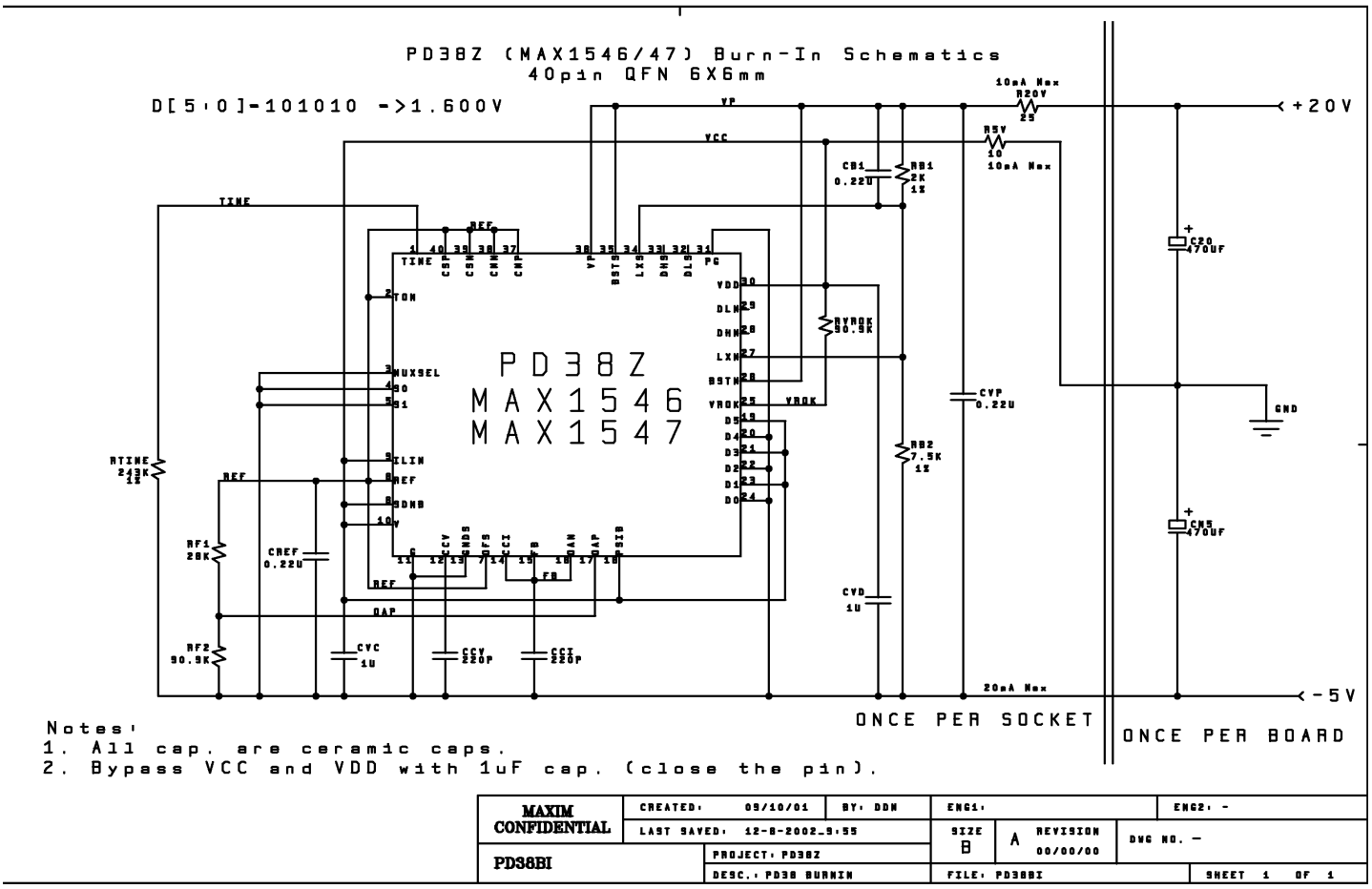


Mil Std 883D
Method 3015.7
Notice 8

6x6x0.8mm QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T4066-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 185x185	PKG.			BOND DIAGRAM #: 05-9000-0383	REV: A
	DESIGN				


PD38Z (MAX1546/47) Burn-In Schematics
40pin QFN 6X6mm
D[5:0]=101010 ->1.600V
+20V
-5V
PD38Z
MAX1546
MAX1547
ONCE PER SOCKET
ONCE PER BOARD
Notes:
1. All cap. are ceramic caps.
2. Bypass VCC and VDD with 1uF cap. (close the pin).
MAXIM CONFIDENTIAL
PD38BI
CREATED: 09/10/01
BY: DDN
LAST SAVED: 12-8-2002_9:55
PROJECT: PD38Z
DESC.: PD38 BURNIN
ENG1:
ENG2: -
SIZE B
A REVISION 00/00/00
DWG NO. -
FILE: PD38BI
SHEET 1 OF 1