HD63140

Universal Pulse Processor (UPP)

Description

The Hitachi HD63140 Universal Pulse Processor is a CMOS peripheral LSI consisting of four independent modules: The universal pulse processor core (UPC), 10-bit A/D converter, 1024-byte RAM, and watchdog timer.

The UPC functions as a programmable pulse I/O module with a 16-bit ALU. It can realize an effective pulse I/O system suitable for versatile applications owing to 16 bit pulse I/O terminals and 24 16-bit universal registers programmable as counter, shifter, compare or capture register. The UPC automatically performs complicated pulse control through the use of 15 commands, which sharply reduces the burden on the MPU. The HD63140 supports an asynchronous bus interface and is easily to connect to the HD6301X, HD6301Y, and HD68HC000 MPUs.

Features

- Universal Pulse Processor Core (UPC)
  - 15 commands for executing pulse I/O operation
  - Up to 16 functions are programmble from the MPU into the function table (RAM)
  - 24 16-bit universal registers (UDR)
  - 16 I/O terminals (8 internal registers for pulse I/O control are also provided)
  - Interrupts can occur at the falling or rising edge of all pulse signals
  - Pulse width resolution is 5 μs when executing 16 commands at 4 MHz operating frequency
- A/D Converter
  - 10-bit $\times$ 10 channels successive approximation A/D converter
  - Scanning operation for up to 4-channels of analog input
  - Interrupts can occur upon completion of conversion
- RAM
  - 1024-byte static RAM
- Watchdog Timer (WDT)
  - Overflow time is selected from 0.128 msec to 131 msec under 4 MHz operation frequency
- Low Power Dissipation
  - Low Power dissipation due to CMOS process
  - Standby mode is available

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Ordering Information

Type No.	Max Operating Frequency	Clock Circuit	On-chip Clock Oscillator	External Clock Operation	Package
HD63140 A00 PS	4.0MHz*	Divide-by-4 Circuit	Yes	Available	64-pin plastic shrink DIP (DP-64S)
HD63140 B00 PS	4.0MHz**	Divide-by-2 Circuit	No	Available	64-pin plastic shrink DIP (DP-64S)
HD63140 A00 CP	4.0MHz*	Divide-by-4 Circuit	Yes	Available	68 pin PLCC (CP-68)
HD63140 B00 CP	4.0MHz**	Divide-by-2 Circuit	No	Available	68 pin PLCC (CP-68)

* 16MHz crystal or 16MHz external clock

** 8MHz external clock

Pin Description

Symbol	Pin No. DP-64S	Pin No. CP-68	Pin Name	I/O
Vcc	12	13	Vcc	I
Vss	1, 21, 49	1, 2, 23, 35, 53	Vss	I
AVcc	61	65	AVcc	I
AVss	50	54	AVss	I
XTAL	3	4	XTAL	I
EXTAL	4	5	EXTAL	I
CLK	2	3	Clock	O
$\overline{RES}$	6	7	Reset	I
$\overline{STBY}$	7	8	Standby	I
D_0-D_7	13-20	15-22	Data bus	I/O
A_0-A_{10}	22-32	24-34	Address bus	I
R/$\overline{W}$	8	9	Read/Write	I
$\overline{DS}$	9	10	Data strobe	I
$\overline{OE}$	5	6	Output enable	I
$\overline{CS}$	10	11	Chip select	I
READY	11	12	Ready	O
$\overline{INT_0}$	64	68	Interrupt 0	O (open drain)
$\overline{INT_1}$	63	67	Interrupt 1	O (open drain)
$\overline{WDTO}$	62	66	Watchdog Timer Out	O (open drain)
U_0/P_{10}-U_{15}/P_{27}	48-33	51-36	U_0/P_{10}~ U_{15}/P_{27}	I/O
AN_0-AN_9	60-51	64-55	Analog input	I

Pin Function

Power Supply

V_{CC}: Power supply pin (+5 V).

V_{SS}: Ground pin: Connect all Vss to ground.

AV_{CC}: Analog power supply pin for A/D converter (+5 V).

AV_{SS}: Ground pin for A/D converter; connect to ground together with V_{SS} (AVss = Vss = GND)

Clock

XTAL, EXTAL: A00: Connect to a crystal whose frequency is four times the operation frequency (16 MHz crystal for 4 MHz operation).

When using an external clock, its frequency should be four times the operation frequency (16 MHz clock for 4 MHz operation), and the XTAL pin must be disconnected.

B00: The frequency of the external clock should be two times that of the internal clock (8 MHz clock for 4 MHz operation), and the XTAL pin must be disconnected.

CLK: CLK outputs a clock signal whose frequency is twice the operation frequency (8 MHz clock for 4 MHz operation).

Reset

$\overline{RES}$: Low level input at $\overline{RES}$ initializes the LSI.

Standby

$\overline{STBY}$: Low level input at $\overline{STBY}$ stops the internal clocks and puts the LSI into standby mode; RAM's data is preserved and other circuits are reset.

MPU Interface

D_0-D_7: 8-bit bidirectional data bus.

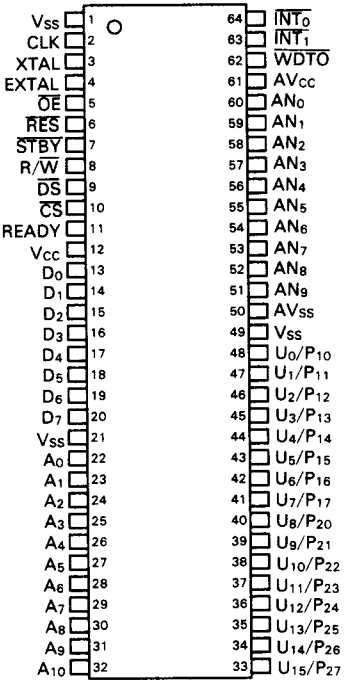
A_0-A_{10}: Address input pins for specifying memory or registers.

R/$\overline{W}$: Controls data transfer direction between UPP and MPU. In general, R/$\overline{W}$ signal output from the MPU is connected to R/$\overline{W}$.

$\overline{DS}$: Read write operation is performed during low level of $\overline{DS}$.

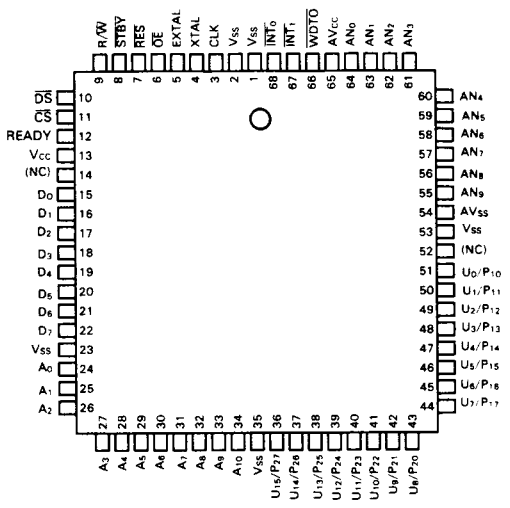
Pin Arrangement

1. 64-pin Plastic Shrink DIP



(Top View)

2. 68-pin PLCC



(Top View)

Note) NC: Non-connected pins; Nothing can be connected to NC pins.

$\overline{OE}$: Controls D_0-D_7 outputs. D_0-D_7 are in high-impedance state during high level of $\overline{OE}$ even in the read cycle.

$\overline{CS}$: Read/write operations to/from memory or registers are performed during low level of $\overline{CS}$. In general, decoded signals for MPU upper addresses are input to $\overline{CS}$.

READY: Inserts a wait cycle for MPU. This is a three-state output. When accessing registers other than RAM, it enters the output state during low level of $\overline{CS}$. Except for this case, it is in high-impedance state.

$\overline{INT_0}$: Logical sum (OR) output of interrupt request registers IRR0-IRR15.

$\overline{INT_1}$: Logical sum (OR) output of interrupt request registers IRR16-IRR23 and interrupt request at the completion of A/D conversion.

WDT Output

$\overline{WDTO}$: Overflow output of watchdog timer.

UPP Input/Output

U_0/P_{10}-U_{15}/P_{27}: UPP pulse I/O pins. They can also be used as an MPU port according to the set data of the UPP contact enable register. Input level of U_0/P_{10}-U_7/P_{17} is TTL, and U_8/P_{20}-U_{15}/P_{27} are Schmitt-trigger inputs.

Analog Input

AN_0-AN_9: Analog input pins for 10-channel A/D converter.

Command Table

Commands		Functions
Counter/Timer, Pulse Input Functions	FRS	Free-Running Counter/Timer with Sampling
		Performs free-running counts and captures the counter at the rising or falling edge of the specified signal.
	INS	Interval Counter/Timer with Sampling
		Counter is captured and reset at the rising or falling edge of the specified signal. (Measures pulse cycle.)
	UDS	Up-Down Counter/Timer with Sampling
		Counter counts upward or downward according to the count direction specification signal, and is captured at the rising or falling edge of the specified signal.
	GTS	Gated Counter/Timer with Sampling
		Clock signal of counter is gated by the specified signal, and the counter is captured and reset at the rising or falling edge of the gate signal.
Counter/Timer, Pulse Output Functions	FRC	Free-Running Counter/Timer witn Compare
		Performs free-running counts, and outputs the result of comparison between compare register data and counter.
	INC	Interval Counter/Timer with Compare
		If counter is the same as the compare register data, pulse is output and counter is reset. (Outputs synchronous pulse.)
	PWC	Pulse Width Counter/Timer with Compare
		Result of comparison between compare register data and counter is output while counter is counting. Counter is reset at the rising or falling edge of the specified signal.
	OSC	One Shot Counter/Timer with Compare
		Counter continuously outputs one-shot pulses from the specified edge of the specified signal until the counter becomes equal to the compare register data.
Special Counter/ Timer Functions	FFC	Fifty-Fifty Duty Cycle Counter/Timer with Compare
		Outputs 50% duty cycle pulse.
	TPC	Two Phase Up-Down Counter
		Increments or decrements counter according to the relation between two-phase pulse signals.
	GTC	Gated Counter/Timer with Compare
		The counter clock signal is gated by the specified signal, and the result of the comparison between compare register data and counter is output. Counter is reset at the specified edge of the gate signal. (Compares pulse width.)
	CTO	Combination Trigger One Shot Counter/Timer
		Counter continuously outputs one-shot pulses, ANDing trigger signal and enable signal until the counter becomes equal to the compare register data.
Shifter and Pulse I/O Functions	SIT	Shift Input
		Input signal is shifted and latched at the specified edge of the specified signal.
	SOT	Shift Output
		Outputs reloaded data, shifting or rotating it. (Outputs scan signal.)
	SPO	Shift Parallel Output
		Outputs reloaded data in parallel, shifting or rotating it.

Internal Registers

Address (HEX)	Register Name	Symbol	R/W	Bit 7	6	5	4	3	2	1	0	Reset Data
000	Data Direction Register 2	DDR2	W									00
001	Data Direction Register 1	DDR1	W									00
002	Port 2 Data Register	PORT2	R/W									*
003	Port 1 Data Register	PORT1	R/W									*
005	Watchdog Timer Register	WDTR	R/W	OVF	WOE	—	MOD	—	OVC2	OVC1	OVC0	08
006	A/D Control and Status Register	ADCSR	R/W	ADEND	ADIE	ADST	SCAN	CH3	CH2	CH1	CH0	00
007	A/D Data Register 0 (H)	ADDR0	R/W	(MSB)								*
008	A/D Data Register 0 (L)	ADDR0	R/W		(LSB)	—	—	—	—	—	—	*
009	A/D Data Register 1 (H)	ADDR1	R/W	(MSB)								*
00A	A/D Data Register 1 (L)	ADDR1	R/W		(LSB)	—	—	—	—	—	—	*
00B	A/D Data Register 2 (H)	ADDR2	R/W	(MSB)								*
00C	A/D Data Register 2 (L)	ADDR2	R/W		(LSB)	—	—	—	—	—	—	*
00D	A/D Data Register 3 (H)	ADDR3	R/W	(MSB)								*
00E	A/D Data Register 3 (L)	ADDR3	R/W		(LSB)	—	—	—	—	—	—	*
00F	RAM Control Register	RAMCR	R/W	RAME	—	—	—	—	—	—	—	FF
010	UPP Contact Enable Register 2	UCER2	W	UCE15	UCE14	UCE13	UCE12	UCE11	UCE10	UCE9	UCE8	00
011	UPP Contact Enable Register 1	UCER1	W	UCE7	UCE6	UCE5	UCE4	UCE3	UCE2	UCE1	UCE0	00
012	UPP Output Register 2	UOR2	W	U15	U14	U13	U12	U11	U10	U9	U8	*
013	UPP Output Register 1	UOR1	W	U7	U6	U5	U4	U3	U2	U1	U0	*
014	Next Data Enable Register	NDER	W									00
016	Next Data Register	NDR	W									*
020	UPP System Control Register	USCR	R/W	TST	TST	TST	TST	—	TST	GFE	UROME	08
021	Maximum Function Number Register	MFNR	R/W	—	—	—	MFN4	MFN3	MFN2	MFN1	MFN0	*
022	Function Number Register	FNR	R/W	—	—	—	FN4	FN3	FN2	FN1	FN0	*
023	**Command Register**	**CMR**	**R/W**	**CMD3**	**CMD2**	**CMD1**	**CMD0**	**OM3**	**OM2**	**OM1**	**OM0**	*
024	**Register Assignment Register A**	**RASRA**	**R/W**	—	—	—	**CTN4**	**CTN3**	**CTN2**	**CTN1**	**CTN0**	*
025	**Register Assignment Register B**	**RASRB**	**R/W**	—	—	—	**CCN4**	**CCN3**	**CCN2**	**CCN1**	**CCN0**	*
026	**I/O Assignment Register A**	**IOARA**	**R/W**	—	**FEDGA**	**FEDGA**	**CPN4**	**CPN3**	**CPN2**	**CPN1**	**CPN0**	*
027	**I/O Assignment Register B**	**IOARB**	**R/W**	—	**FEDGB**	**FEDGB**	**SPN4**	**SPN3**	**CPN2**	**SPN1**	**SPN0**	*
028	**I/O Assignment Register C**	**IOARC**	**R/W**	—	—	—	**LPNA4**	**LPNA3**	**LPNA2**	**LPNA1**	**LPNA0**	*
029	**I/O Assignment Register D**	**IOARD**	**R/W**	—	—	—	**LPNB4**	**LPNB3**	**LPNB2**	**LPNB1**	**LPNB0**	*
02A	Interrupt Enable Register 3	IER3	R/W	IRE23	IRE22	IRE21	IRE20	IRE19	IRE18	IRE17	IRE16	00
02B	Interrupt Enable Register 2	IER2	R/W	IRE15	IRE14	IRE13	IRE12	IRE11	IRE10	IRE9	IRE8	00
02C	Interrupt Enable Register 1	IER1	R/W	IRE7	IRE6	IRE5	IRE4	IRE2	IRE2	IRE1	IRE0	00
02D	Interrupt Request Register 3	IRQR3	R	IRR23	IRR22	IRR21	IRR20	IRR19	IRR18	IRR17	IRR16	00
02E	Interrupt Request Register 2	IRQR2	R	IRR15	IRR14	IRR13	IRR12	IRR11	IRR10	IRR9	IRR8	00
02F	Interrupt Request Register 1	IRQR1	R	IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0	00
030	Interrupt Status Register 3	ISR3	R	IRS23	IRS22	IRS21	IRS20	IRS19	IRS18	IRS17	IRS16	00
031	Interrupt Status Register 2	ISR2	R	IRS15	IRS14	IRS13	IRS12	IRS11	IRS10	IRS9	IRS8	00
032	Interrupt Status Register 1	ISR1	R	IRS7	IRS6	IRS5	IRS4	IRS3	IRS2	IRS1	IRS0	00
033	Interrupt Status Clear Register 3	ISCR3	W	IRSC23	IRSC22	IRSC21	IRSC20	IRSC19	IRSC18	IRSC17	IRSC16	00
034	Interrupt Status Clear Register 2	ISCR2	W	IRSC15	IRSC14	IRSC13	IRSC12	IRSC11	IRSC10	IRSC9	IRSC8	00
035	Interrupt Status Clear Register 1	ISCR1	W	IRSC7	IRSC6	IRSC5	IRSC4	IRSC3	IRSC2	IRSC1	IRSC0	00
036	UPP I/O Register	UIOR	R/W	U23	U22	U21	U20	U19	U18	U17	U16	*
040	UPP Data Register 0 (H)	UDR0	R/W									*
041	UPP Data Register 0 (L)	UDR0	R/W									*
042	UPP Data Register 1 (H)	UDR1	R/W									*
043	UPP Data Register 1 (L)	UDR1	R/W									*
044	UPP Data Register 2 (H)	UDR2	R/W									*
045	UPP Data Register 2 (L)	UDR2	R/W									*
046	UPP Data Register 3 (H)	UDR3	R/W									*

☐ : Function table

* : Undetermined

Note : Reset data of not-used bit is described "1" (which is equal to read data) in this table. Read data of write-only bits is different from reset data described in this table.

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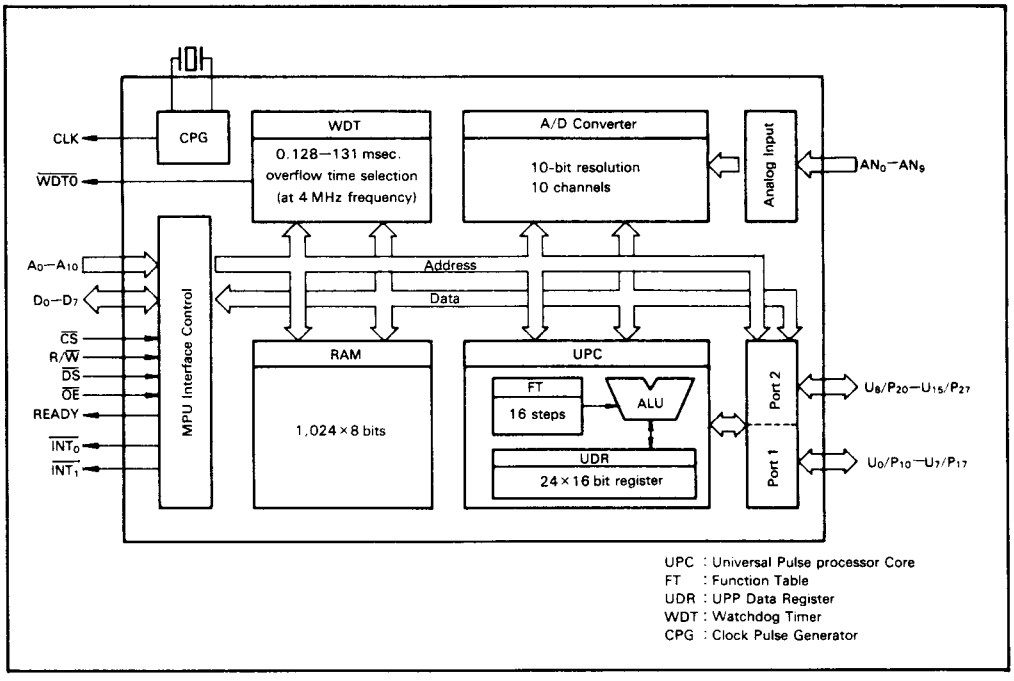
Address (HEX)	Register Name	Symbol	R/W	Bit 7	6	5	4	3	2	1	0	Reset Data
047	UPP Data Register 3 (L)	UDR3	R/W									*
048	UPP Data Register 4 (H)	UDR4	R/W									*
049	UPP Data Register 4 (L)	UDR4	R/W									*
04A	UPP Data Register 5 (H)	UDR5	R/W									*
04B	UPP Data Register 5 (L)	UDR5	R/W									*
04C	UPP Data Register 6 (H)	UDR6	R/W									*
04D	UPP Data Register 6 (L)	UDR6	R/W									*
04E	UPP Data Register 7 (H)	UDR7	R/W									*
04F	UPP Data Register 7 (L)	UDR7	R/W									*
050	UPP Data Register 8 (H)	UDR8	R/W									*
051	UPP Data Register 8 (L)	UDR8	R/W									*
052	UPP Data Register 9 (H)	UDR9	R/W									*
053	UPP Data Register 9 (L)	UDR9	R/W									*
054	UPP Data Register 10 (H)	UDR10	R/W									*
055	UPP Data Register 10 (L)	UDR10	R/W									*
056	UPP Data Register 11 (H)	UDR11	R/W									*
057	UPP Data Register 11 (L)	UDR11	R/W									*
058	UPP Data Register 12 (H)	UDR12	R/W									*
059	UPP Data Register 12 (L)	UDR12	R/W									*
05A	UPP Data Register 13 (H)	UDR13	R/W									*
05B	UPP Data Register 13 (L)	UDR13	R/W									*
05C	UPP Data Register 14 (H)	UDR14	R/W									*
05D	UPP Data Register 14 (L)	UDR14	R/W									*
05E	UPP Data Register 15 (H)	UDR15	R/W									*
05F	UPP Data Register 15 (L)	UDR15	R/W									*
060	UPP Data Register 16 (H)	UDR16	R/W									*
061	UPP Data Register 16 (L)	UDR16	R/W									*
062	UPP Data Register 17 (H)	UDR17	R/W									*
063	UPP Data Register 17 (L)	UDR17	R/W									*
064	UPP Data Register 18 (H)	UDR18	R/W									*
065	UPP Data Register 18 (L)	UDR18	R/W									*
066	UPP Data Register 19 (H)	UDR19	R/W									*
067	UPP Data Register 19 (L)	UDR19	R/W									*
068	UPP Data Register 20 (H)	UDR20	R/W									*
069	UPP Data Register 20 (L)	UDR20	R/W									*
06A	UPP Data Register 21 (H)	UDR21	R/W									*
06B	UPP Data Register 21 (L)	UDR21	R/W									*
06C	UPP Data Register 22 (H)	UDR22	R/W									*
06D	UPP Data Register 22 (L)	UDR22	R/W									*
06E	UPP Data Register 23 (H)	UDR23	R/W									*
06F	UPP Data Register 23 (L)	UDR23	R/W									*
400 to 7FF	RAM		R/W									*

Internal Block Diagram



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Universal Pulse Processor Core (UPC)

Figure 1 shows a block diagram of the UPC. The functions stored in the function table ① are sequentially read by the function number register (FNR), which has a counting function. The UPP control unit ② interprets and executes these functions by controlling the execution unit ③ (consisting of UPP data registers and an ALU) and pulse I/O ④.
HD63140 has a RAM for use as a function table. RAM must be selected by the UPP system control register. The MPU's user program can write functions to the RAM. In addition, read/write to and from all registers in UPC can be performed from the MPU, to monitor the UPC operating condition.
The number of UPP pulse inputs and outputs is 24 (U_0 to U_{23}). Among these, U_0 to U_{15} possess UPP output registers 1 and 2, and pulses can be input and output from external terminals U_0/P_{10} to U_{15}/P_{27}. U_{16} to U_{23} have no input/output terminals, and are only input output to the internal UPP I/O registers.

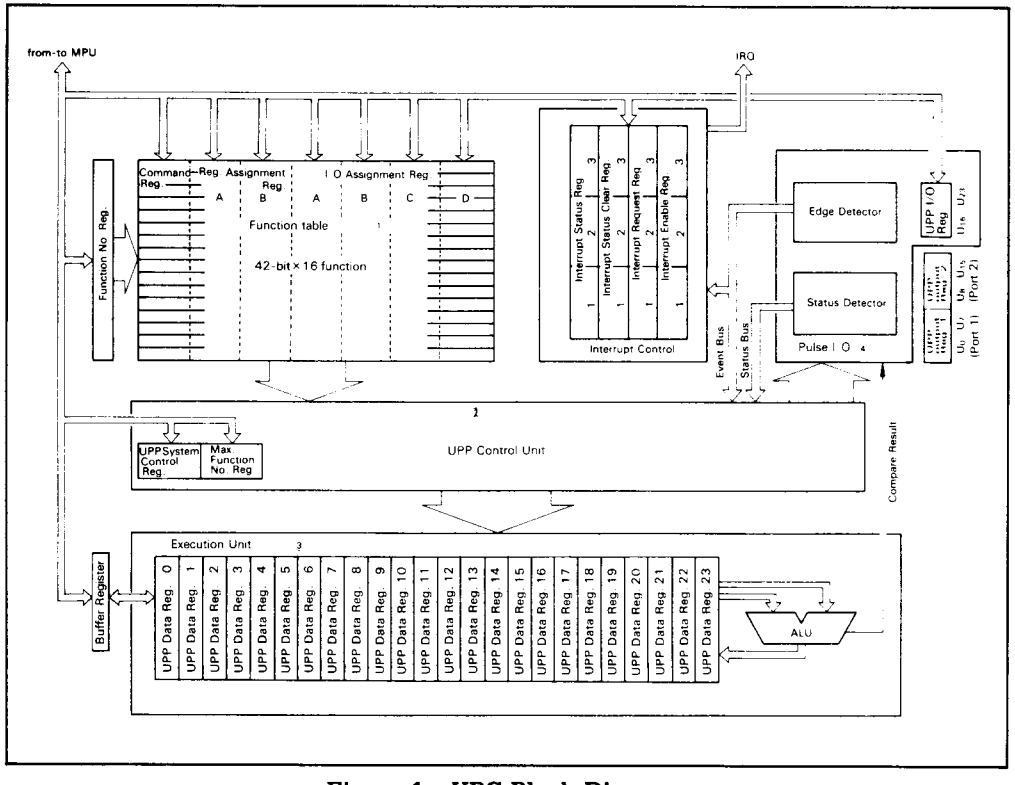

Figure 1. UPC Block Diagram

A/D Converter

Figure 2 shows a block diagram of the UPP's built-in 10-bit succesive approximation A/D converter. It has 10 input channels. The input level of the channel selected by the multiplexer is compared with the output of the 10-bit D/A converter shown. The result is converted bit by bit from the upper bit and fed back to the compare register. When a 10-bit converted result is finally obtained in the compare data registers, this data is output to the A/D data register. Since a scanner is incoporated in the channel selecting circuit of this A/D converter, a maximum of four channels can be scanned, depending on the conditions set in the A/D status and control register. The conversion rate is 42 μs/channel in either single mode or scan mode.

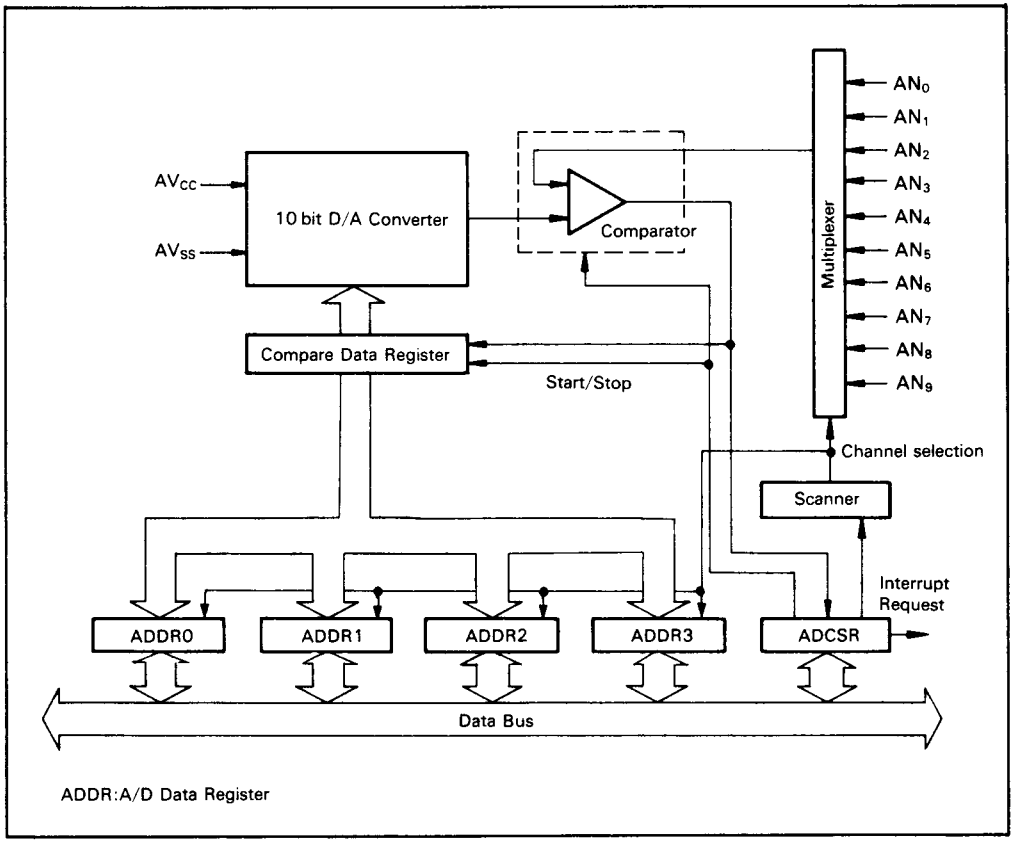

Figure 2. A/D Converter Block Diagram

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Watchdog Timer (WDT)

The watchdog timer consists of a 10-bit prescaler, 8-bit counter, and watchdog timer register (WDTR) as shown in figure 3. The prescaler counts 2 MHz internal clock pulses (4 MHz operation), and outputs the carry to the 8-bit counter. The dividing rate of the prescaler can be specified in 7 steps from 0.128 to 131 ms according to the specified value of the WDTR. The 10-bit prescaler cannot be accessed from external circuits; however, the 8-bit counter can be reset during counting. Usually, this counter is periodically reset by the MPU to prevent overflow. If the 8-bit counter overflows, overflow flag (OVF) of WDTR is set and a low pulse is output for approximately 8.5 μs (4 MHz operation) to the $\overline{\text{WDTO}}$ pin. Accordingly, if this pin is connected to the reset pin of the MPU, the MPU can be reset when it doesn't reset the counter for some reasons like malfunctions. When this timer is used as an interval timer, OVF's inverse signal can be directly output to $\overline{\text{WDTO}}$, specified by WDTR. In this case, when the timer overflows, $\overline{\text{WDTO}}$ holds its output low until OVF is cleared by the MPU reading WDTR.

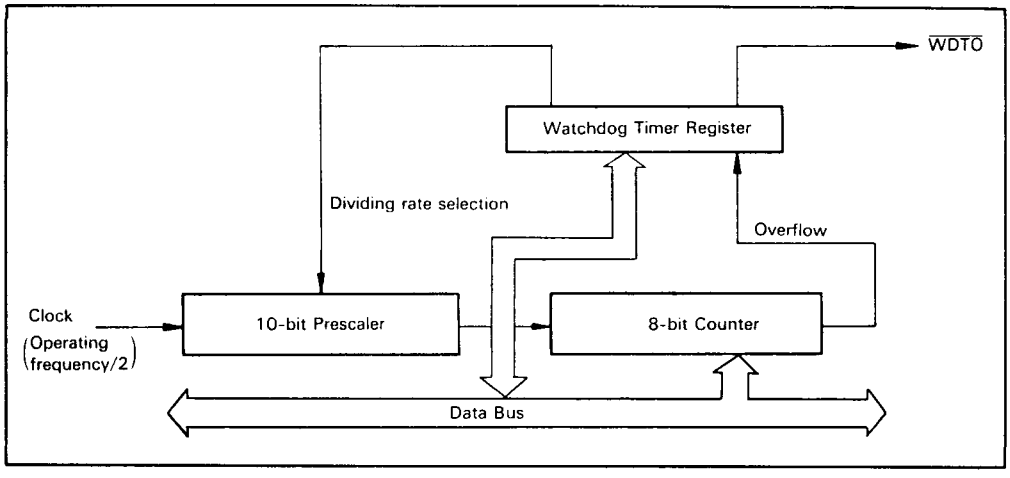

Figure 3. Watchdog Timer Block Diagram

System Block Example

An example of system is shown in figure 4.

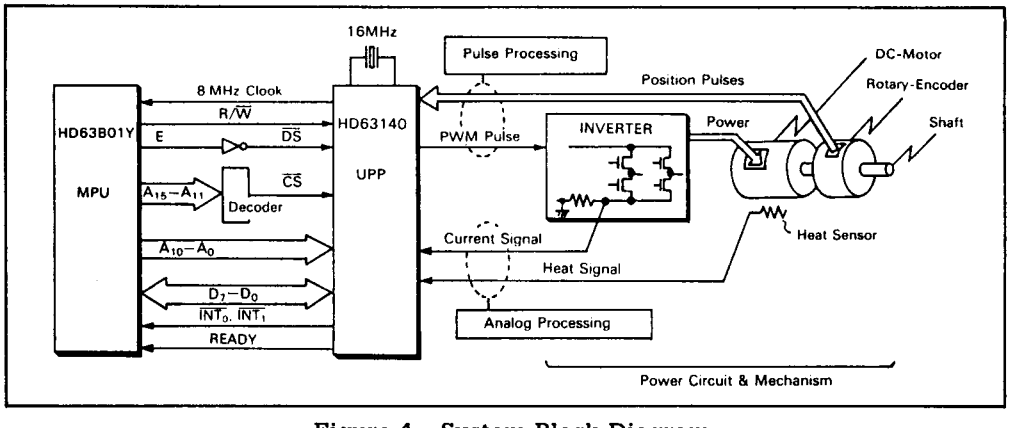

Figure 4. System Block Diagram

UPC, Port 1, and Port 2 Internal Registers

UPP Control Circuit

Maximum Function Number Register (MFNR)

Bit 7	6	5	4	3	2	1	0
–	–	–	MFN4	MFN3	MFN2	MFN1	MFN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 021

Bits 7-5 : Not used

MFN4-MFN0 (Maximum function number): MFN4-MFN0 bits specify the maximum value of the function number register (FNR) which is incremented from 0 during UPC operation. The number of functions to be executed and pulse width resolution are determined by specified values. The relationship between specified values and the number of functions to be executed is shown in table 1. The pulse width resoltion at 4 MHz operation is:

$$(\text{MFNR}) \times \frac{1}{\text{Operating frequency (MHz)}} = (\text{MFNR}) \times 0.25\ \mu s$$

When MFNR is 0, however, the resolution is 8 μs

Table 1. MFNR and Number of Functions to be Executed

MFNR Value (MFNR)	MFN4	MFN3	MFN2	MFN1	MFN0	Number of Functions to be Executed
0	0	0	0	0	0	16
1	0	0	0	0	1	0
2	0	0	0	1	0	1
3	0	0	0	1	1	2
4	0	0	1	0	0	3
5	0	0	1	0	1	4
6	0	0	1	1	0	4
7	0	0	1	1	1	5
8	0	1	0	0	0	6
9	0	1	0	0	1	7
10	0	1	0	1	0	8
11	0	1	0	1	1	8
12	0	1	1	0	0	9
13	0	1	1	0	1	10
14	0	1	1	1	0	11
15	0	1	1	1	1	12
16	1	0	0	0	0	12
17	1	0	0	0	1	13
18	1	0	0	1	0	14
19	1	0	0	1	1	15
20	1	0	1	0	0	16
21	1	0	1	0	1	16
22	1	0	1	1	0	16
23	1	0	1	1	1	16
24	1	1	0	0	0	16
25	1	1	0	0	1	16
26	1	1	0	1	0	16
27	1	1	0	1	1	16
28	1	1	1	0	0	16
29	1	1	1	0	1	16
30	1	1	1	1	0	16
31	1	1	1	1	1	16

Function Number Register (FNR)

Bit 7	6	5	4	3	2	1	0
–	–	–	FN4	FN3	FN2	FN1	FN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 022

Bits 7-5 : Not used

FN4-FN0 (Function number): Function number register (FNR) selects functions from the function table like a program counter. During UPC operation, the FNR is automatically incremented and functions stored in the function table are read and executed sequentially. Note that FNR = 0, 5, 10, or 15 indicates cycles for the MPU to read or write the UPP data register; no functions are executed during these cycles. FNR is reset if its value becomes equal to that specified by MFNR. FNR cannot be accessed by the MPU during UPC operation, but can be when the UPC stops operation. Function numbers from 1 to 4, 6 to 9, 11 to 14, or 16 to 19 are to be specified in this register when programming functions. "UPC operation" means the state in which the GFE bit of the UPP system control register (USCR) is equal to 1.
UPC operation is started from the same FNR value as it has when a 1 is written into the GFE bit. For example, if the data of FNR when a 1 is written into the GFE bit is egual to 1, UPC operation is started from FNR = 1.

UPP System Control Register (USCR)

Bit 7	6	5	4	3	2	1	0
TST	TST	TST	TST	–	TST	GFE	UROME
W	W	W	W		R/W	R/W	R/W

Address: $ 020

TST (Test): Test bits (bit 7-bit 4) are for testing, and cannot be used for user applications; clear to 0s when setting USCR.

Bit 3: Not used

TST (Test): Test bit (bit 2) is also for testing only; clear to 0 when setting USCR.

GFE (General function enable): The UPC is in operation and executes functions when GFE = 1, and is stopped when GFE = 0. This bit is cleared by reset.

UROME (UPP ROM enable): RAM is selected as the function table when UROME = 0, and mask ROM when UROME = 1. This bit is cleared by reset.
Clear to 0 (select RAM) when setting USCR because mask ROM isn't supported.

Function Table

As shown in figure 5, the HD63140 has a RAM as a function table, and the function table consists of a command register (CMR), two blocks of register assignment registers (RASRA, RASRB), and four blocks of I/O assignment registers (IOARA, IOARB, IOARC, IOARD). Each register has 16 registers corresponding to function numbers. First, the registers in the vertical column are selected by setting numbers in FNR; next, the registers in the horizontal column are selected by address inputs. RAM function programming is enabled only when GFE is equal to 0; that is, the UPC is not in operation. (Do not set functions when UPC is in operation.) In this case, values greater than those set in FNR, or 0, must be set in MFNR.

Command Register (CMR):

Bit 7	6	5	4	3	2	1	0
CMD3	CMD2	CMD1	CMD0	OM3	OM2	OM1	OM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 023

CMD3-CMD0 (Command code): CMD3-CMD0 bits specify the command code. Refer to "UPP Commands" for each command description. Also, refer to notes on UPP command setting (1).

OM3-OM0 (Operation mode): OM3-OM0 bits specify the command contents in detail. Refer to "UPP Commands" for details.

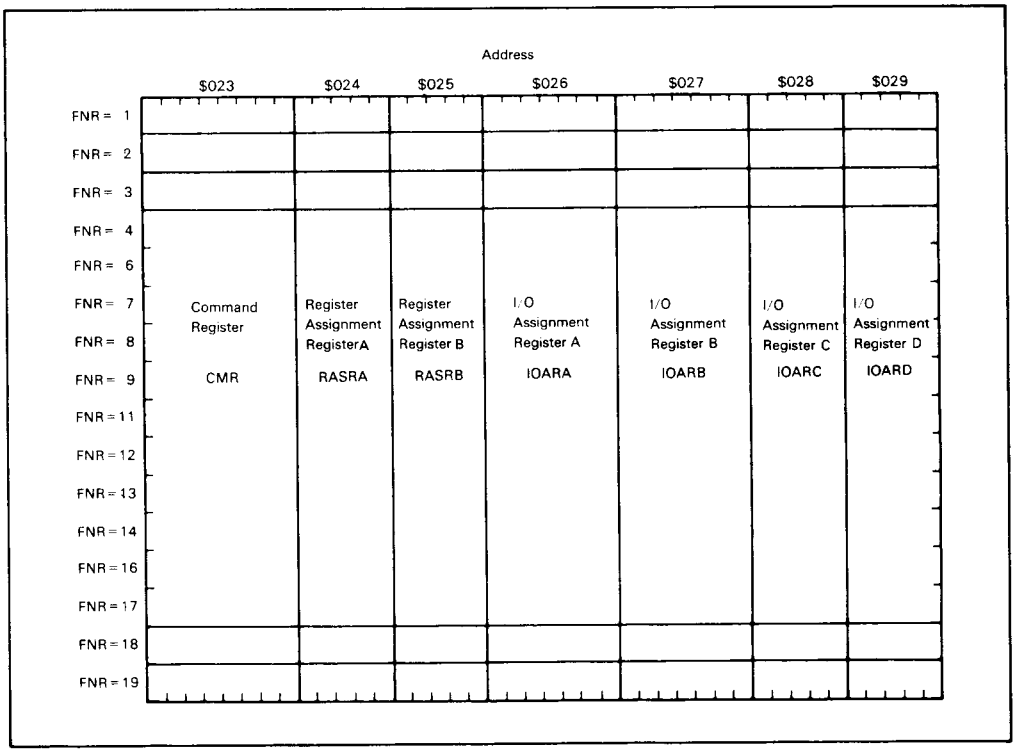

Figure 5. Function Table Configuration

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Register Assignment Register A (RASRA)

Bit 7	6	5	4	3	2	1	0
–	–	–	CTN4	CTN3	CTN2	CTN1	CTN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 024

Bits 7-5 : Not used

CTN4-CTN0 (Counter/timer/shifter no.): CTN4-CTN0 bits specify the number of UPP data register (UDR) (0 to 23) to be used as a counter, timer, or shifter in each function. (A counter counts clocks specified by the I/O assignment register, and a timer counts internal clocks of periodic cycle.) The same register can be specified by other functions.

Register Assignment Register B (RASRB)

Bit 7	6	5	4	3	2	1	0
–	–	–	CCN4	CCN3	CCN2	CCN1	CCN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 025

Bits 7-5 : Not used

CCN4-CCN0 (Capture/compare/reload register no.): CCN4-CCN0 bits specify the UDR number to be used as a capture register, compare register, or data register (shift command) in each function. The register numbers are 0 to 23; however, 24 to 31 are set if these registers are not used. The same register can be specified by other functions. (A register, for example, which is specified as a counter by one function, can be specified as a compare register by another function.)

I/O Assignment Register A (IOARA): This register specifies the clock input pin number as well as the edge direction to define the external clock for a shifter or counter specified by RASRA. This register data is ignored in shift mode by an internal clock and timer mode.

Bit 7	6	5	4	3	2	1	0
–	FEDGA	REDGA	CPN4	CPN3	CPN2	CPN1	CPN0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 026

Bit 7: Not used

FEDGA (Falling edge A): When FEDGA bit is 1, counting or shifting is performed on the falling edge of the signal specified by CPN4-CPN0.

REDGA (Rising edge A): When REDGA bit is 1, counting or shifting is performed on the rising edge of the signal specified by CPN4-CPN0.

When FEDGA and REDGA are both 1, counting or shifting is performed at both edges. When FEDGA and REDGA are both 0, counting or shifting is not performed even if the function is executed.

CPN4-CPN0 (Clock/Shift clock Pin No.): CPN4-CPN0 bits specify the input pin number (0 to 23) of the clock signal for counter or shifter. (No external input/output pins are provided on 16 to 23. The bits of the UPP I/O register, which is one of internal registers, correspond to 16 to 23.)

I/O Assignment Register B (IOARB): This register specifies the pulse input pin number as well as the edge direction for defining sampling pulse, trigger pulse, reset pulse, and data set pulse for the shifter.

Bit 7	6	5	4	3	2	1	0
–	FEDGB	REDGB	SPN4	SPN3	SPN2	SPN1	SPN0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 027

Bit 7: Not used

FEDGB (Falling edge B): When this bit is 1, sampling, triggering, resetting, or setting is performed on the falling edge of the signal specified by SPN4-SPN0.

REDGB (Rising edge B): When this bit is 1, sampling, triggering, resetting, or setting is performed on the rising edge of the signal specified by SPN4-SPN0.

When FEDGB and REDGB are both 1, the above operation is performed at both edges. When they are both 0, the operation is not performed.

SPN4-SPN0 (Sampling/trigger/reset/set pin no.): SPN4-SPN0 bits specify the input pin number (0 to 23)* of the sampling pulse for a capture register, trigger pulse for one-shot pulse output, reset pulse for counter, set pulse for shifter, one pulse signal for two-phase pulse counting, and gate signal.

I/O Assignment Register C (IOARC)

Bit 7	6	5	4	3	2	1	0
–	–	–	LPNA4	LPNA3	LPNA2	LPNA1	LPNA0
			R/W	R/W	R/W	R/W	R/W

Address: $ 028

Bits 7-5 : Not used

LPNA4-LPNA0 (Level pin no. A): LPNA4-LPNA0 bits specify the pulse output pin number (0 to 23).* When no pulses are output, 24 to 31 are specified.
For the TPC and SPO commands, refer to "UPP Commands" in this data sheet.

I/O Assignment Register D (IOARD)

Bit 7	6	5	4	3	2	1	0
–	–	–	LPNB4	LPNB3	LPNB2	LPNB1	LPNB0
			R/W	R/W	R/W	R/W	R/W

Address: $ 029

Bits 7-5 : Not used

LPNB4-LPNB0 (Level pin no. B): LPNB4-LPNB0 bits specify the pulse input pin number (0 to 23)* of direction setting signal for the counter or shiter, the input pin number of gate signal or tigger enable signal, and the input pin number of one pulse signal for two-phase pulse counting.

* No external input/output pins are provided on 16 to 23. The bits of the UPP I/O register, which is one of internal registers, correspond to 16 to 23.

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UPP Data Registers 0-23 (UDR0-UDR23)
UDR, consisting of twenty-four 16-bit registers, can function as counter/timer, shifter, capture, or compare registers according to function settings.
The same register can be specified as referred by several functions.
UDR is accessible by the MPU while both executing functions and suspended via a 16-bit buffer register.
When a MPU write a data to the address of the UDR upper byte, the data is written into the upper byte of the buffer register. When it continuously write a data to the address of the UDR lower byte, the data is written into the lower byte of the buffer register and all the 16 bits data of the buffer register is transferred to the UDR at the same time.
During a read cycle, the reverse operation is performed. When a MPU read the UDR upper byte, all the 16 bits data of the UDR is transferred to the buffer register and then the data in the upper byte of the buffer register is read. When it continuously read the UDR lower byte, the data in the lower byte of the buffer register is read.
In this way, UDR should be read or written in the order of upper byte first and lower byte second.

Address: $40 - $06F

I/O Port

HD63140 has sixteen I/O pins (U_0/P_{10}-U_7/P_{17}, U_8/P_{20}-U_{15}/P_{27}) and an 8-bit UPP I/O register (UIOR) for pulse input and output. As shown in figure 6, these I/O pins are connected with UPP output registers (UOR1, UOR2), port data registers (Port1, Port2), UPP contact enable registers (UCER1, UCER2), and data direction registers (DDR1, DDR2). These pins can also be used as an MPU I/O port. In addition, U_8/P_{20} to U_{15}/P_{27} are connected with next data register (NDR) and next data enable register (NDER), and data set in NDR can be output at a certain timing. UIOR can be used when external output is not necessary like when using the output of one function as input for another function.
The block structure of the registers is shown in figure 7.

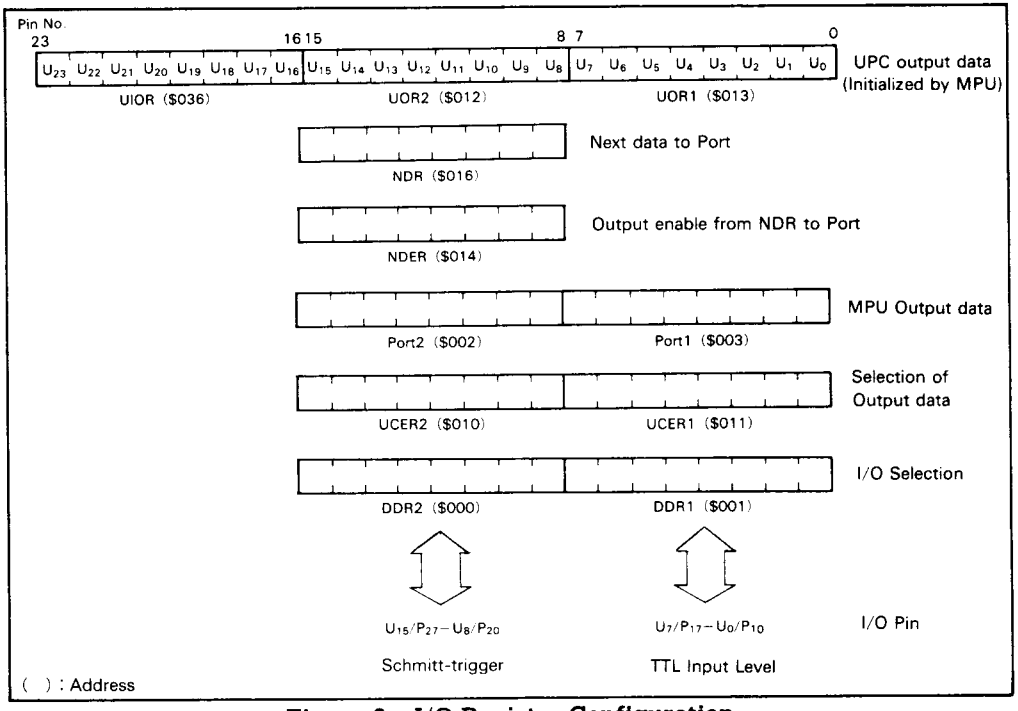

Figure 6. I/O Register Configuration

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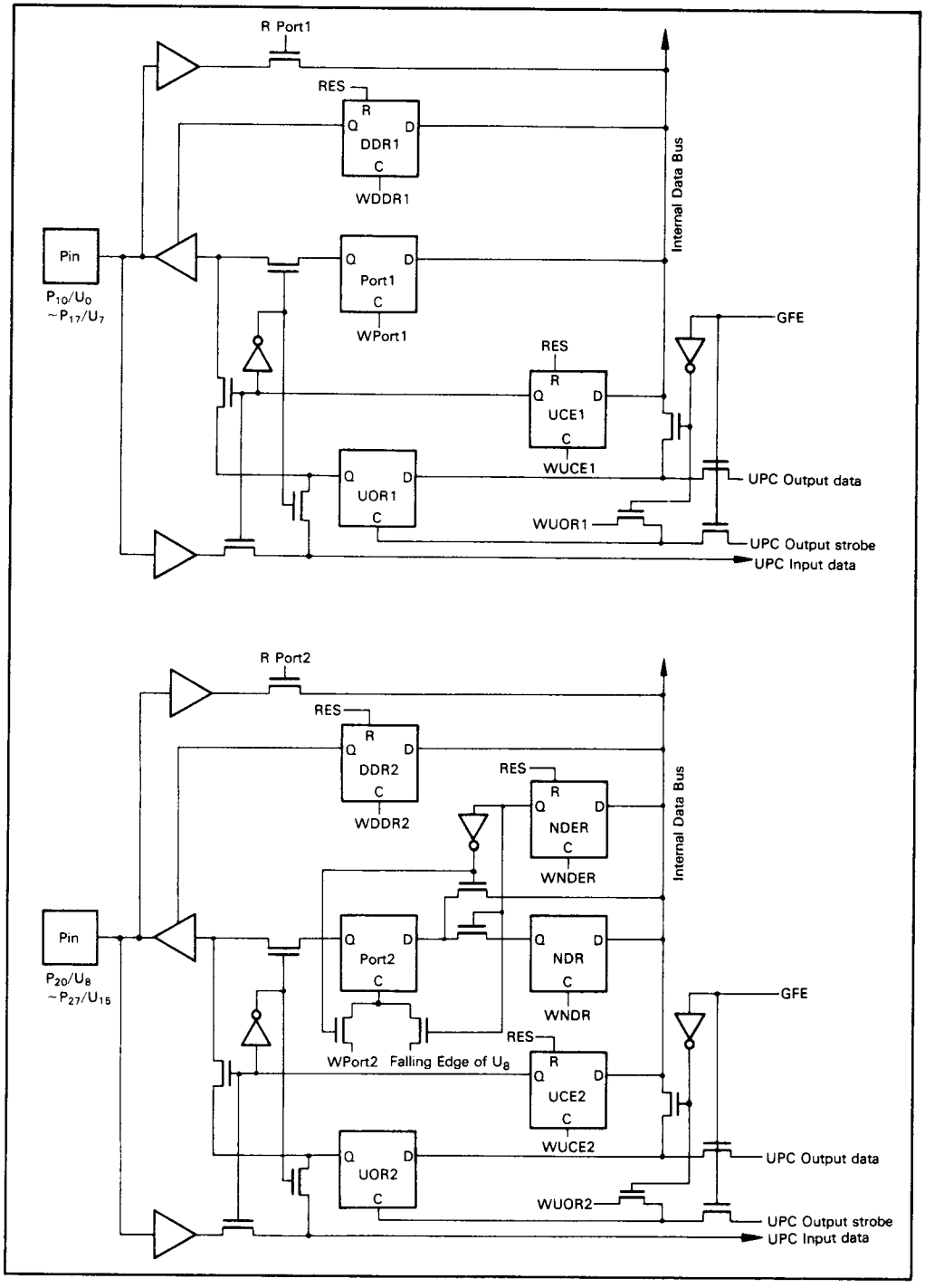

Figure 7. Block Configuration of I/O Resisters

Data Direction Register 1, 2 (DDR1, DDR2): DDR1, DDR2 specify data direction of the corresponding bits of a port. Data is output when the bit is 1, and input when 0. DDR1 and DDR2 are cleared by reset.

UPP Output Register 1, 2 (UOR1, UOR2): During UPC operation, these registers cannot be accessed by the MPU since data are being stored here by the UPC. However, while the UPC is stopped, they are write accessible by the MPU. After reset, this register value is indefinite and should be initialized before setting GFE as required. These registers cannot be read directly during both operation and suspension of the UPC.

UPP I/O Register (UIOR): As the UPP I/O register has no external input/output pins, pulses cannot be input to or output from it. However it can be used for relay when the output of one function is used as the input of another function. This register is accessible by the MPU both while executing and suspending UPC operation, but when UPC is in operation, the bit specified as output of UPC cannot be set by the MPU.
After reset, this register value is indefinite and should be initialized before setting GFE as required.

Port Data Register 1, 2 (Port1, Port2): These are output data registers when I/O pins are used as an MPU port. Reading the port data registers address returns the input output value of the pins.

UPP Contact Enable Register 1, 2 (UCER1, UCER2): UCER1, UCER2 determine whether I/O pins are used as pulse I/O pins of the UPC or as I/O ports of the MPU in bit units.

(1) Setting a UCE bit to 1 specifies the corresponding pin as a pulse I/O pin of the UPC. The corresponding contents of UOR are output onto this pin when DDR=1. If this pin is specified as an input pin of the UPC, I/O value of the pin is input regardless of DDR.

(2) When a UCE bit is 0, the corresponding pin is specified as I/O pins of the MPU port. The corresponding contents of port data register are output onto this pin when DDR=1. UOR is now separated from the pin, but can be used as an I/O register of the UPC. If this pin is specified as an input pin of the UPC, the values of UOR1 and UOR2 are input.

Next Data Register (NDR): The next data register is write-enabled from the MPU. It is used when data, which was set in advance, is output in a certain timing. NDR value is output to port 2 upon transition of bit 0 of UOR2 from 1 to 0, when the next data enable register (NDER) is 1.

Next Data Enable Register (NDER): The next data enble register determines bit by bit whether or not data in NDR is output to port 2. When a bit is 1, the corresponding data in NDR can be output to port 2, and the corresponding bit of port 2 cannot be set by the MPU. When 0, it functions as a standard port, and the NDR value is not output to port 2.

Interrupt Request

The UPC can post interrupt requests at the edge of input/output pulse U_0-U_{23}. As shown in figure 8, interrupt processing is controlled by the following four sets of registers: interrupt status registers (ISR1-ISR3), interrupt enable registers (IER1-IER3), interrupt request registers (IRQR1-IRQR3), and interrupt status clear register (ISCR1-ISCR3). Interrupt requests from pins 0 to 15 are output to $\overline{INT_0}$, and those from pins 16-23 to $\overline{INT_1}$.

Interruput Status Register (ISR1-ISR3): The corresponding bits of this register are set on detecting the edges of pulse signals from U_0 to U_{23}. ISR3 is set at the falling edge of the pulse signal. The upper 4 bits of ISR1 and ISR2 are set at the rising edge of the pulse signal, and lower 4 bits are set at its falling edge. This register is cleared by reset, as well as by setting the interrupt status clear register.

Interrupt Enable Register (IER1-IER3): IER1-IER3 enables or disables interrupt requests. An interrupt is generated if the corresponding bit of the interrupt status ragister is set when this register bit is 1, and it is masked when it is 0. This register is cleared by reset.

Interrupt Request Register (IRQR1-IRQR3): IRQR1-IRQR3 is set by a logical AND of the interrupt status register and the interrupt enable register. Interrupt request is allowed by logical OR between each bit of this register as shown in figure 9.

Interrupt Status Clear Register (ISCR1-ISCR3): ISCR1-ISCR3 clears the interrupt status registers. The corresponding bits of the interrupt status register are cleared by writing a 0 into this register. When a 1 is written into this register, the data of the corresponding bits of the interrupt status register are held.

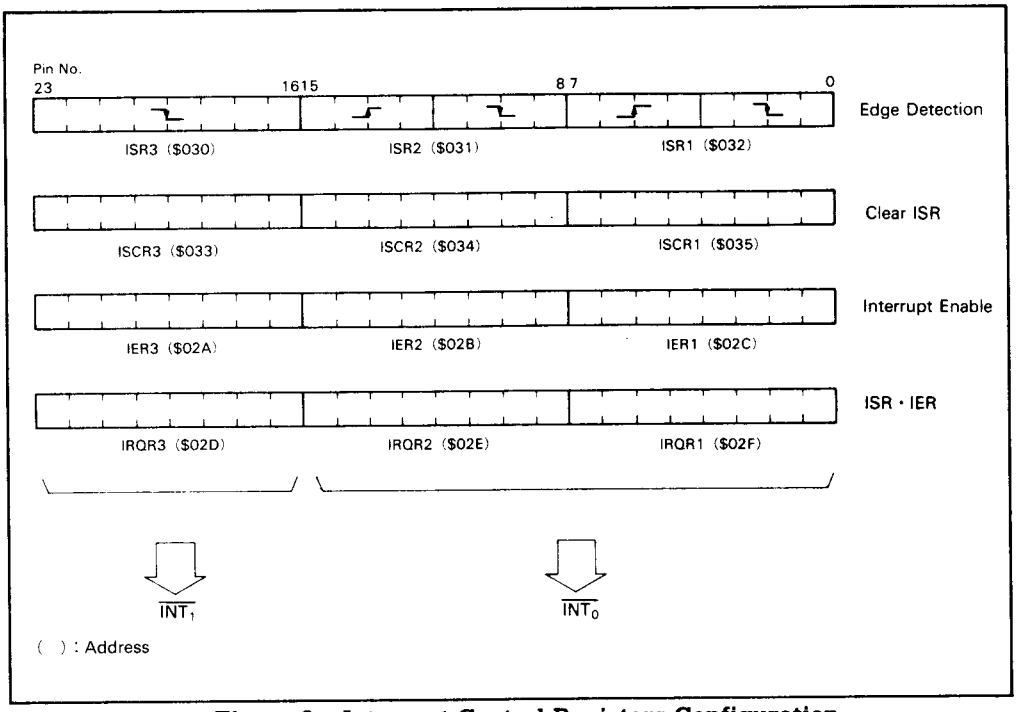

Figure 8. Interrupt Control Registers Configuration

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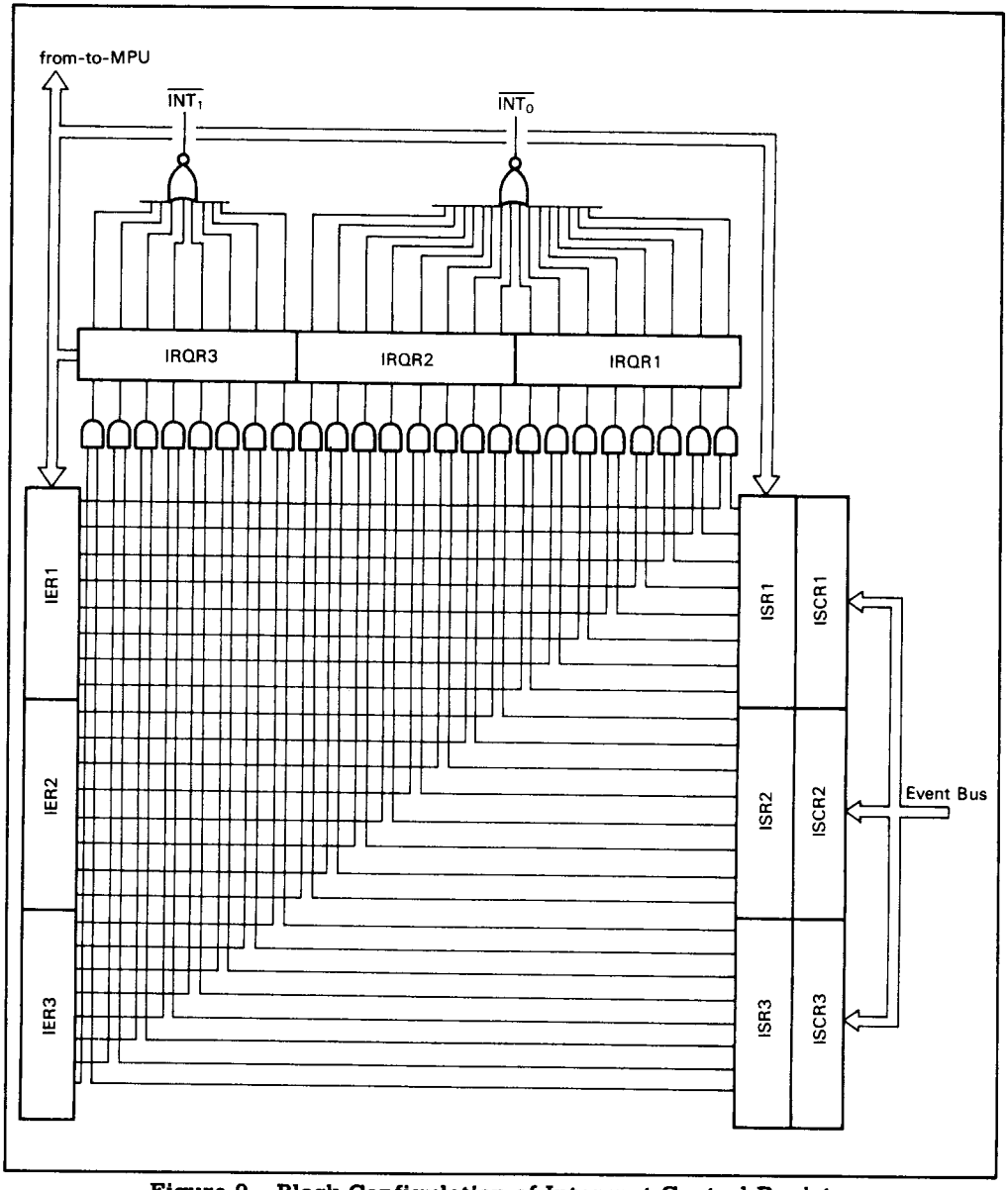

Figure 9. Block Configulation of Interrupt Control Registers

A/D Converter Internal Registers

A/D Control Status Register (ADCSR)

Bit 7	6	5	4	3	2	1	0
ADEND	ADIE	ADST	SCAN	CH 3	CH 2	CH 1	CH 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 006

ADEND (A/D end): The ADEND bit is set to 1 upon completion of A/D conversion. In scan mode, it is set to 1 when the first A/D conversion of all the selected channels is completed. It is cleared by reading ADDR after reading ADCSR, or by writing a 0 into this bit. This bit cannot be written with a 1.

ADIE (A/D interrupt enable): The ADIE flag enables an interrupt request. Interrupt request ($\overline{INT_1}$) is generated by setting ADEND if this bit is set to 1, and is masked if it is 0. This bit is cleared by reset.

ADST (A/D start): Writing a 1 into this bit starts A/D conversion. It remains 1 during conversion, and in single mode, it is cleared upon conversion completion. In scan mode, conversion is started by setting this bit, and continues until this bit is cleared by the MPU. Writing a 1 again during conversion restarts A/D conversion from the beginning.

SCAN (Scan mode selection): Scan mode is selected when this bit is 1, and single mode when 0. In single mode, A/D conversion of the selected channel is executed only once. In scan mode, conversion of all the selected channels is sequentially continued until the ADST bit is cleared. These bits are cleared by reset.

CH3-CH0 (Channel selection): The CH3-CH0 bits select an analog input channel. The relationship between these bits and selected channels in single and scan mode is shown in table 2. These bits are cleared by reset.

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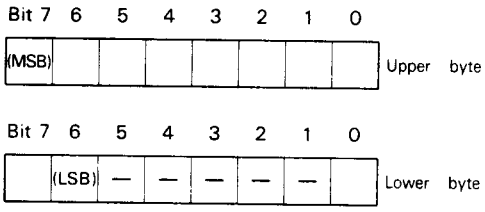
A/D Data Register (ADDR0-ADDR3)



The result of A/D conversion is set in the A/D data register. It consists of 2 bytes. The upper 8 bits of 10-bit A/D conversion data are set in the ADDR's upper byte, and its lower 2 bits are set in the upper 2 bits of ADDR's lower byte, taking 8-bit resolution into consideration. In scan mode, when the upper byte of data is read, the lower byte of data is not updated until the lower byte is read. The UPP possesses four A/D registers so that scanning can be performed for a maximum of four channels. Which channel's conversion result is output to which register is determined in both scan mode and single mode. This relation is shown in table 2. When read, bits 0 to 5 of the ADDR's lower byte are output as 0.

Table 2. Relation between Selected Channel and ADDR in Single and Scan Modes

Mode	SCAN	CH3	CH2	CH1	CH0	ADDR0 ($007, 008)	ADDR1 ($009, 00A)	ADDR2 ($00B, 00C)	ADDR3 ($00D, 00E)
Single Mode	0	0	0	0	0	AN_0	–	–	–
		0	0	0	1	–	AN_1	–	–
		0	0	1	0	–	–	AN_2	–
		0	0	1	1	–	–	–	AN_3
		0	1	0	0	AN_4	–	–	–
		0	1	0	1	–	AN_5	–	–
		0	1	1	0	–	–	AN_6	–
		0	1	1	1	–	–	–	AN_7
		1	0	0	0	AN_8	–	–	–
		1	0	0	1	–	AN_9	–	–
Scan Mode	1	0	0	0	0	AN_0	–	–	–
		0	0	0	1	AN_0	AN_1	–	–
		0	0	1	0	AN_0	AN_1	AN_2	–
		0	0	1	1	AN_0	AN_1	AN_2	AN_3
		0	1	0	0	AN_4	–	–	–
		0	1	0	1	AN_4	AN_5	–	–
		0	1	1	0	AN_4	AN_5	AN_6	–
		0	1	1	1	AN_4	AN_5	AN_6	AN_7
		1	0	0	0	AN_8	–	–	–
		1	0	0	1	AN_8	AN_9	–	–

RAM Internal Resister

RAM Control Register (RAMCR)

Bit 7	6	5	4	3	2	1	0
RAME	–	–	–	–	–	–	–
R/W							

Address: $ 00F

RAME (RAM Enable): Writing 0 to this bit disables access to RAM (address $400-$7FF), preserving RAM data. This is useful when entering the standby mode. This bit is set to 1 by reset.

Bit 6-0: Not used

Watchdog Timer Internal Register

HD63140 is provided with a built-in programmable 8-bit watchdog timer and can monitor the system. This watchdog timer consists of a prescaler, 8-bit counter, and watchdog timer register (WDTR).
When the timer overflows, low is output at $\overline{\text{WDTO}}$ pin.
The 8-bit counter and the watchdog timer register (WDTR) are mapped at the same address. With the first write to this address after reset, data is set in the WDTR, and at the same time, the 8 -bit counter starts counting up. However, with the second or subsequent accesses, data is set in the counter and no data can be written to the WDTR until the counter overflows. When this address is read, WDTR contents are read, and counter contents cannot be read. When the timer overflows, 1 is set in WDTR's OVF bit, and the timer starts counting from 0. When OVF bit is 1, the WDTR can be set again after reading the WDTR. When WDTR read is not performed, not the WDTR but the counter is set.

Bit 7	6	5	4	3	2	1	0
OVF	WOE	–	MOD	–	OVC2	OVC1	OVC0
R	R/W		R/W		R/W	R/W	R/W

Address: $ 005

OVF (Overflow flag): When the 8-bit counter reaches $FF, this bit is set to 1. It is cleared by reset or reading WDTR.

WOE (WDT Output enable): When OVF is 1 with WOE set to 1, low is output from the $\overline{\text{WDTO}}$ pin. When it is 0, no pulse is output. This bit is cleared by reset.

Bit 5: Not used

MOD (Mode): The MOD bit specifies the output method of the overflow signal from the $\overline{\text{WDTO}}$ pin. If the counter overflows when the MOD bit is 0, low is output for approximately 8.5μs (4 MHz operation). When it is 1, the inverse signal of the WDTR's OVF is directly output to the $\overline{\text{WDTO}}$ pin, and low output is held until OVF is cleared by reading the WDTR by MPU.

Bit 3: Not used

OVC2-OVC0 (Overflow cycle): OVC2-OVC0 bits specify the dividing ratio of the 10-bit prescaler, and defines the interval between WDTR setting and counter overflow. The relation between the specified values of OVC2 to OVC0 and overflow time is shown in table 3.

Table 3. Overflow Time of Watchdog Timer (4 MHz operation)

OVC2	OVC1	OVC0	Interval (ms)
0	0	0	131.072
0	0	1	32.768
0	1	0	8.192
0	1	1	2.048
1	0	0	1.024
1	0	1	0.512
1	1	0/1	0.128

4

UPP Commands

Table 5 shows the function format of the UPP. The function consists of command, register assignment, and I/O assignment. In each function, register i functions as a timer, counter, or shifter. In commands other than TPC command, either of internal clock or external clock is selectable as clock for the register i by setting the bit 3 of CMR register.

For each command description in the following pages, an external clock is utilized. In this case, the value of register i is incremented, decremented or shifted upon function execution only when the specified edge of the specified signal is detected.

On the other hand, when an internal clock is utilized, the contents of IOARA defining a clock are ignored. The value of register i is incremented, decremented, or shifted upon every function execution if necessary conditions such as a gate signal are satisfied. Therefore, the apparent internal clock frequency is determined by the interval between executions of the same function which is the inverse of pulse width resolution (refer to MFNR description.)

In commands having pulse output capability, the increment or decrement of register i (which functions as a counter or timer) and the comparision between register i and compare register j are performed at the same time by the ALU. (Comparison is performed between this incremented or decremented value and register j.) Table 4 shows the relation between the value of register i (i), that of j (j), and comparison result CR. Refer to each command description for the relation between CR and output pulses. Reset value of counter or timer is 0 at both incrementation and decrementation.

Table 4. Register Data and Comparison Result

D/$\overline{U}$	Condition	Comparison Result CR
0	(i) < (j)	0
	(i) ≧ (j)	1
1	(i) ≦ (j)	0
	(i) > (j)	1

(i): Register i (counter/timer) data
(j): Register j (compare register) data

Table 5. UPP Function Format

Register	Command Register (CMR)								Register Assignment Register A (RASRA)	Register Assignment Register B (RASRB)	I/O Assignment Register A (IOARA)	I/O Assignment Register B (IOARB)	I/O Assignment Register C (IOARC)	I/O Assignment Register D (IOARD)
Bit / Command	7	6	5	4	3	2	1	0	4 3 2 1 0	4 3 2 1 0	6 5 4 3 2 1 0	6 5 4 3 2 1 0	4 3 2 1 0	4 3 2 1 0
FRS	0	0	0	0	C/$\overline{T}$	D/$\overline{U}$	0	0	i	j	FA RA p	FB RB q	r	–
INS	0	0	0	1	C/$\overline{T}$	D/$\overline{U}$	0	0	i	j	FA RA p	FB RB q	r	–
UDS	0	0	1	0	C/$\overline{T}$	I/$\overline{N}$	0	0	i	j	FA RA p	FB RB q	r	s
GTS	0	0	1	1	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$	i	j	FA RA p	FB RB s	r	s
FRC	0	1	0	0	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$	i	j	FA RA p	– – –	r	–
INC	0	1	0	1	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA RA p	– – –	r	–
PWC	0	1	1	0	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA RA p	FB RB q	r	–
OSC	0	1	1	1	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA RA p	FB RB q	r	–
FFC	1	0	0	0	C/$\overline{T}$	0	0	0	i	j	FA RA p	– – –	r	–
TPC	1	0	0	1	1	I/$\overline{N}$	0	0	i	–	FA RA p	FB RB q	p	q
GTC	1	0	1	0	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$	i	j	FA RA p	FB RB s	r	s
CTO	1	0	1	1	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA RA p	FB RB q	r	s
SIT	1	1	0	0	E/$\overline{I}$	L/$\overline{R}$	0	0	i	j	FA RA p	FB RB q	r	–
SOT	1	1	0	1	E/$\overline{I}$	S2	S1	S0	i	j	FA RA p	FB RB q	r	s
SPO	1	1	1	0	E/$\overline{I}$	S2	S1	S0	i	j	FA RA p	FB RB q	O4 O3 O2 O1 O0	s
NOP	1	1	1	1	–	–	–	–	–	–	– – –	– – –	–	–

C/$\overline{T}$ (CTR/$\overline{TMR}$) : When 0, register i functions as a timer and counts internal clock pulses. When 1, register i functions as a counter and counts the specified direction edge of signal Up.

E/$\overline{I}$ (EXT/$\overline{INT}$) : When 0, register i is shifted according to an internal clock. When 1, register i is shifted at the specified direction edge of external clock signal Up.

D/$\overline{U}$ (DWN/$\overline{UP}$) : When 0, register i functions as an up-counter. When 1, register i functions as a down-counter.

I/$\overline{N}$ (INV/$\overline{NINV}$) : Controls counting direction of a counter. For details, refer to the command description.

H/$\overline{L}$ (HIGH/$\overline{LOW}$) : This bit specifies polarity of output pulse and gate signal. The polarity of the counter overflow signal is not affected by this bit. For details, refer to the command description.

L/$\overline{R}$ (LEFT/$\overline{RIGHT}$) : When 0, register i is shifted to right. When 1, register i is shifted to left.

i : Number of UDR functioning as a counter/timer or shifter.

j : Number of UDR functioning as a capture register, compare register, or data register (shift command).

p : Clock input pin No.

q : Pulse input pin No.

r : Pulse output pin No.

s : Count direction control signal, gate signal, trigger enable signal, or shift direction control signal input pin No.

FA (FEDGA) : Detects falling edge of signal Up when FA = 1.

RA (REDGA) : Detects rising edge of signal Up when RA = 1.

FB (FEDGB) : Detects falling edge of signal Uq or Us when FB = 1.

RB (REDGB) : Detects rising edge of signal Uq or Us when RB = 1.

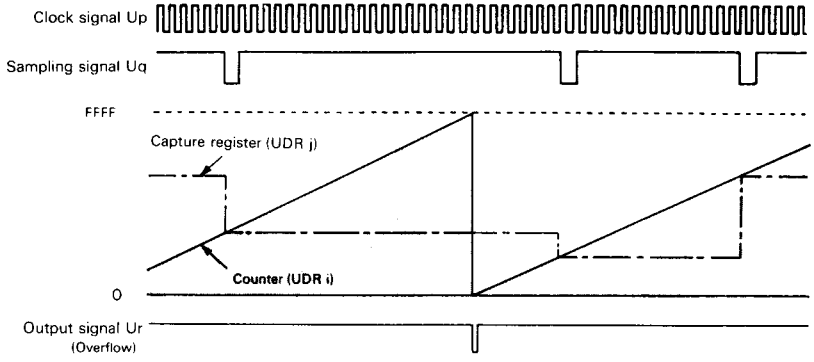
S0–S2, O0–O4 : Specify the shift mode and output method of shift commands. For details, refer to the command description.

4

COMMAND **1. Free-Running Counter/Timer with Sampling (FRS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.
   (Pulse signal counting)

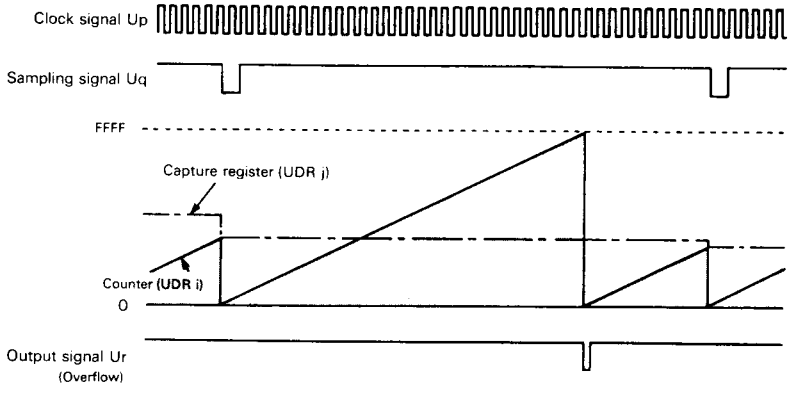
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, FB = 1, RB = 0**



COMMAND **2. Interval Counter/Timer with Sampling (INS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) and register i is reset on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.
   (Pulse signal interval measurement)

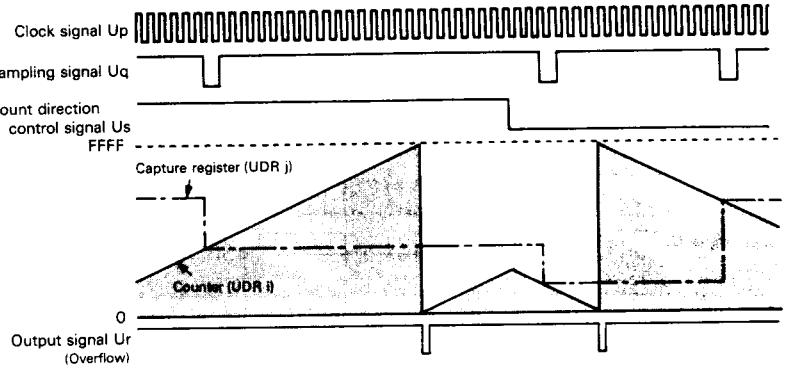
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, FB = 1, RB = 0**



COMMAND **3. Up-Down Counter/Timer with Sampling (UDS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by count direction control signal Us and bit 2 ($I/\overline{N}$) of CMR.
   Incrementation is performed if $I/\overline{N} \oplus Us = 1$, and decrementation if $I/\overline{N} \oplus Us = 0$.
2. Value of register i is set into register j (capture register) on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.

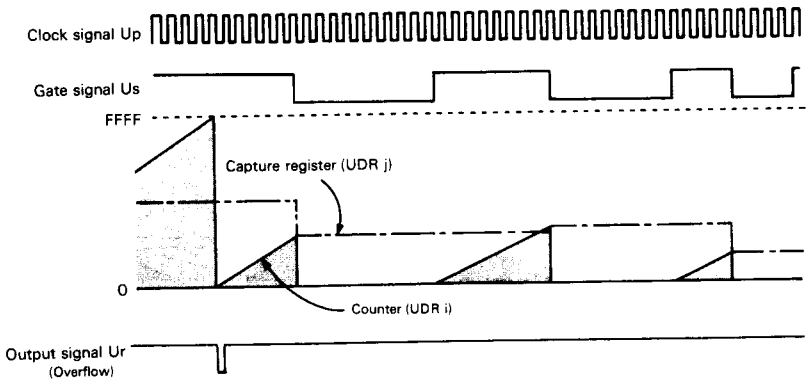
EXAMPLE **Program in Function Table: $C/\overline{T}$ = 1, $I/\overline{N}$ = 0, FB = 1, RB = 0**



COMMAND **4. Gated Counter/Timer with Sampling (GTS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up, when gate signal Us is set as bit 0 ($H/\overline{L}$) of the CMR. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) and register i is reset on detecting at the specified direction edge of signal Uq.
3. Overflow signal of register i is output to Ur.
   (Gate width measurement)

EXAMPLE **Program in Function Table: $C/\overline{T}$ = 1, $D/\overline{U}$ = 0, $H/\overline{L}$ = 1, FB = 1, RB = 0**



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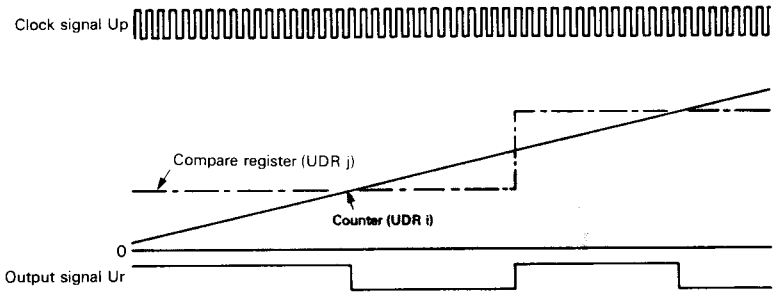
COMMAND **5. Free-Running Counter/Timer with Compare (FRC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Comparison result CR between register i and register j (compare register) is output to Ur. Output level is specified by bit 0 of CMR, and is equal to $\overline{CR \oplus H/\overline{L}}$.

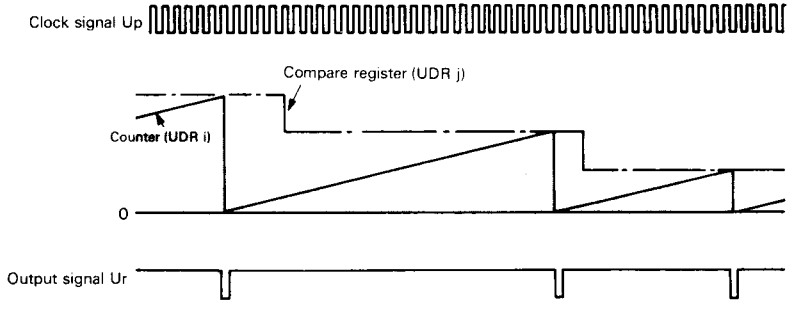
EXAMPLE **Program in Function Table: $C/\overline{T} = 1$, $D/\overline{U} = 0$, $H/\overline{L} = 0$**



COMMAND **6. Interval Counter/Timer with Compare (INC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. When comparison result CR between register i and register j (compare register) is 1, the pulse signal specified by bit 0 of CMR is output to Ur and register i is reset.
   Range of register i is from 0 to (j) − 1 ((j) = the data of register j).
   Output pulse width is equal to pulse width resolution both in timer mode and counter mode.
   (Interval pulse output)

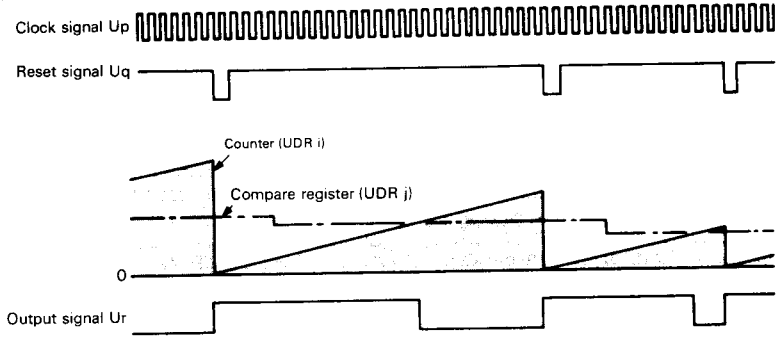
EXAMPLE **Program in Function Table: $C/\overline{T} = 1$, $H/\overline{L} = 0$**



COMMAND **7. Pulse Width Counter/Timer with Compare (PWC)**

1. The inverse of the signal level specified by bit 0 of CMR is output to Ur and register i (counter) is reset on detecting the specified direction edge of reset signal Uq.
2. Register i is incremented on detecting the specified direction edge of clock signal Up.
3. When comparison result CR between register i and register j (compare register) is 1, the output level of Ur is inverted and held until the next reset pulse is input. Register i keeps incrementing while CR=1. It is not reset while CR=0 even if a reset pulse is input.
   (When a reset pulse is input, the output level of Ur is inverted regardless of the value of CR. Accordingly if the value of compare register j is set to 0, the pulse width does not become 0, and a pulse having the same width as the pulse width resolution can be obtained.)

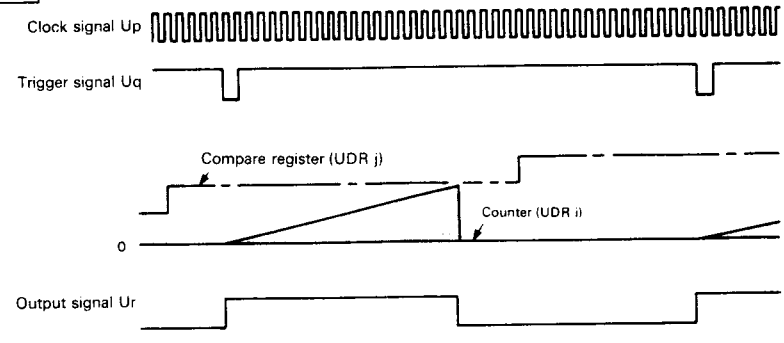
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **8. One Shot Counter/Timer with Compare (OSC)**

1. Counter (UDR i) starts and the inverse of the signal level specified by CMR's bit 0 is output to Ur on detecting the specified edge of trigger signal Uq, and the value of register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparison result CR between register i and register j (compare register) is 1, the output level of Ur is inverted, register i is reset, and this level is held until the next trigger signal is input.
   Even if the next trigger signal is input while CR=0, it is ignored and no trigger takes place. (Similarly to the case of PWC, if the value of compare register j is set to 0, the pulse width does not become 0, and a pulse having the same width as the pulse width resolution can be obtained.)
   (One-shot pulse output)

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



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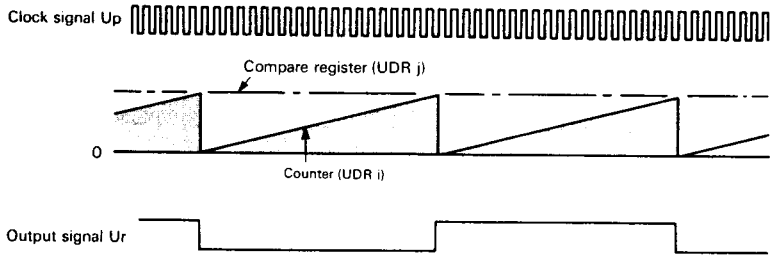
COMMAND **9. Fifty-Fifty Duty Cycle Counter/Timer with Compare (FFC)**

1. Value of register i (counter) is incremeted on detecting the specified direction edge of clock signal Up.
2. When comparison result CR between register i and register j (compare register) is 1, register i is reset and the output level of Ur is inverted.
(50% duty cycle pulse output)

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1**



COMMAND **10. Two Phase Up-Down Counter (TPC)**

Value of register i (counter) is incremented or decremented according to the phase relation between two-phase pulse signals Up and Uq, as shown in table 6. Incrementation or decrementation is determined by the specified value of I/$\overline{N}$.
(Two-phase pulse signal counting)

EXAMPLE **Program in Function Table: I/$\overline{N}$ = 0, FA = RA = FB = RB = 1**

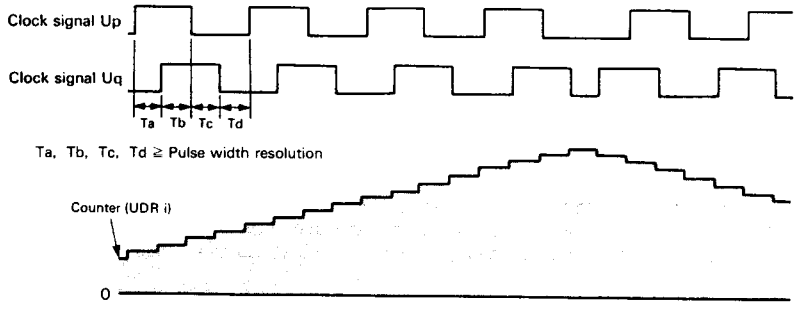


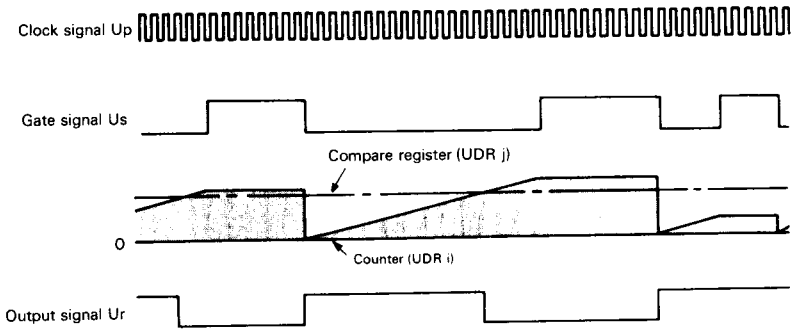
Table 6. TPC Command Function

P	q	Condition	I/$\overline{N}$ = 0	I/$\overline{N}$ = I
↑	0	RA = 1	(i) +1 → (i)	(i) −1 → (i)
1	↑	RB = 1	(Incrementation)	(Decrementation)
↓	1	FA = 1		
0	↓	FB = 1		
↑	1	RA = 1	(i) −1 → (i)	(i) +1 → (i)
1	↓	FB = 1	(Decrementation)	(Incrementation)
↓	0	FA = 1		
0	↑	RB = 1		

COMMAND **11. Gated Counter/Timer with Compare (GTC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up, when gate signal Us is set as specified by bit 0 of the CMR. Incrementation or decrementaion is determined by bit 2 of CMR.
2. Comparison result CR between register i and register j (compare register) is output onto Ur. The output level is specified by bit 0 of CMR, and is equal to $\overline{CR \oplus H/\overline{L}}$.
   Register i is reset at the specified direction edge of the gate signal.
   (Gate width definition)

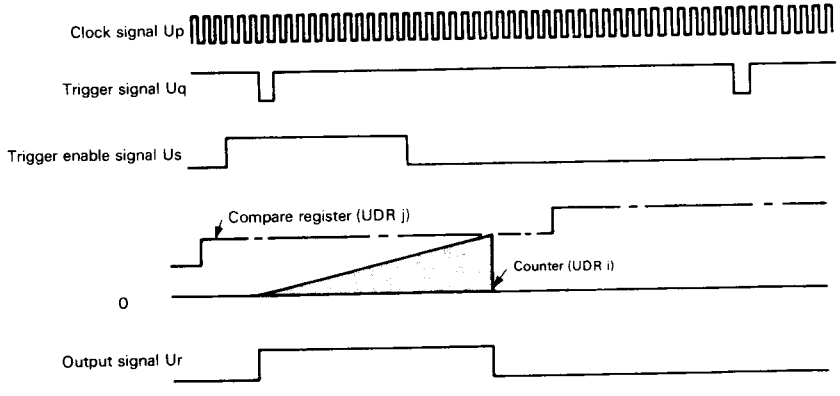
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **12. Combination Trigger One Shot Counter/Timer (CTO)**

1. When trigger enable signal Us is 1, the inverse of the signal level specified by CMR's bit 0 is output to Ur on detecting the specified direction edge of trigger signal Uq, and then register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparision result CR between register i and register j (compare register) is 1, the output level of Ur is inverted, register i is reset, and this level of Ur is held until the next trigger signal is input.
   Even if the next trigger signal is input while CR=0, it is ignored and no trigger takes place.
   (One-shot pulse output with trigger enable)

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



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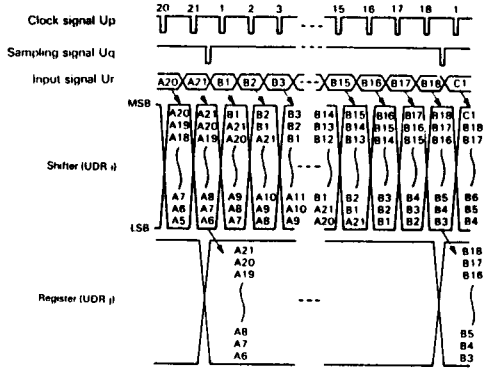
COMMAND **13. Shift Input (SIT)**

1. Value of register i (shifter) is shifted and value of Ur is read to register i on detecting the specified direction edge of clock pulse Up. Shifting direction is determined by bit 2 (L/$\overline{R}$) of CMR.
2. Value of register i is set into register j on detecting the specified direction edge of sampling pulse Uq.
   (Serial input)

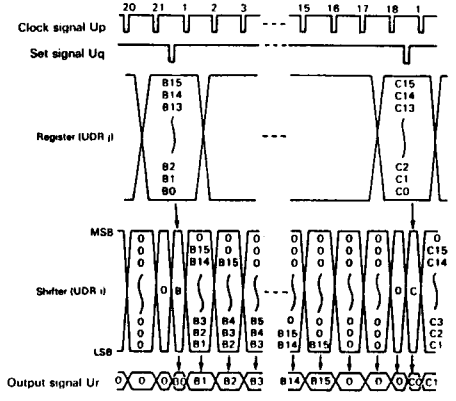
EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, L/$\overline{R}$ = 0, FA = 1, RA = 0, FB = 1, RB = 0**



COMMAND **14. Shift Output (SOT)**

1. Value of register j is set into register i (shifter) on detecting the specified direction edge of set signal Uq.
2. Value of register i is shifted or rotated, and the shift output value is presented onto Ur on detecting the specified direction edge of clock signal Up.
   Mode for shift and rotation is determined by bits 2-0 of CMR as shown in table 7.
   The direction of rotation can be specified by shift direction control signal Us in certain modes as shown in table 7.
3. When S2(CMR's bit 2)=0, the LSB of register i is output to Ur, while S2=1, the MSB of register i is output to Ur.

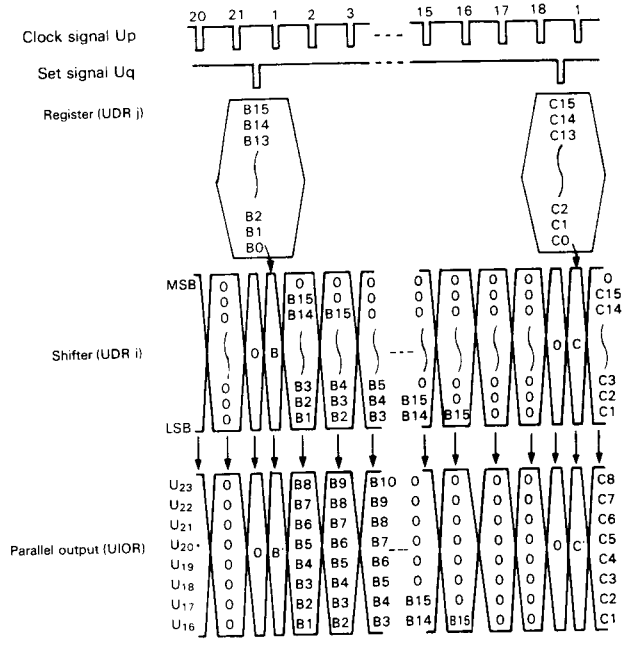
EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, S0 = S1 = S2 = 0, FA = 1, RA = 0, FB = 1, RB = 0**



COMMAND **15. Shift Parallel Output (SP0)**

1. Value of register j is set into register i (shifter) on detecting the specified direction edge of set signal Uq.
2. Value of register i is shifted or rotated and the lower 8 bits are output on detecting the specified direction edge of clock signal Up.
   Mode for shift and rotation is determind by bits 2-0 of CMR register as shown in table 7.
   The direction of rotation can be specified by shift direction control signal Us in certain modes as shown in table 7.
3. The lower 8 bits of the shifter are output according to the specification of IOARC. The specification method of the output is described in table 8. O4 determines the output destination, UOR1 or UIOR, and O3 to O0 are output-enable bits in 2-bit units.
   The SPO command cannot be output to UOR2.

EXAMPLE **Program in Function Table: E $\bar{I}$ = 1, SO = S1 = S2 = 0, FA = 1, RA = 0, FB = 1, RB = 0**



Note: B′, C′ are respectively the lower 8 bits of data B and C.

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Table 7. The Relationship between S0 to S2 and Shift or Rotation Mode in the SOT and SPO Commands. (Output to Ur is only for SOT.)

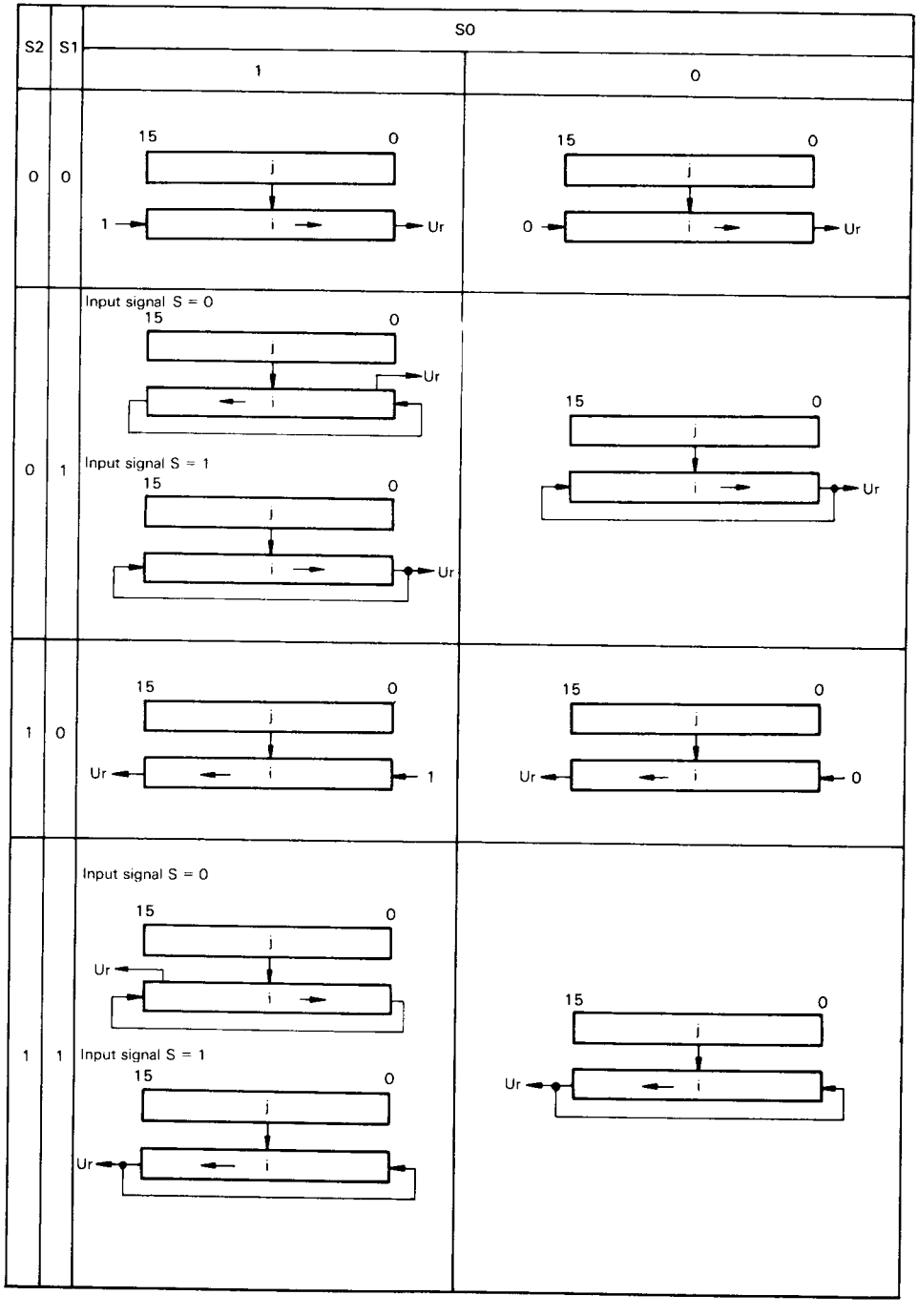


Table 8. Output Destination in the SPO Command

	O4 = 1	O4 = 0
O0 = 1	Shifter bit 0 → U_0	Shifter bit 0 → U_{16}
	Shifter bit 1 → U_1	Shifter bit 1 → U_{17}
O1 = 1	Shifter bit 2 → U_2	Shifter bit 2 → U_{18}
	Shifter bit 3 → U_3	Shifter bit 3 → U_{19}
O2 = 1	Shifter bit 4 → U_4	Shifter bit 4 → U_{20}
	Shifter bit 5 → U_5	Shifter bit 5 → U_{21}
O3 = 1	Shifter bit 6 → U_6	Shifter bit 6 → U_{22}
	Shifter bit 7 → U_7	Shifter bit 7 → U_{23}

Note: If O0 to O3 are 0, the shifter data is not output, and corresponding UOR1 and UIOR bits are not affected by the SPO command.

Notes

Oscillator

The internal clock signal is obtained from the HD63140A00 oscillator by connecting a crystal to XTAL and EXTAL pins or by inputting an external clock to EXTAL pin. The frequency of the crystal or the external clock should be four times that of the internal clock. The oscillator's divide-by-four circuit outputs a system clock signal whose frequency is twice the operation frequency.

Figure 10 shows a crystal connection. An AT-cut parallel resonant crystal should be used. Required characteristics of the crystal (Co, Rs) and capacitance (CL_1, CL_2) are listed in the table 9.

As shown in figure 10, routing signal lines adjacent to the oscillator may result in faulty oscillation due to induction, and such a board design should be avoided. In addition, the crystal and capacitor should be positioned adjacent to XTAL and EXTAL pins. An example of board design is shown in figure 11.

When applying an external clock, the XTAL pin must be disconnected. External clock duty cycle must be 50±5%, and high level voltage must be more than $V_{CC} \times 0.7$ V.

The frequency of the external clock must be two times that of the internal clock (8 MHz clock for 4 MHz operation) in HD63140B00. With HD63140B00, clock duty cycle must be 50±5%, and high level voltage must be more than 2.0 V.

4

Table 9. Typical Crystal Characteristics

	Oscillation Frequency		
Item	**4 MHz**	**4 MHz<f≤12.288 MHz**	**12.288 MHz<f≤16 MHz**
Co	<7 pF	<7 pF	<7 pF
Rs	<60Ω	<60Ω	<35Ω
CL_1, CL_2*	10–22 pF±10%	10–22 pF±10%	10 pF±20%

* CL_1, CL_2 contains stray capacity of wired lines.

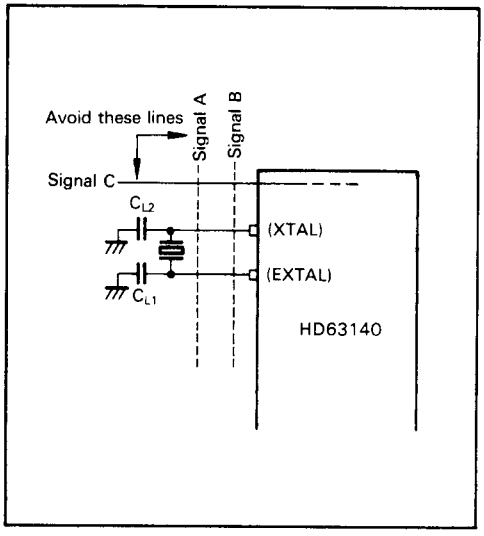


Figure 10. Crystal Connection

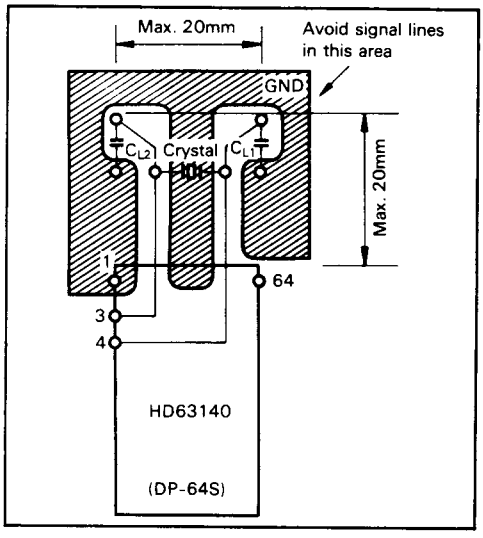


Figure 11. Typical Board Design

Standby Mode

Applying a low level to the $\overline{STBY}$ pin places the HD63140 into standby mode. In standby mode, RAM contents are preserved, all clocks of the HD63140 are inactive, and current dissipation is lowered to 15 μA or less (except for AIcc). All pins except power supply pins (V_{cc}, V_{ss}), $\overline{STBY}$, $\overline{RES}$, and XTAL (outputs low level) are disconnected from internal circuits and the LSI is reset.

HD63140 can return from standby mode by reset start. When entering standby mode with a low level on the $\overline{STBY}$ pin, it does not matter whether the $\overline{RES}$ pin is low or high; however, when returning from standby mode it must be held low until oscillation stabilization. This relationship is shown in figure 12.

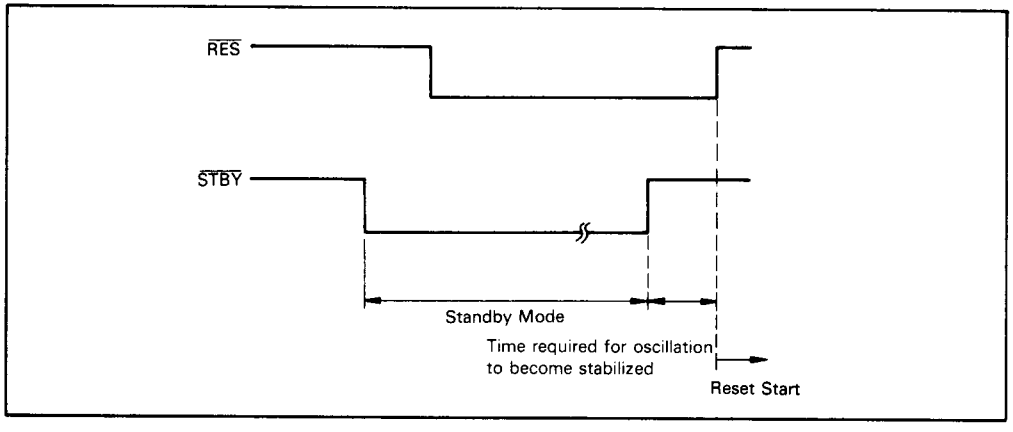


Figure 12. Standby Mode Timing

Notes on using the watchdog timer.

The watchdog timer is undefined at power-on and is not reset until the rising edge of the $\overline{RES}$ signal. Therefore the $\overline{WDTO}$ pin may output a low level while a low level is input to the $\overline{RES}$ pin after power-on.
This may cause your system to stay in the reset state after power-on if the system is constructed as shown in figure A.

Please connect the output of the power-on-reset circuit directly to the $\overline{RES}$ pin of the HD63140 in order to avoid this malfunction (see figure B).

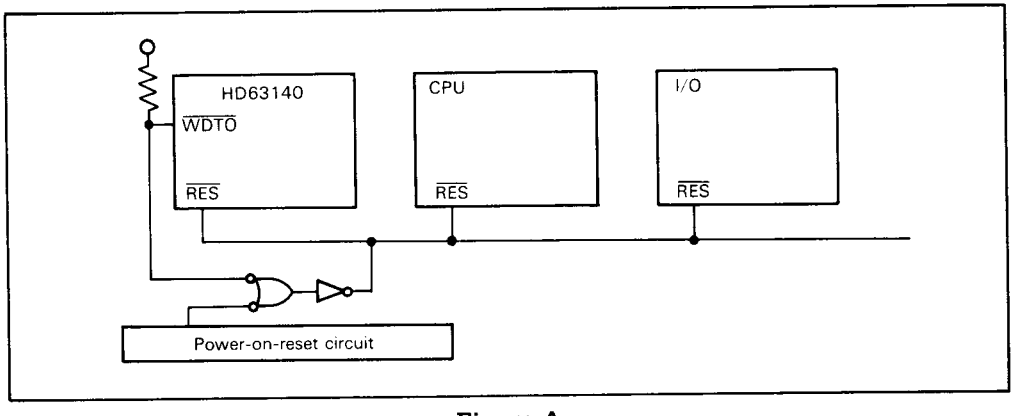


Figure A

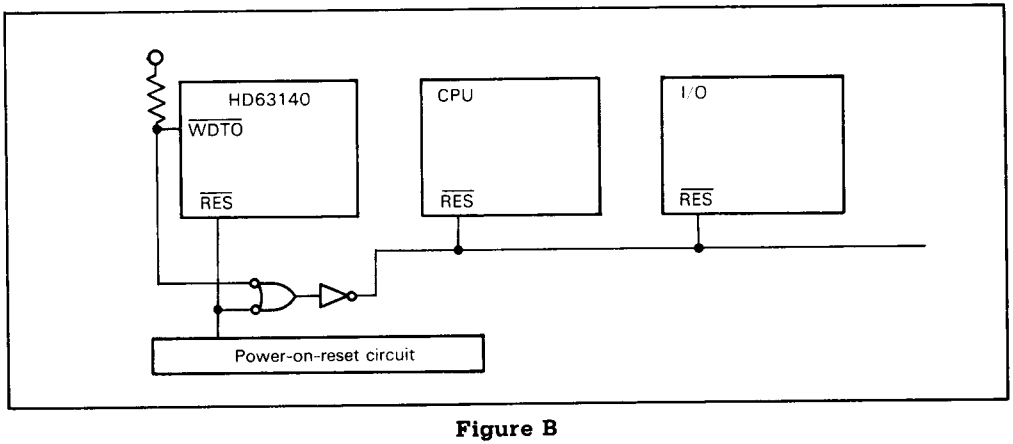


Figure B

4

Notes on UPP Command Setting (1)

The UPP's pulse width resolution depends on the specified value of maximum function number register MFNR: the resolution is inversely proportional to the specified values. Accordingly, to increase resolution, a minimum value should be set in the MFNR according to the number of functions to be executed.

In addition, when a value larger than the necessary minimum value (or 0) is set in MFNR so as to adjust pulse width resolution, set NOP in the command registers (CMR) of unused function numbers in the function table (figure 13). Since the values in the function table after reset are undefined, they may affect the execution of other functions if they are read and executed.

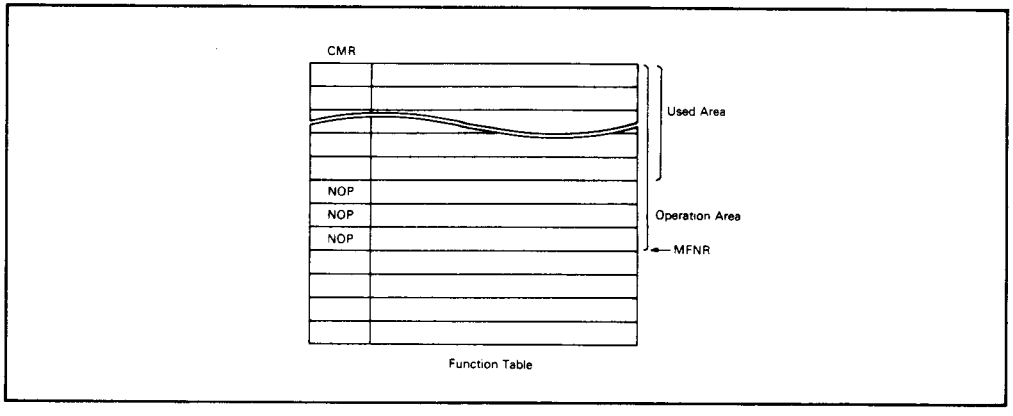


Figure 13. Filling Function Table with NOP

Notes on UPP Command Setting (2)

In the HD63140, an edge detecting cirucit is provided on each pulse input and output of U_0 to U_{23}. Edges are detected by sampling the input and output level and comparing them with the previous sampling value at the timing the function number register (FNR) periodically returns to 0 during UPC operation. Accordingly, while UPC is not in operation, no edges can be detected. In addition, even in operation, narrower pulse edges than the sampling interval cannot be detected (refer to A of figure 14).
Flip-flops for sampling have been cleared by reset. Consequently, as indicated by B of figure 14, if GFE is set while U_0 to U_{23} are 1, rising edges are detected. Accordingly, if edge detection, which is performed at GFE setting, is a problem, avoid such setting combination of the pulse and the edge detecting direction, or set and reset GFE at FNR = 1.

At UPC re-start after interruption, flip-flops for sampling store the data just before interruption.

Notes on using capture commands

When the HD63140 generates an interrupt request signal to MPU at a capturing operation at the edge of input signal, a gap will appear between the timing of the interrupt request signal generation and the capturing operation as shown in figure 15. Therefore, extra care should be taken when processing the value in the capture register in the interrupt request routine.

The UPC samples the input signal every time the value of the function number register becomes 0. It detects the edge of the input signal by the change of the sampled value. Interrupt request signal appears immediately after the sampling at which the edge of the input signal has been detected, but the capturing operation is delayed until the capture command is performed after the sampling. Therefore, the value of the capture register is not updated for 5μs (max) at 4 MHz operation. If this dalay time is inconvenient, set the capture command to as small a function number as possible.

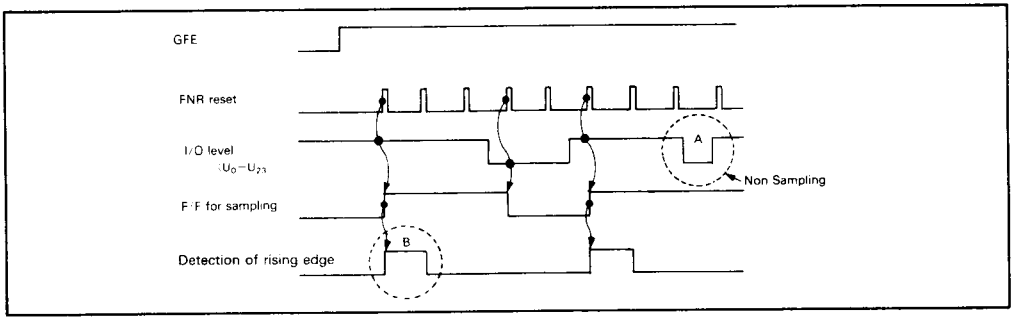


Figure 14. Edge Detection Timing

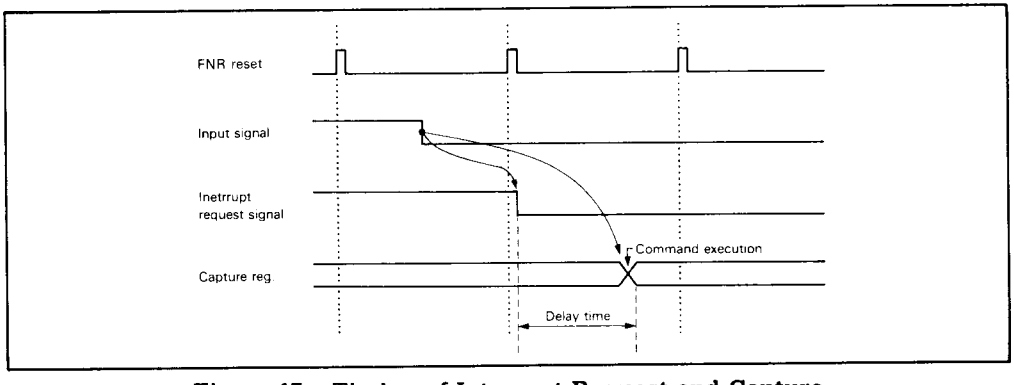


Figure 15. Timing of Interrupt Request and Capture

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	Vcc (Note 2)	−0.3 to + 7.0	V
Input Voltage	Vin (Note 2)	−0.3 to Vcc + 0.3	V
Analog Supply Voltage	AVcc (Note 2)	−0.3 to + 7.0	V
Analog Input Voltage	V_{AN} (Note 2)	−0.3 to AVcc + 0.3	V
Operating Temperature (Note 1)	Topr	−20 to +75	°C
Storage Temperature	Tstg	−55 to +150	°C
Allowable Output Current	|Io| (Note 3)	10	mA
Total Allowable Output Current	|Σ Io| (Note 4)	100	mA

Notes: 1. Wide temperature range (−40°C to +85°C) version is also available. For details, please contact the sales department.
2. With respect to V_{SS} (system GND)
3. The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.
4. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.
5. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LIS.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}*	4.5	5.0	5.5	V
Input Low Voltage	V_{IH}*	2.0	—	V_{CC}	V
Input High Voltage	V_{IL}*	0	—	0.8	V
Schmitt-trigger Input Voltage	V_{T-}*	1.0	0	2.0	V
Schmitt-trigger Input Voltage	V_{T+}*	3.0	—	4.0	V
Analog Supply Voltage	AV_{CC}*	—	5.0	—	V
Analog Input Voltage	V_{AN}*	0	—	AV_{CC}	V
Operating Temperature	T_{opr}	−20	25	75	°C

*Note: *With respect to $V_{SS} = AV_{SS} = 0V$

Electrical Characteristics

DC Characteristics
(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to+75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Schmitt-trigger Input Voltage	$U_8/P_{20}-U_{15}/P_{27}$	V_T^-	1.0	–	2.0	V	Figure 16 V_{cc} = 5.0 V
		V_T^+	3.0	–	4.0	V	
		$V_T^+ - V_T^-$	1.0	–	–	V	
Input high Voltage	$\overline{RES}$, $\overline{STBY}$	V_{IH}	Vcc−0.5	–	Vcc+0.3	V	
	EXTAL		Vcc×0.7	–	Vcc+0.3	V	
	Other Inputs		2.0	–	Vcc+0.3	V	
Input low Voltage	All Inputs	V_{IL}	−0.3	–	0.8	V	
Input Leakage Current	$\overline{RES}$, $\overline{STBY}$ A_0-A_{10}, $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$, $\overline{OE}$, AN_0-AN_9	$\|I_{IN}\|$	–	–	1.0	μA	Vin = 0.5− Vcc−0.5V
Three State Leakage Current (Off state)	D_0-D_7, READY $U_0/P_{10}-U_7/P_{17}$ $U_8/P_{20}-U_{15}/P_{27}$	$\|I_{TSI}\|$	–	–	1.0	μA	Vin = 0.5− Vcc−0.5V
Output high Voltage	All Outputs	V_{OH}	2.4	–	–	V	I_{OH} = −200 μA
			Vcc−0.7	–	–	V	I_{OH} = −10 μA
Output low Voltage	All Outputs	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Leakage Current (Off state)	$\overline{INT_0}$, $\overline{INT_1}$, $\overline{WDTO}$	I_{LOH}	–	–	1.0	μA	V_{IN} = Vcc−0.5
Input Capacitance	All Inputs	Cin	–	–	15	pF	Vin = 0 V f = 1.0 MHz Ta = 25°C
Current Dissipation*		Icc	–	–	30	mA	fopr = 4 MHz **
Standby Current (Except Alcc)		I_{STB}	–	–	15	μA	
RAM Standby Voltage		V_{RAM}	2.0	–	–	V	
Analog Supply Current		Alcc	–	–	1	mA	

Notes: * Current dissipation varies in proportion to operating frequency (fopr).

** fopr = $f_{XTAL}/4$ or $f_{EXT}/4$: HD63140A00
= $f_{EXT}/2$: HD63140B00

AC Characteristics
(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Oscillation Stable Time	t_{RC}	–	–	20	ms	Figure 17
Clock Frequency	f_{opr}	1.0	–	4.0	MHz	Figure 25
Output Clock Frequency	f_{CLK}	–	foprx2	–	MHz	
Output Clock High Pulse Width	t_{CWH}	55	–	–	ns	
Output Clock Low Pulse Width	t_{CWL}	55	–	–	ns	
Output Clock Rise Time	t_{Cr}	–	–	10	ns	
Output Clock Fall Time	t_{Cf}	–	–	10	ns	
Address Set-up Time	t_{AS}	30	–	–	ns	Figure 18-22
Address Hold Time	t_{AH}	5	–	–	ns	Figure 25
Delay Time from $\overline{CS}$ Low until READY Low (Other than RAM)	t_{CRD1}	–	–	60	ns	
Delay Time from $\overline{DS}$ Low until READY High — UDR(UPC)*	t_{WAIT}	–	–	3	μs	
Delay Time from $\overline{DS}$ Low until READY High — Others*				750	ns	
Delay Time from $\overline{DS}$ High until READY Low	t_{CRD2}	–	–	80	ns	
$\overline{DS}$ High Pulse Width	t_{DWH}	80	–	–	ns	Figure 18
R/$\overline{W}$ Set-Up Time	t_{RS}	10	–	–	ns	Figure 20
R/$\overline{W}$ Hold Time	t_{RH}	5	–	–	ns	Figure 21
Read Data Delay Time (RAM)	t_{RDD}	–	–	140	ns	Figure 25
Read Data Delay Time from READY High	t_{RRDD}	–	–	60	ns	
Read Data Delay Time from $\overline{OE}$	t_{ORDD}	–	–	80	ns	
Read Data Hold Time	t_{RDH}	10	–	–	ns	
Read Data Hold Time from $\overline{OE}$ High	t_{ORDH}	10	–	–	ns	
Write Data Delay Time *	t_{WDD}	–	–	120	ns	Figure 19
Write Data Set-Up Time	t_{WDS}	100	–	–	ns	Figure 21
Write Pulse Hold Time from READY High*	t_{WH}	120	–	–	ns	Figure 25
Write Pulse Low Width	t_{WWL}	100	–	–	ns	
Write Data Hold Time	t_{WDH}	5	–	–	ns	
READY Turn Off Time from $\overline{CS}$ High	t_{RTO}	–	–	50	ns	Figure 20-22 Figure 25

Notes: * At fopr = 4 MHz, these times vary in inverse ratio to operating frequency (fopr).

Port I/O Characteristics
(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Port Input Data Set-up Time	t_{PDS}	60	–	–	ns	Figure 23
Port Input Data Hold Time	t_{PDH}	60	–	–	ns	
Port Output Data Delay Time*	t_{PDD}	–	–	170	ns	Figure 24. 25

Notes: * At fopr = 4 MHz, these times vary in inverse ratio to operating frequency (fopr).

4

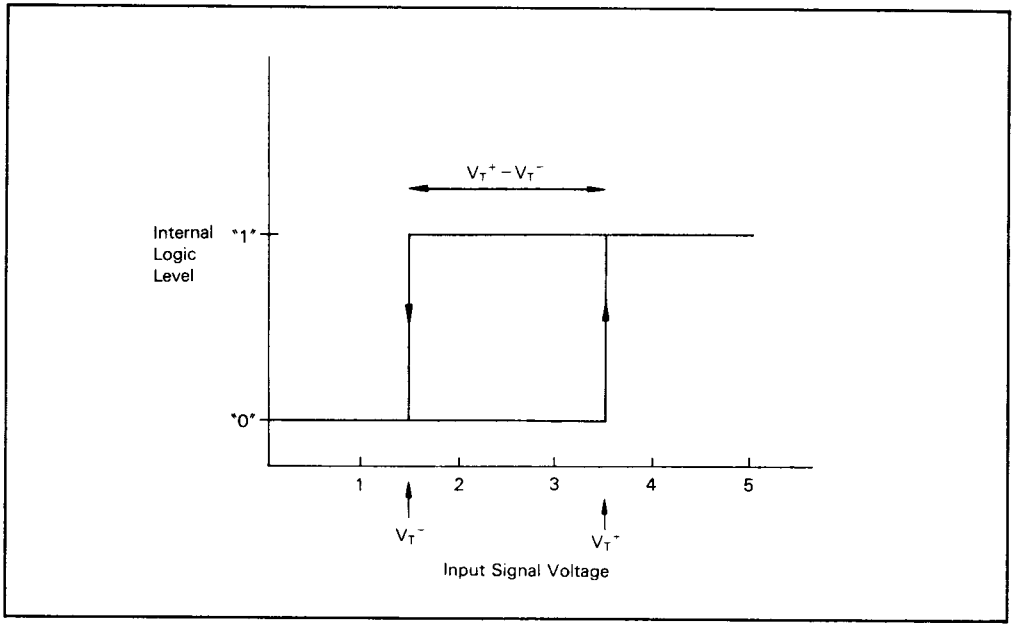


Figure 16. Schmitt Trigger Threshold Level

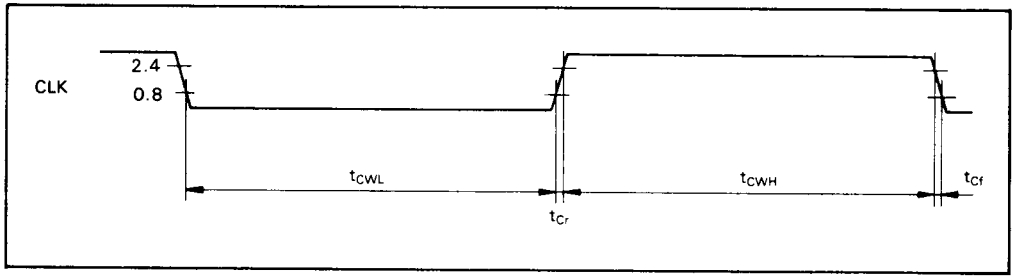
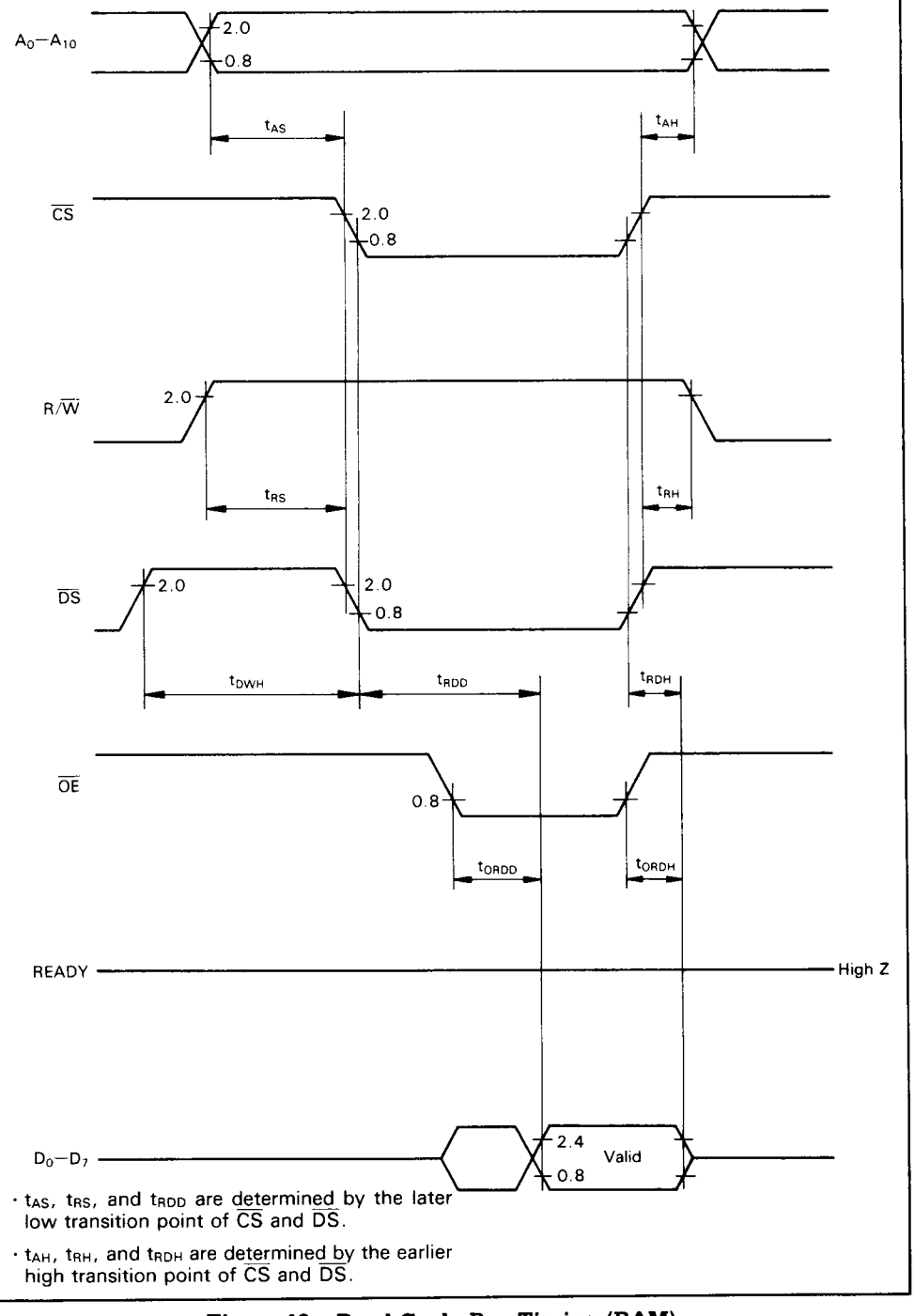


Figure 17. Output Clock Waveform

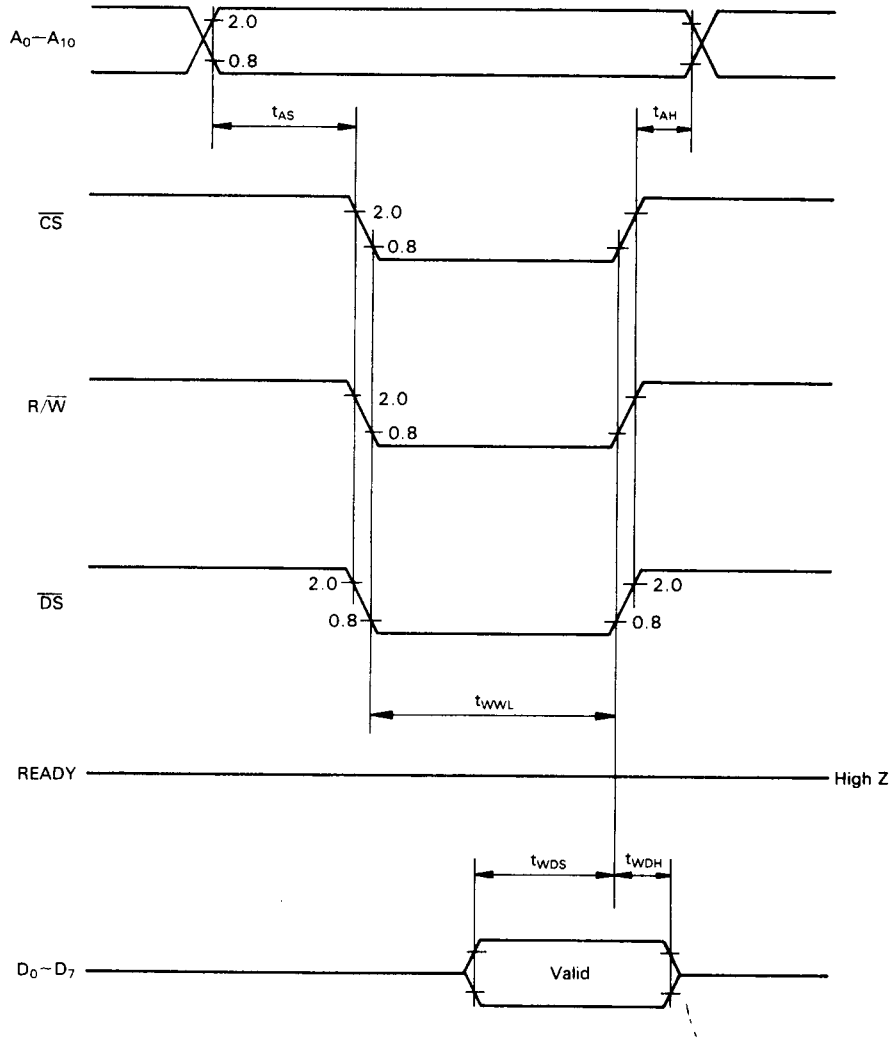


· t_{AS}, t_{RS}, and t_{RDD} are determined by the later low transition point of $\overline{CS}$ and $\overline{DS}$.

· t_{AH}, t_{RH}, and t_{RDH} are determined by the earlier high transition point of $\overline{CS}$ and $\overline{DS}$.

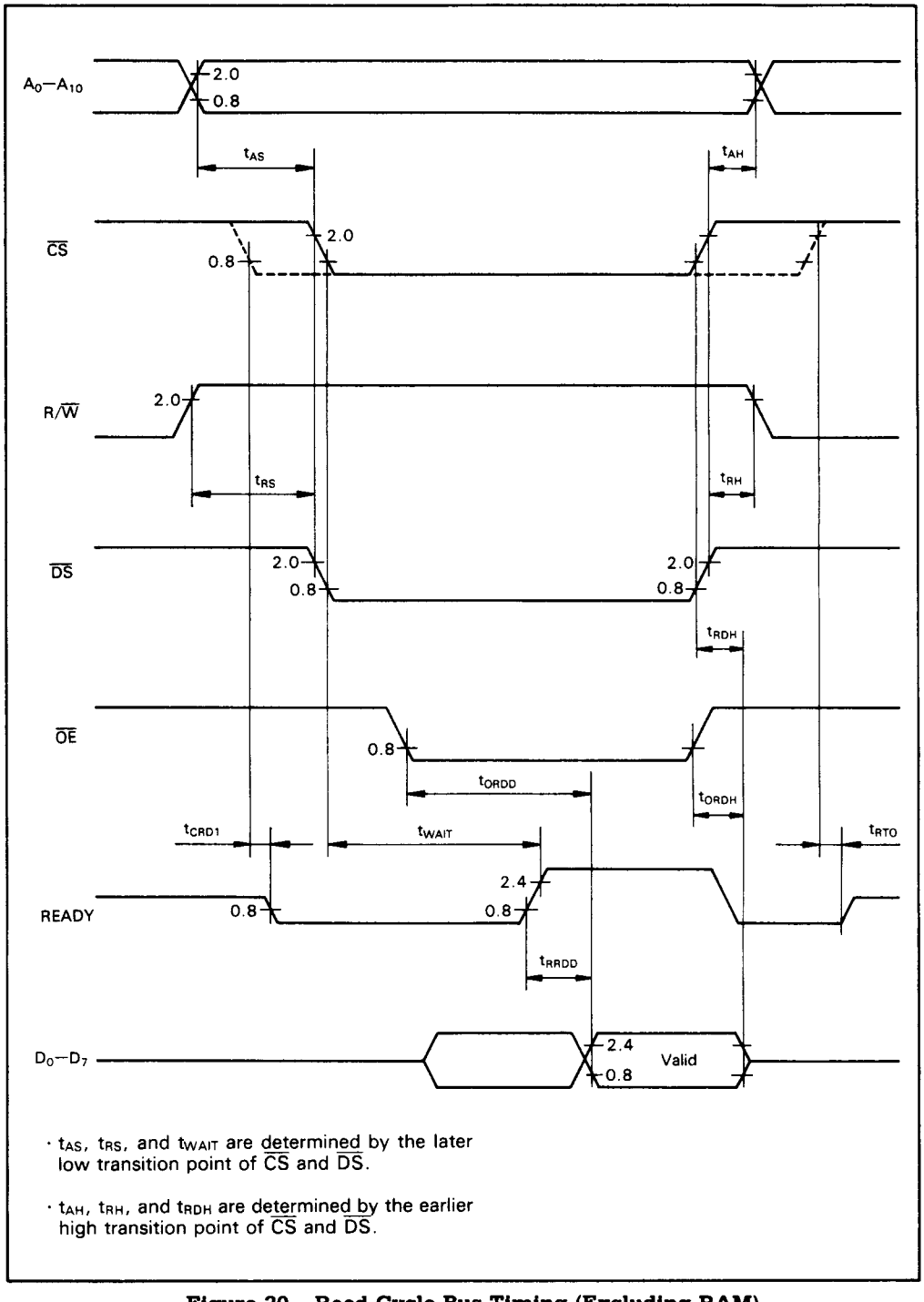
Figure 18. Read Cycle Bus Timing (RAM)

4



- t_{AS} is determined by the latest low transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.
- t_{WWL} is determined by the latest low transition point and the earliest high transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.
- t_{AH} is determined by the earliest high transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.

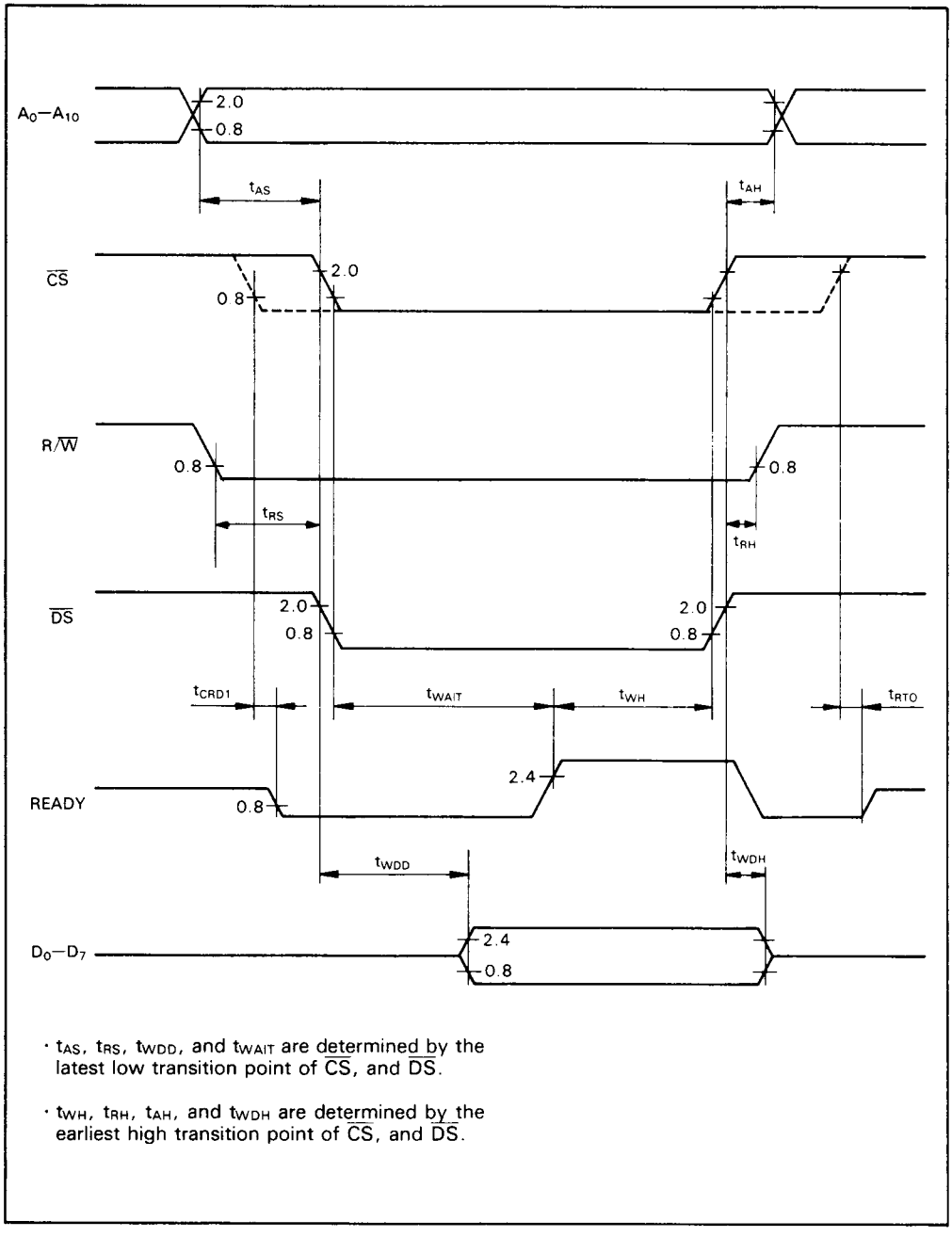
Figure 19. Write Cycle Bus Timing (RAM)



- t_{AS}, t_{RS}, and t_{WAIT} are determined by the later low transition point of $\overline{CS}$ and $\overline{DS}$.
- t_{AH}, t_{RH}, and t_{RDH} are determined by the earlier high transition point of $\overline{CS}$ and $\overline{DS}$.

Figure 20. Read Cycle Bus Timing (Excluding RAM)

4



· t_{AS}, t_{RS}, t_{WDD}, and t_{WAIT} are determined by the latest low transition point of $\overline{CS}$, and $\overline{DS}$.

· t_{WH}, t_{RH}, t_{AH}, and t_{WDH} are determined by the earliest high transition point of $\overline{CS}$, and $\overline{DS}$.

Figure 21. Write Cycle Bus Timing (Excluding RAM)

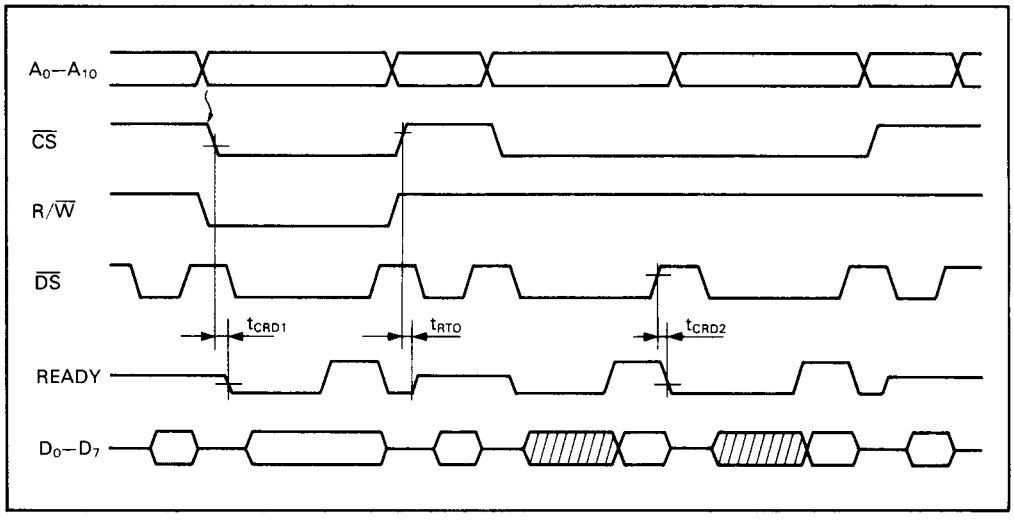


Figure 22. READY Timing for 1-Byte (Write) and 2-Byte (Read) Access

4

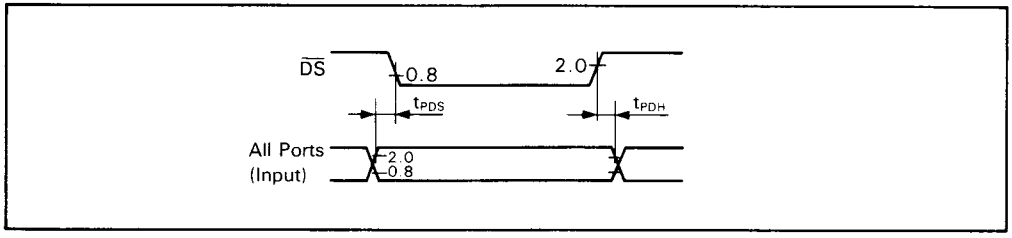


Figure 23. Port Input Timing

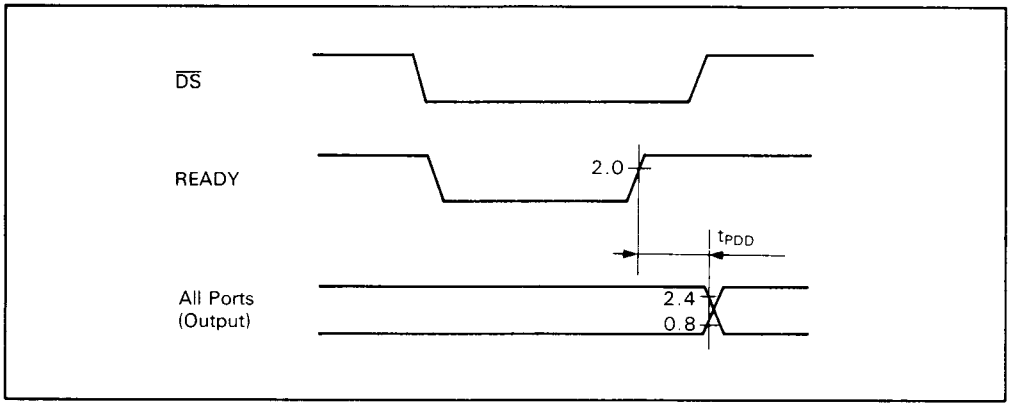
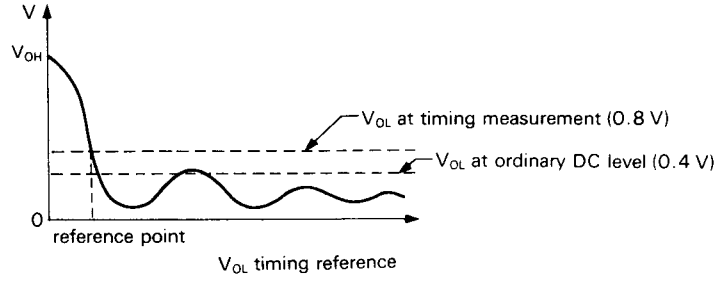


Figure 24. Port Output Timing

Timing Measurement Method

Output low voltage at measurement is 0.8 V.

Whereas ordinary output low voltage (DC characteristics) is 0.4 V.



Timing Measurement point of V_{OL}

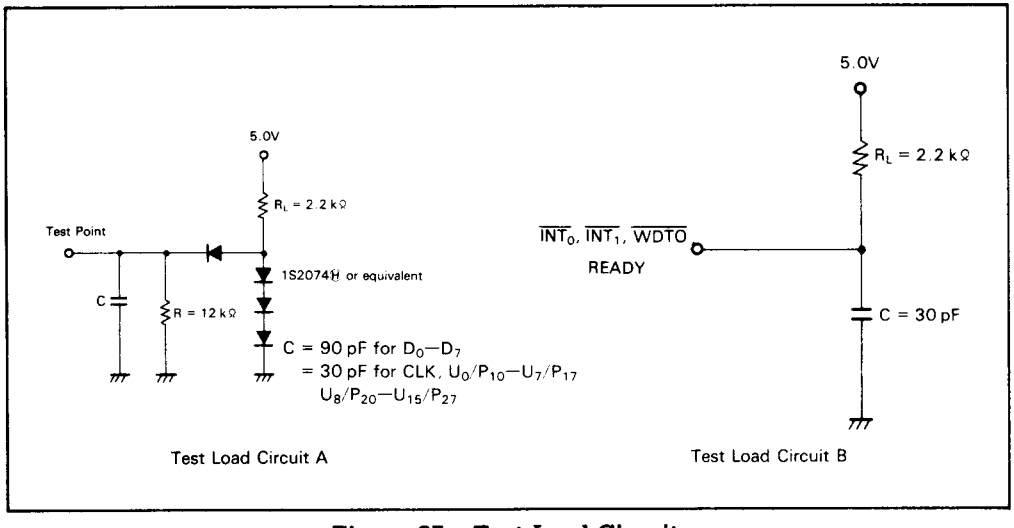


Figure 25. Test Load Cicurit

4

A/D Conversion (Vcc = 5.0 V, AVcc = 5.0 V, Vss = AVss = 0V, Ta = −20°C to 75°C, unless otherwise noted)

Item	Min	Typ	Max	Unit
Resolution	–	10	–	bits
Non-Linearity Error	–	±1	±1.5	LSB
Offset Error	–	–	±1	LSB
Full-Scale Error	–	–	±1	LSB
Quantization Error	–	–	±0.5	LSB
Absolute Accuracy	–	±1.5	±2	LSB

Note: The external input resistance must be lower than 10 k Ω.

The definition of A/D conversion accuracy for the HD63140 is described below.

Resolution: The number of output binary digit.

Offset Error: The deviation from the ideal A/D conversion characteristics of an analog input volrage value when a digital output changes from a minimum voltage value of 000...0 to 000.....1. (Refer to figure 26)

Full-Scale Error: The deviation from the ideal A/D conversion characteristics of an analog input voltage value when digital output changes from 1111....10 to full-scale value 1111....11.

Quantization error: This error is intrinsic to A/D converters and is represented by ±0.5 LSB.

Non-Linearity Error: The deviation from the ideal A/D conversion characteristics from O V to the full-scale voltage, except for the offset error, full-scale error, and quantization error.

Absolute error: The deviation between a digital output value and analog input value. All errors from (2) to (5) are included.

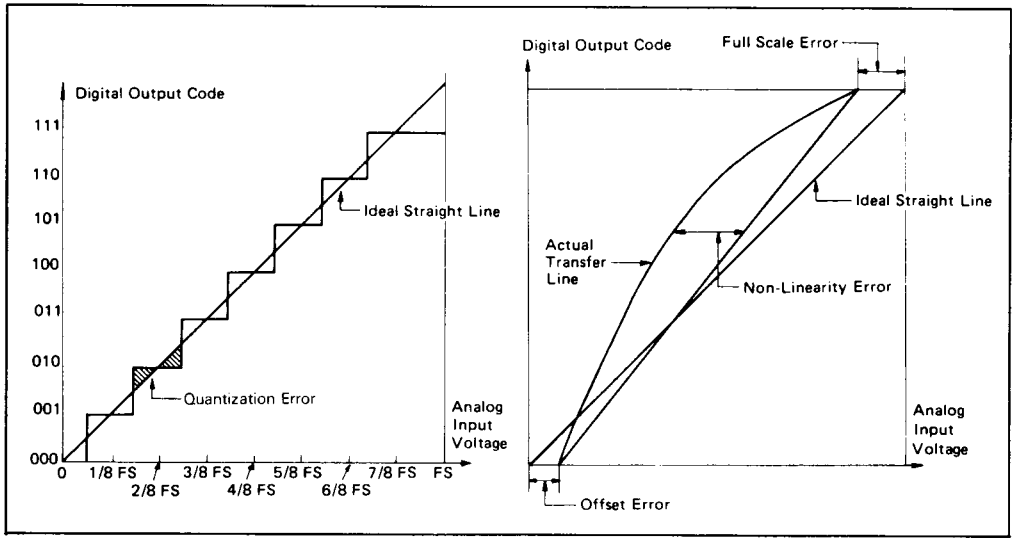


Figure 26. The Definition of A/D Conversion

Refer to application note (No. ADE-502-002) for detail of this product.