

# FDW2502P

## Dual P-Channel 2.5V Specified PowerTrench<sup>®</sup> MOSFET

### General Description

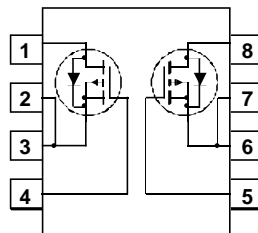
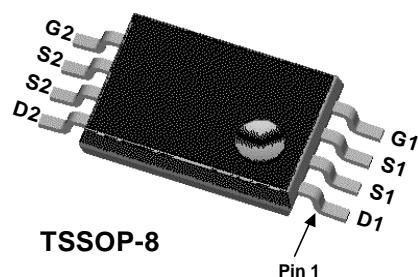
This P-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild's Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V -12V).

### Applications

- Load switch
- Motor drive
- DC/DC conversion
- Power management

### Features

- -4.4 A, -20 V.  $R_{DS(ON)} = 0.035 \Omega @ V_{GS} = -4.5 V$   
 $R_{DS(ON)} = 0.057 \Omega @ V_{GS} = -2.5 V$ .
- Extended  $V_{GSS}$  range ( $\pm 12V$ ) for battery applications.
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- Low profile TSSOP-8 package.



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	-4.4	A
		-30	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.0	W
		0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	125	$^\circ C/W$
		208	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2502P	FDW2502P	13"	12mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-17		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-1.0	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		3.1		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -4.4\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -4.4, T_J = 125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -3.3\text{ A}$		0.028 0.039 0.043	0.035 0.056 0.057	$\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-30			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -4.4\text{ A}$		17		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1330		pF
$C_{oss}$	Output Capacitance			552		pF
$C_{rss}$	Reverse Transfer Capacitance			153		pF

**Switching Characteristics (Note 2)**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		12	25	ns
$t_r$	Turn–On Rise Time			19	40	ns
$t_{d(off)}$	Turn–Off Delay Time			60	100	ns
$t_f$	Turn–Off Fall Time			37	70	ns
$Q_g$	Total Gate Charge	$V_{DS} = -5\text{ V}, I_D = -4.4\text{ A},$ $V_{GS} = -4.5\text{ V}$		14	20	nC
$Q_{gs}$	Gate–Source Charge			3.0		nC
$Q_{gd}$	Gate–Drain Charge			3.9		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-0.83	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.83\text{ A}$ (Note 2)		-0.7	-1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

- a)  $R_{\theta JA}$  is  $125^\circ\text{C/W}$  (steady state) when mounted on a  $1\text{ inch}^2$  copper pad on FR-4.  
b)  $R_{\theta JA}$  is  $208^\circ\text{C/W}$  (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics

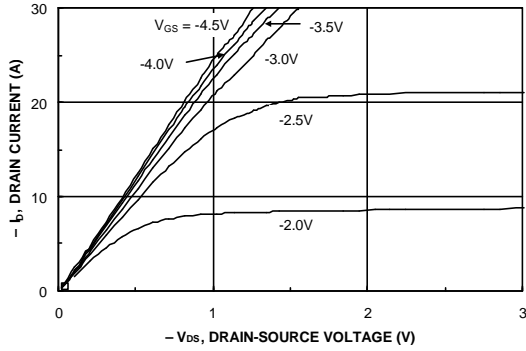


Figure 1. On-Region Characteristics.

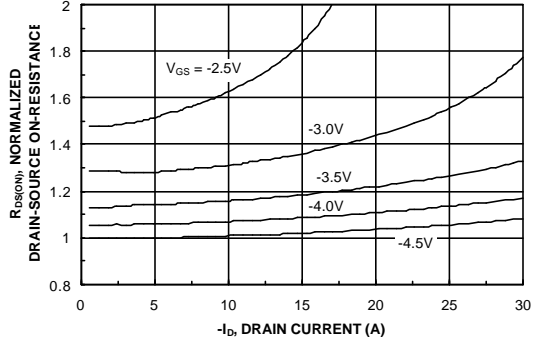


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

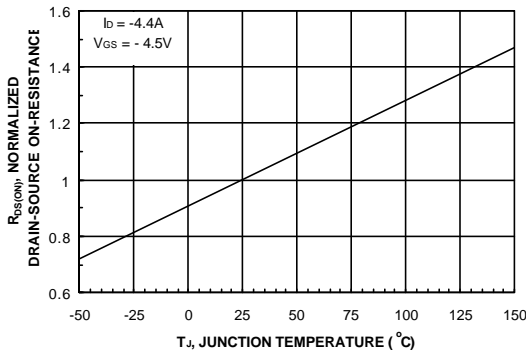


Figure 3. On-Resistance Variation with Temperature.

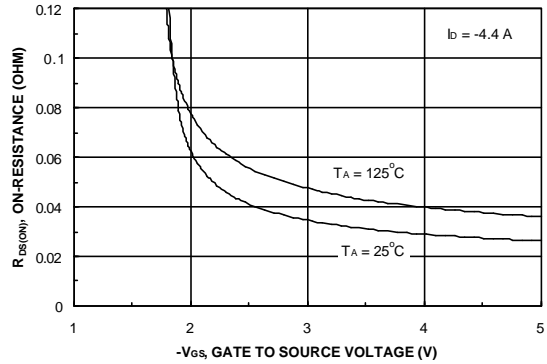


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

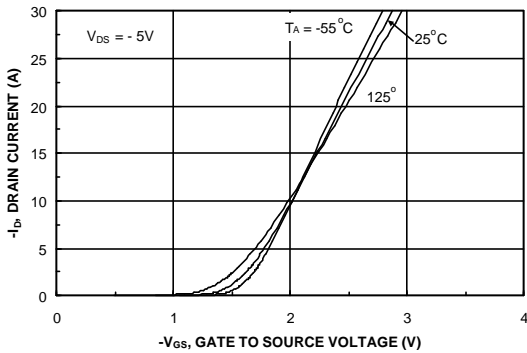


Figure 5. Transfer Characteristics.

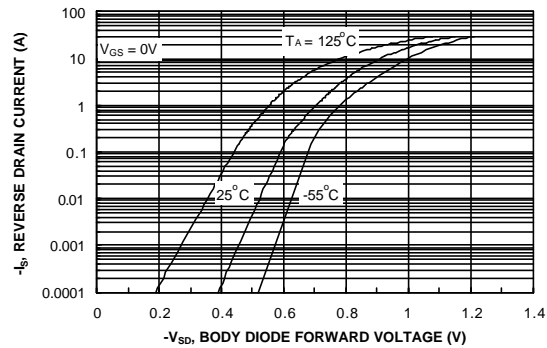


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics

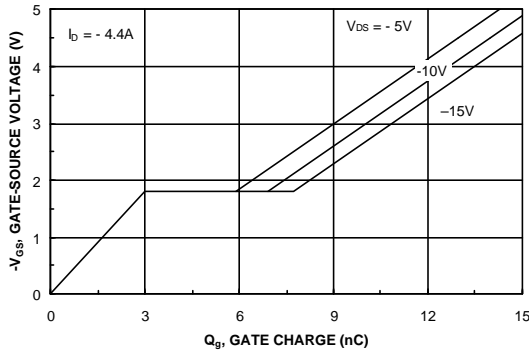


Figure 7. Gate Charge Characteristics.

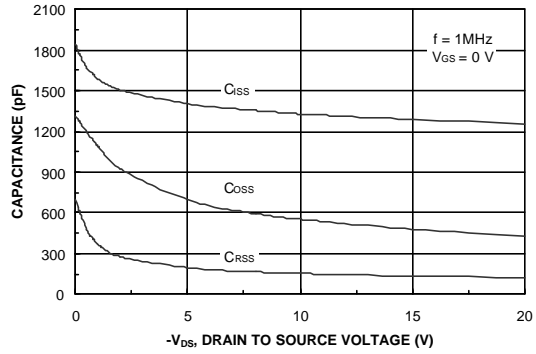


Figure 8. Capacitance Characteristics.

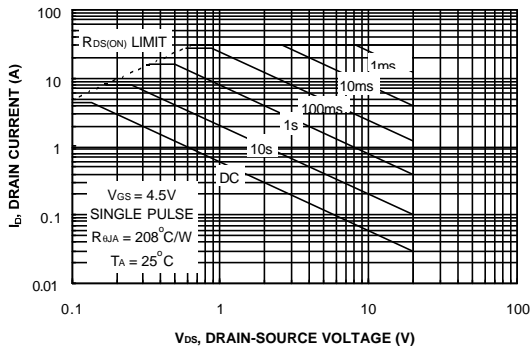


Figure 9. Maximum Safe Operating Area.

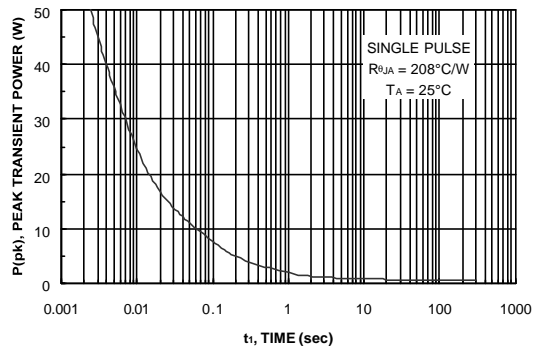


Figure 10. Single Pulse Maximum Power Dissipation.

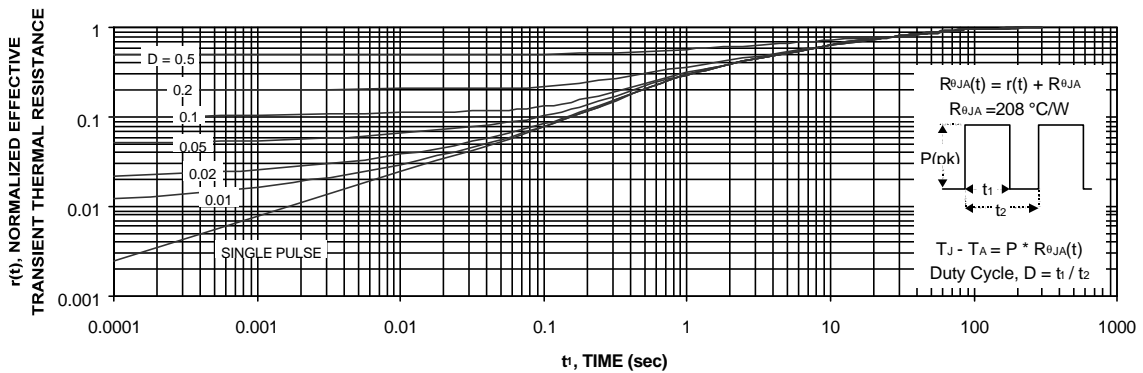


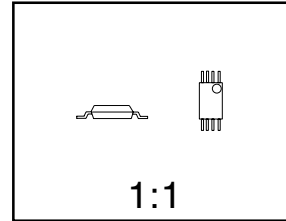
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.  
Transient thermal response will change depending on the circuit board design.

# TSSOP-8 Package Dimensions



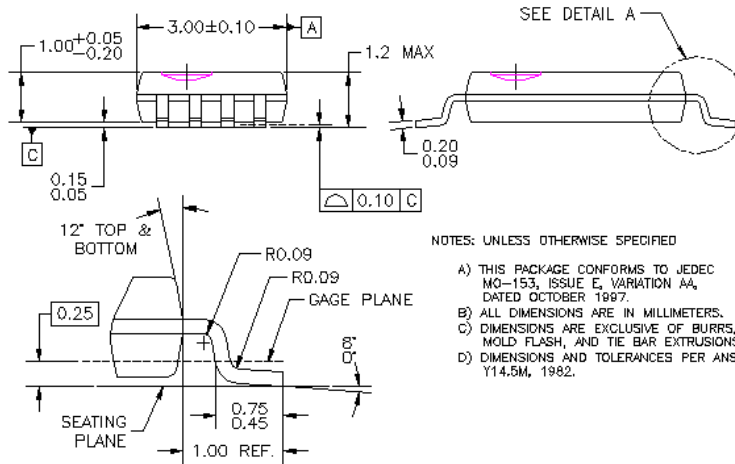
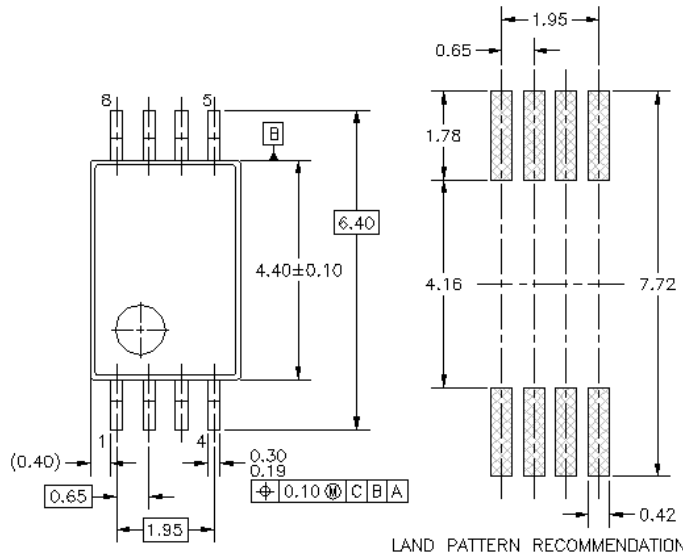
## TSSOP-8 (FS PKG Code S4)



Scale 1:1 on letter size paper

Dimensions shown below are in millimeters

Part Weight per unit (gram): 0.0334



DETAIL A  
SCALE: 2X

MTC06REV6

NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MO-153, ISSUE E, VARIATION AA, DATED OCTOBER 1987.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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