SONY

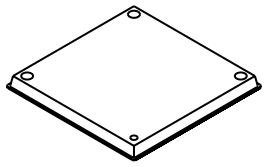
CXD3526GG

Digital Signal Driver/Timing Generator

Description

The CXD3526GG incorporates digital signal processor type RGB driver, color shading correction and timing generator functions onto a single IC. Operation is possible with a system clock up to 85 [MHz] (max.). This IC can process video signals in bands up to XGA standard, and can output the timing signals for driving various Sony LCD panels such as XGA and SVGA.

144 pin BGA (Plastic)



Features

- Various picture quality adjustment functions such as user adjustment, white balance adjustment and gamma correction
- OSD MIX, black frame processing, mute and limiter functions
- LCD panel color shading correction function
- Drives various Sony data projector LCD panels such as XGA and SVGA
- Controls the CXA3562AR and CXA7000R sample-and-hold drivers
- Line inversion and field inversion signal generation
- Supports AC drive of LCD panels during no signal
- On-chip serial interface
- The data of gamma correction and color shading correction can be downloaded automatically from the external EEPROM.

Applications

LCD projectors and other video equipment

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (V_{SS} = 0V)

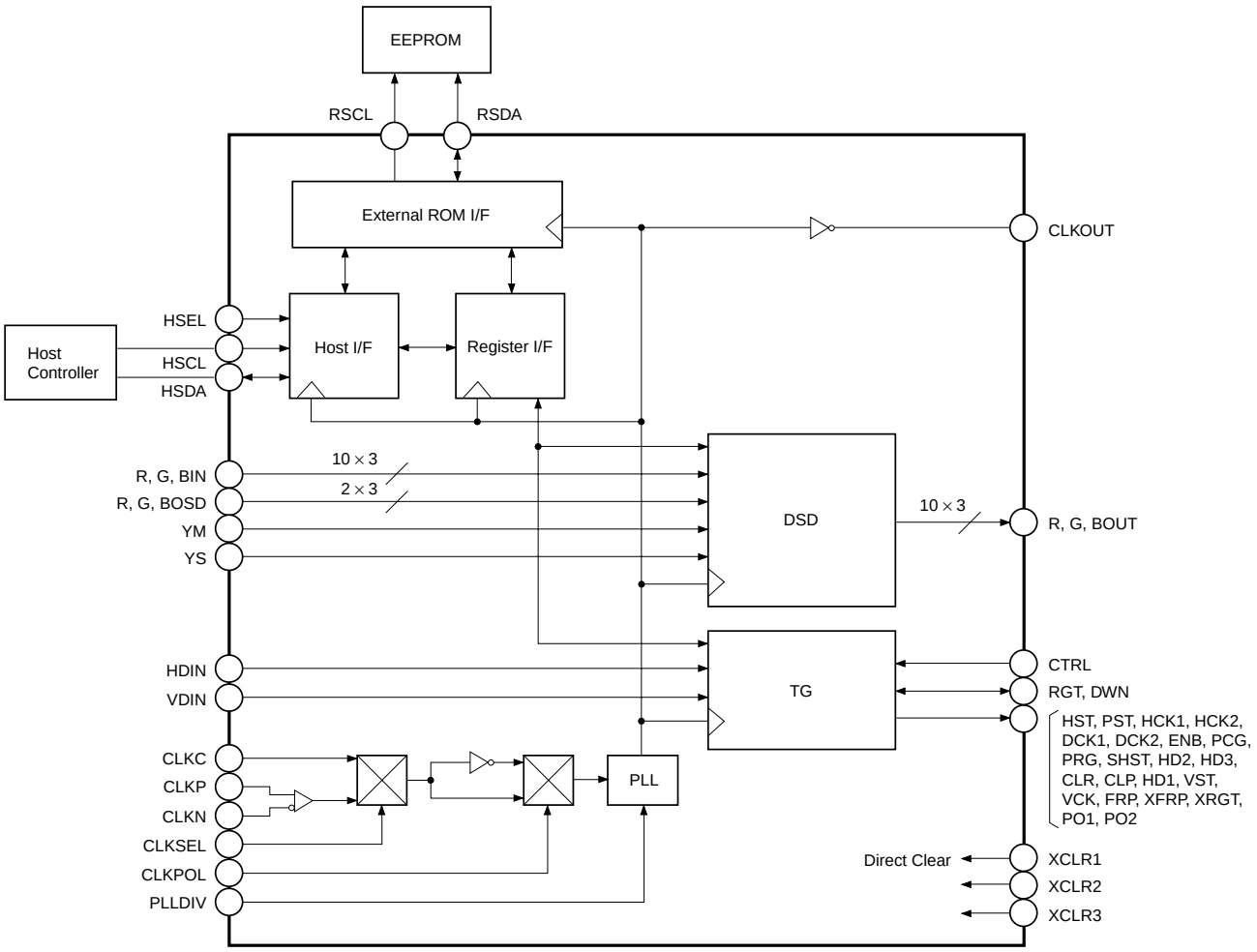
• Supply voltage	V_{DD1}	V_{SS} – 0.5 to +3.0	V
	V_{DD2}	V_{SS} – 0.5 to +4.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD2} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD2} + 0.5	V
• Storage temperature	Tstg	–55 to +125	°C
• Junction temperature	Tj	125	°C

Recommended Operating Conditions

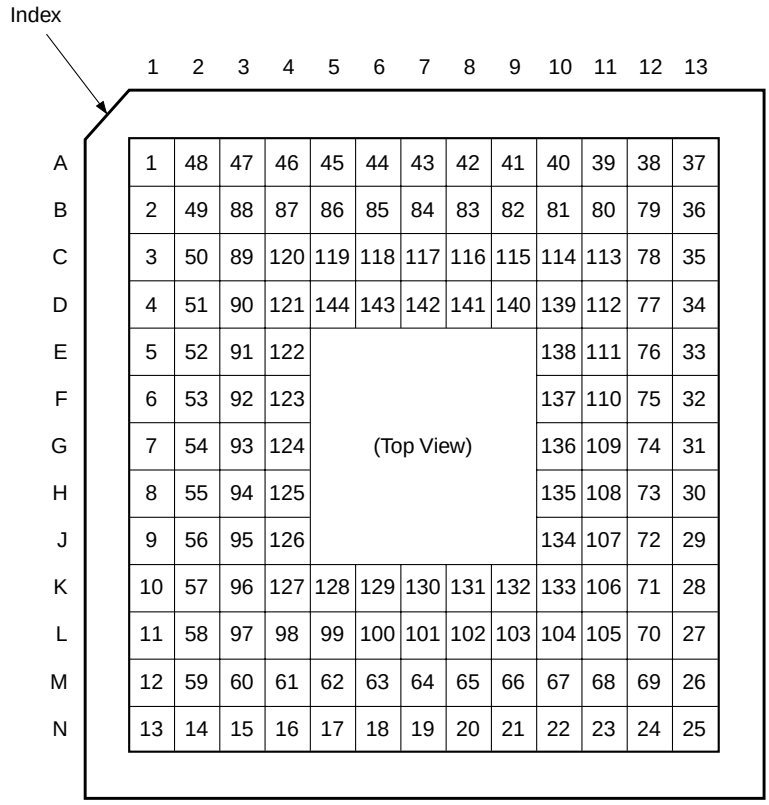
• Supply voltage	V_{DD1}	2.3 to 2.7	V
	V_{DD2}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

E01X09A26

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	Input pin processing for open status
1	V_{SS}	—	GND	—
2	RGT	I/O	Horizontal scan direction switching signal I/O	—
3	XRGT	O	Horizontal scan direction switching signal output (reversed polarity of RGT)	—
4	RIN5	I	Red data input	—
5	RIN2	I	Red data input	—
6	RIN0	I	Red data input	—
7	GIN4	I	Green data input	—
8	GIN0	I	Green data input	—
9	BIN7	I	Blue data input	—
10	BIN4	I	Blue data input	—
11	BIN1	I	Blue data input	—
12	BIN0	I	Blue data input	—
13	V_{SS}	—	GND	—
14	ROSD0	I	OSD red data input	—
15	GOSD0	I	OSD green data input	—
16	BOSD0	I	OSD blue data input	—
17	VDIN	I	Vertical sync signal input	—
18	TEST1	—	Test pin (Connect to GND.)	—
19	V_{SS}	—	GND	—
20	V_{DD1}	—	Internal operation power supply	—
21	V_{SS}	—	GND	—
22	HSEL	I	Serial bus slave address selection signal input	—
23	RSCL	I/O	Serial bus clock I/O (external ROM I/F)	—
24	TEST2	—	Test pin (Connect to V_{DD2}.)	—
25	V_{SS}	—	GND	—
26	TEST3	—	Test pin (Connect to V_{DD2}.)	—
27	TEST4	—	Test pin (Connect to V_{DD2}.)	—
28	CLKOUT	O	Internal clock output (inverted output)	—
29	BOUT3	O	Blue data output	—
30	V_{DD2}	—	I/O power supply	—
31	V_{SS}	—	GND	—
32	GOUT3	O	Green data output	—
33	GOUT6	O	Green data output	—
34	GOUT9	O	Green data output	—
35	ROUT2	O	Red data output	—
36	ROUT6	O	Red data output	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
37	V_{SS}	—	GND	—
38	ROUT9	O	Red data output	—
39	ROUT8	O	Red data output	—
40	ROUT7	O	Red data output	—
41	VST	O	Vertical display start timing pulse output	—
42	HD2	O	Horizontal auxiliary pulse output 2	—
43	HD3	O	Horizontal auxiliary pulse output 3	—
44	V_{DD2}	—	I/O power supply	—
45	PRG	O	2-step precharge timing pulse output	—
46	ENB	O	Gate enable pulse output	—
47	PO1	O	Parallel output 1	—
48	PO2	O	Parallel output 2	—
49	DWN	I/O	Vertical scan direction switching signal I/O	—
50	RIN8	I	Red data input	—
51	RIN6	I	Red data input	—
52	RIN3	I	Red data input	—
53	RIN1	I	Red data input	—
54	GIN5	I	Green data input	—
55	GIN1	I	Green data input	—
56	BIN8	I	Blue data input	—
57	BIN5	I	Blue data input	—
58	BIN2	I	Blue data input	—
59	ROSD1	I	OSD red data input	—
60	GOSD1	I	OSD green data input	—
61	BOSD1	I	OSD blue data input	—
62	HDIN	I	Horizontal sync signal input	—
63	CLKPOL	I	Internal clock polarity selection (High: inverted; Low: non-inverted)	L
64	V_{SS}	—	GND	—
65	TEST5	—	Test pin (Connect to V_{DD2}.)	—
66	XCLR2	I	External clear (Low: reset)	H
67	TEST6	—	Test pin (Connect to GND.)	—
68	HSCL	I	Serial bus clock (host I/F)	—
69	RSDA	I/O	Serial bus data I/O (external ROM I/F)	—
70	HSDA	I/O	Serial bus data I/O (host I/F)	—
71	V_{SS}	—	GND	—
72	BOUT2	O	Blue data output	—
73	BOUT6	O	Blue data output	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
74	BOUT9	O	Blue data output	—
75	GOUT2	O	Green data output	—
76	GOUT5	O	Green data output	—
77	GOUT8	O	Green data output	—
78	ROUT1	O	Red data output	—
79	ROUT5	O	Red data output	—
80	ROUT4	O	Red data output	—
81	ROUT3	O	Red data output	—
82	VCK	O	Vertical display transfer clock output	—
83	HD1	O	Horizontal auxiliary pulse output 1	—
84	PCG	O	Collective precharge timing pulse output	—
85	V_{SS}	—	GND	—
86	CLR	O	CLR pulse output	—
87	DCK1	O	DCK1 pulse output	—
88	CTRL	I	Scan direction control method switching (Low: internal register; High: external)	L
89	RIN9	I	Red data input	—
90	RIN7	I	Red data input	—
91	RIN4	I	Red data input	—
92	GIN8	I	Green data input	—
93	GIN6	I	Green data input	—
94	GIN2	I	Green data input	—
95	BIN9	I	Blue data input	—
96	BIN6	I	Blue data input	—
97	BIN3	I	Blue data input	—
98	YM	I	OSD YM input	L
99	YS	I	OSD YS input	L
100	CLKSEL	I	Input clock selection (High: CLKC; Low: CLKP/N)	L
101	CLKP	I	Clock input (small-amplitude differential input, positive polarity)	—
102	XCLR1	I	External clear (Low: reset)	H
103	XCLR3	I	External clear (Low: reset)	H
104	TEST7	—	Test pin (Connect to GND.)	—
105	V_{SS}	—	GND	—
106	BOUT0	O	Blue data output	—
107	BOUT1	O	Blue data output	—
108	BOUT5	O	Blue data output	—
109	BOUT8	O	Blue data output	—
110	GOUT1	O	Green data output	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
111	GOUT4	O	Green data output	—
112	GOUT7	O	Green data output	—
113	ROUT0	O	Red data input	—
114	V_{DD2}	—	I/O power supply	—
115	CLP	O	CLP pulse output	—
116	HST	O	Horizontal display start timing pulse output	—
117	HCK1	O	Horizontal display transfer clock output 1	—
118	FRP	O	AC drive inversion timing pulse output	—
119	SHST	O	SHST pulse output	—
120	DCK2	O	DCK2 pulse output	—
121	V_{SS}	—	GND	—
122	V_{DD1}	—	Internal operation power supply	—
123	GIN9	I	Green data input	—
124	GIN7	I	Green data input	—
125	GIN3	I	Green data input	—
126	V_{DD2}	—	I/O power supply	—
127	Vss	—	GND	—
128	V_{DD1}	—	Internal operation power supply	—
129	PLLDIV	I	Internal PLL setting (High: 55MHz or less; Low: 55MHz or more)	L
130	CLKN	I	Clock input (small-amplitude differential input, negative polarity)	—
131	CLKC	I	Clock input (CMOS input)	—
132	V_{DD2}	—	I/O power supply	—
133	V_{SS}	—	GND	—
134	V_{DD1}	—	Internal operation power supply	—
135	BOUT4	O	Blue data output	—
136	BOUT7	O	Blue data output	—
137	GOUT0	O	Green data output	—
138	V_{DD2}	—	I/O power supply	—
139	V_{SS}	—	GND	—
140	V_{DD1}	—	Internal operation power supply	—
141	PST	O	Dot sequential precharge start timing pulse output	—
142	HCK2	O	Horizontal display transfer clock output 2	—
143	XFRP	O	AC drive inversion timing pulse output (reversed polarity of FRP)	—
144	V_{DD2}	—	I/O power supply	—

Electrical Characteristics

DC Characteristics

(Topr = –20 to +75°C, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD1}	—	—	2.3	2.5	2.7	V
	V_{DD2}	—	—	3.0	3.3	3.6	
Input voltage 1	V_{IH1}	*1	CMOS input cell	2.0	—	V_{DD2} + 0.3	
	V_{IL1}			–0.3	—	0.8	
Input voltage 2	V_{IH2}	HDIN, VDIN, HSCL	CMOS Schmitt trigger input cell	0.8V_{DD2}	—	V_{DD2} + 0.3	
	V_{IL2}			–0.3	—	0.2V_{DD2}	
Input voltage 3	VC*2	CLKP, CLKN	Small-amplitude differential input	1.718	2.0	2.281	
	V_{IH3}			1.868	VC + 0.4	V_{DD2}	
	V_{IL3}			V_{SS}	VC – 0.4	2.131	
Output voltage	V_{OH}	All output pins	—	V_{DD2} – 0.2	—	V_{DD2}	
	V_{OL}		—	V_{SS}	—	0.2	
Power consumption	PD*3	—	CLKP = 85MHz	—	950	1140	mW

*1 Input pins other than those indicated in items Input voltage 2 and Input voltage 3.

*2 V_{IH3} > VC (max.) and V_{IL3} < VC (min.).

*3 Tj [°C] ≥ Toprmax [°C] + θja [°C/W] × PD [W].

AC Characteristics

(Topr = –20 to +75°C, V_{DD1} = 2.5 ± 0.2V, V_{DD2} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Clock input period	—	CLKP, CLKN, CLKC	—	10.0	—	—	ns
Input setup time	tis	RGB input, OSD input, HDIN, VDIN	—	2.0	—	—	
Input hold time	tih		—	2.0	—	—	
Input setup time	tis	HSCL, HSDA, RSDA	—	5.0	—	—	
Input hold time	tih		—	5.0	—	—	
Output rise/fall delay time	tor/tof	*4	CL = 20pF	2.5	4.0	7.0	
Output rise/fall delay time	tor/tof	FRP, XFRP, SHST, CLKOUT	CL = 50pF	2.5	4.0	7.0	
Cross-point time difference	Δt	HCK1, HCK2, DCK1, DCK2	CL = 20pF	–5.0	—	5.0	
HCK1 duty	th/(th + tl)	HCK1	CL = 20pF	48	50	52	%
HCK2 duty	tl/(th + tl)	HCK2	CL = 20pF	48	50	52	
Phase compensation PLL operating frequency	—	—	PLLDIV = L	55	—	100	MHz
			PLLDIV = H	27.5	—	55	

*4 Output pins other than FRP, XFRP, SHST and CLKOUT.

Power Consumption and Allowable Power Dissipation

The relationship between the power consumption and junction temperature of this IC must satisfy the following formula.

$Tj\ [°C] \geq Toprmax\ [°C] + \theta ja\ [°C/W] \times PD\ [W]$

In addition, specification values are as follows.

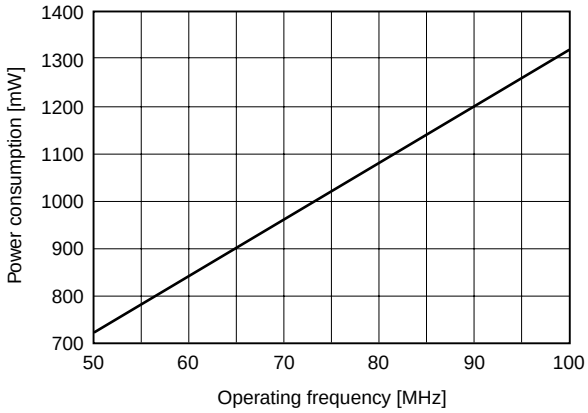
Tjmax = 125 [°C]
Toprmax = 75 [°C]
θja = 43 [°C/W] (When mounted on 4-layer substrate, wind speed 0m/s)

Under these conditions, PDmax, the maximum allowable power dissipation for the package, is as follows.

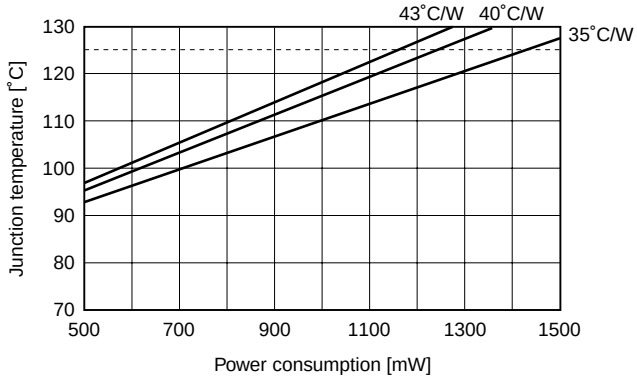
PDmax = (125 – 75)/43 = 1162 [mW]

Furthermore, if the operating frequency of this IC exceeds 85MHz, the junction temperature may exceed its maximum value depending on conditions of use. Use this IC under conditions where the maximum value for the junction temperature will not be exceeded by lowering the thermal resistance of the package as follows by taking thermal countermeasures at this time.

Wind speed 1m/s: θja = 40 [°C/W] (When mounted on 4-layer substrate)
Wind speed 3m/s: θja = 35 [°C/W] (When mounted on 4-layer substrate)



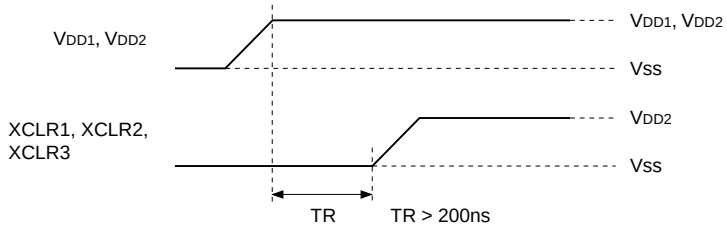
Operating Frequency vs. Power Consumption (Maximum Values)



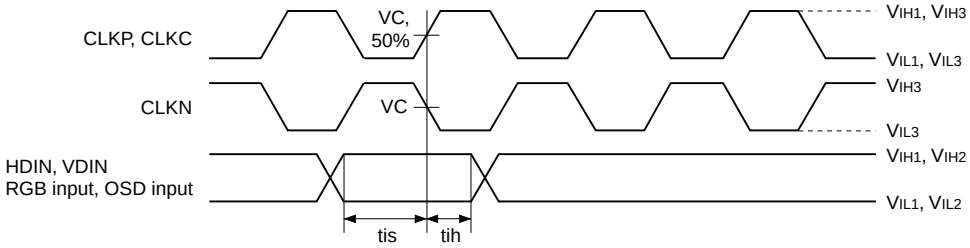
Power Consumption vs. Junction Temperature (for Various Values of Thermal Resistance)

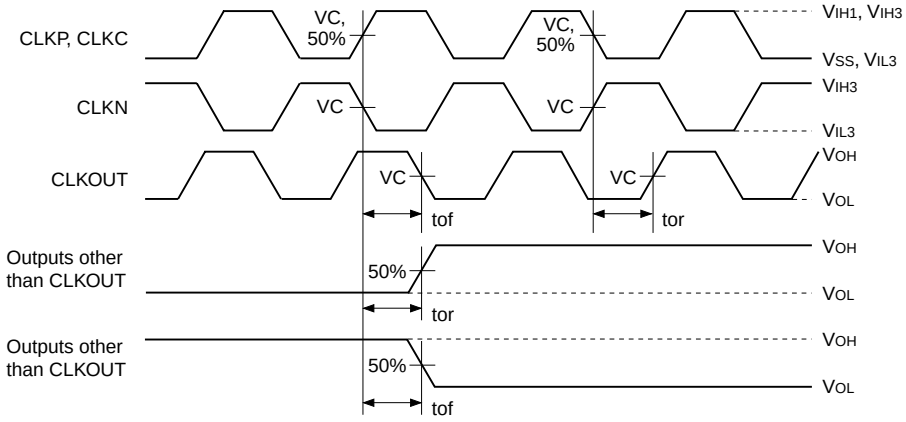
Power-on and Initialization of Internal Circuit

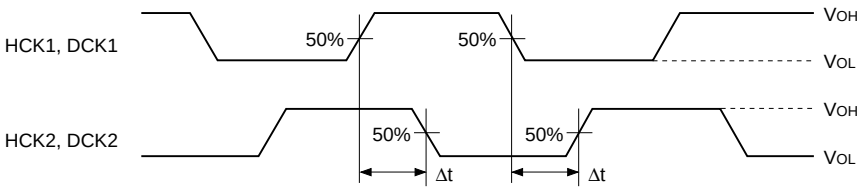
As for this IC, two systems of supply voltage should be turned on simultaneously. The initialization of the internal circuit should be also performed by maintaining the system clear pin at low during the specified time after setting the supply voltage in the range of recommended operating conditions and stabilizing as shown in the figure below. Keep in mind that the internal circuit may not be initialized correctly if system clear cancellation is performed before the supply voltage is set in the range of the recommended operating conditions.

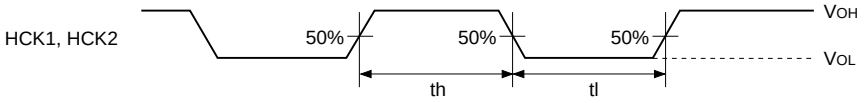


Timing Definition









Description of Operation

1. Description of I/O Pins

(a) System clear pins (XCLR1, XCLR2 and XCLR3)

All internal circuits are initialized by setting XCLR1 (Pin 102) low. In addition, the internal PLL is initialized by setting XCLR2 (Pin 66) low, and RGB output is initialized (preset) by setting XCLR3 (Pin 103) low.
Initialization should be performed when power is turned on.

(b) Sync signal input pins (HDIN and VDIN)

Horizontal and vertical separate sync signals are input to HDIN (Pin 62) and VDIN (Pin 17), respectively. The CXD3526GG supports only non-interlace sync signals with a dot clock of 100MHz or less.

(c) Master clock input pins (CLKP/CLKN, CLKC, CLKSEL and CLKPOL)

Phase comparison is performed by an external circuit and a clock synchronized to the sync signal is input. The master clock input pins have two systems consisting of CLKP/CLKN (Pins 101 and 130) for small-amplitude differential input (center level: 2.0V, amplitude: ±0.4V), and CLKC (Pin 131) for CMOS level input. In addition, the clock path selection is performed with CLKSEL (Pin 100) and CLKPOL (Pin 63). The setting values are as follows.

CLKSEL: 0 = CLKP and CLKN input; 1 = CLKC input
CLKPOL: 0 = Input clock is non-inverted; 1 = Input clock is inverted

(d) PLL setting pin (PLLDIV)

PLLDIV (Pin 129) sets the divider setting of the internal phase compensation PLL circuit. The setting values for master clock frequency are as follows.

PLLDIV: 0 = 55 to 100MHz; 1 = 27.5 to 55MHz

Note that the frequency of the clock input to the CXD3526GG must be within the phase compensation PLL operating range, even during free running.

(e) RGB signal input pins (RIN, GIN and BIN)

These pins input RGB digital signals in 10 bits. The Red signal is input to RIN (Pins 4 to 6, 50 to 53 and 89 to 91), the Green signal to GIN (Pins 7, 8, 54, 55, 92, 93 and 123 to 125), and the Blue signal to BIN (Pins 9 to 12, 56 to 58 and 95 to 97) respectively.

(f) OSD signal input pins (ROSD, GOSD, BOSD, YS and YM)

These pins input OSD signals. The Red signal is input to ROSD (Pins 14 and 59), the Green signal to GOSD (Pins 15 and 60), and the Blue signal to BOSD (Pins 16 and 61) respectively. In addition, the YM signal is input to YM (Pin 98), and the YS signal to YS (Pin 99).

(g) Host I/F serial clock input pin (HSCL)

HSCL (Pin 68) is the clock input pin used to set the I/O timing for serial data from the host. Data is taken from the HSDA pin when the clock signal rises, and data is output to the HSDA pin when the clock signal falls.

(h) Host I/F serial I/O pin (HSDA)

This is the I/O pin for serial data from the host. It is necessary to switch the input to the HSDA (Pin 70) while the signal level of HSCL is low.

(i) Slave address input pin (HSEL)

With this IC, it is possible to select host I/F slave address. Since a slave address is used to identify each of these devices, this pin should be connected to V_{DD} or Vss externally. This V_{DD} and Vss setting drives the device which matches the slave address input from the HSDA pin. The slave addresses of this IC used for the HSEL (Pin 22) setting are as follows.

HSEL: 0 = 74h; 1 = 76h

(j) External ROM I/F serial clock output pin (RSCL)

RSCL (Pin 23) is the clock output pin used to set the I/O timing of serial data sent to the external EEPROM. Data is taken from the RSDA pin when the clock signal rises, and data is output to the RSDA pin when the clock signal falls.

(k) External ROM I/F serial I/O pin (RSDA)

This is the I/O pin for serial data sent to the external EEPROM. It is necessary to switch the input to the RSDA (Pin 69) while the signal level of RSCL is low.

2. Pipeline Delay of the RGB and OSD Signals

The pipeline delay for the I/O of the RGB signals is 32 clock cycles of the master clock. In addition, the pipeline delay for the OSD, YS and YM signals is 25 clock cycles of the master clock.

3. Serial Bus

The serial bus of this IC consists of a host I/F, external ROM I/F and register I/F.

3-1. Host I/F

With this IC, each register setting and data set to built-in RAM are performed over a serial bus. Bus protocol conforms to I^2C bus specifications. Note that this IC does not support multi-slave functions, and that the bus should be independent from ICs having the other I^2C bus specification. Also, when accessing gamma RAM, always access memory address from odd addresses in 2-byte units. The following restrictions are placed on the host I/F of this IC.

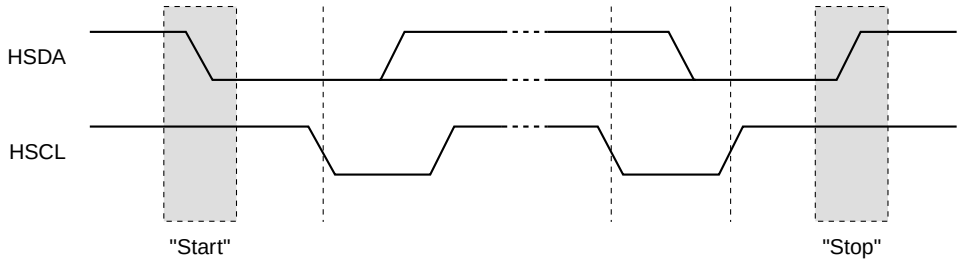
- Only I^2C bus slave operations are performed.
- Standard mode and fast mode are supported. Hs mode is not supported.
- Multi-slave functions are not supported.
- The general call address and start byte of the slave address are not acknowledged.
- C bus compatibility is not supported.
- Acknowledgment is not performed for 10-bit slave addresses.
- Low is not asserted for HSCL. (Wait control is not performed.)

(1) "Start" conditions

Read and write operations enter "Start" status by switching HSDA input from high to low level while HSCL input is high.

(2) "Stop" conditions

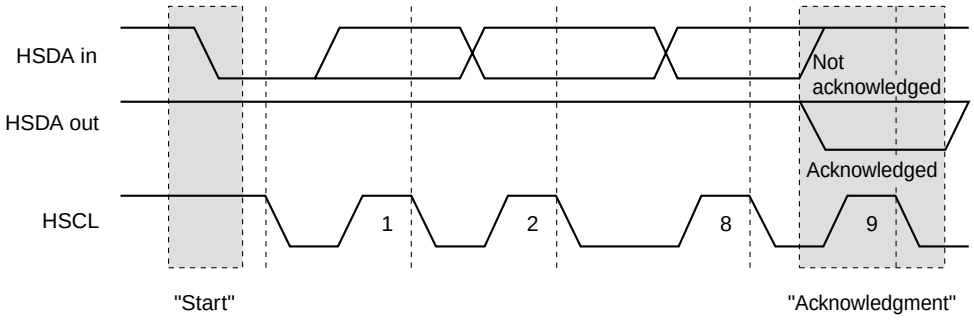
"Stop" results by switching HSDA input from low to high while HSCL input is high. Setting "Stop" status causes read processing to terminate during read operations, and causes the input of write data to terminate during write operations.



"Start" Conditions and "Stop" Conditions

(3) Acknowledgment

Acknowledgment is used to indicate whether or not data has been sent/received normally. The "Acknowledgment" of a data transfer is performed after that data transfer when the sender releases the bus on the 9th clock of HSCL and the receiver drives low. If the host is the receiver, the IC is informed by the host that data has ended by the fact that "Acknowledgment" is not generated for the last data sent from the IC.



Acknowledgment on the I²C Bus

(4) Slave address specification

After "Start" is sent, a 7-bit slave address and 1-bit read/write code is sent. Read/write operations with this IC start if the input slave address matches the device address set using HSEL. If the device address does not match, "Acknowledgment" is not generated and the system does nothing.

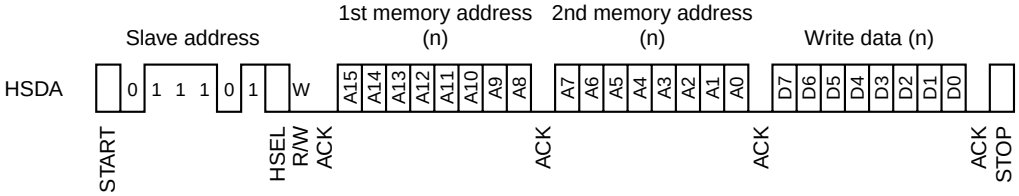
Slave Address Word (8 bits)							
Device Code (fixed)						Device Select	R/W Code
0	1	1	1	0	1	HSEL	R/W

* If R/W = 1, read results, if R/W = 0, write results.

Slave Address Specification

(5) Byte write operation

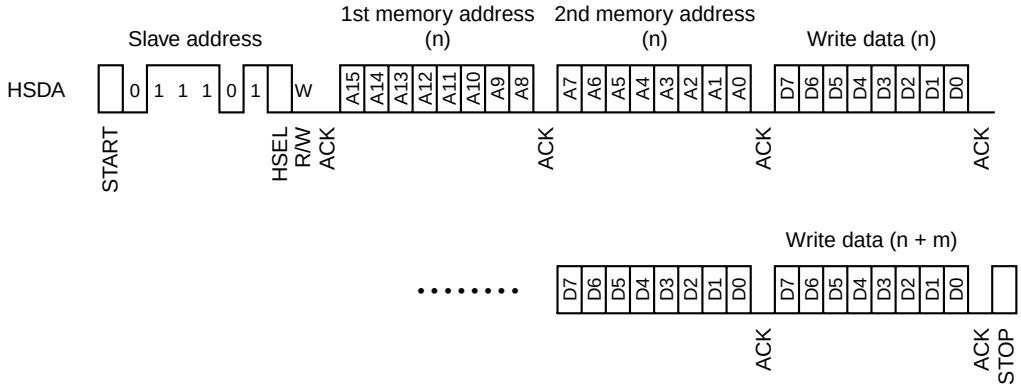
After "Start" is sent, the R/W code is set to low and an 8-bit device address word is input. The IC outputs "Acknowledgment" on the 9th bit and enters write mode. After this, "Acknowledgment" is output every 8 bits after each of the two 8-bit memory addresses are input. Next, "Acknowledgment" is output after 8 bits of write data is input and written to the IC.



Byte Write Operation

(6) Continuous write operation

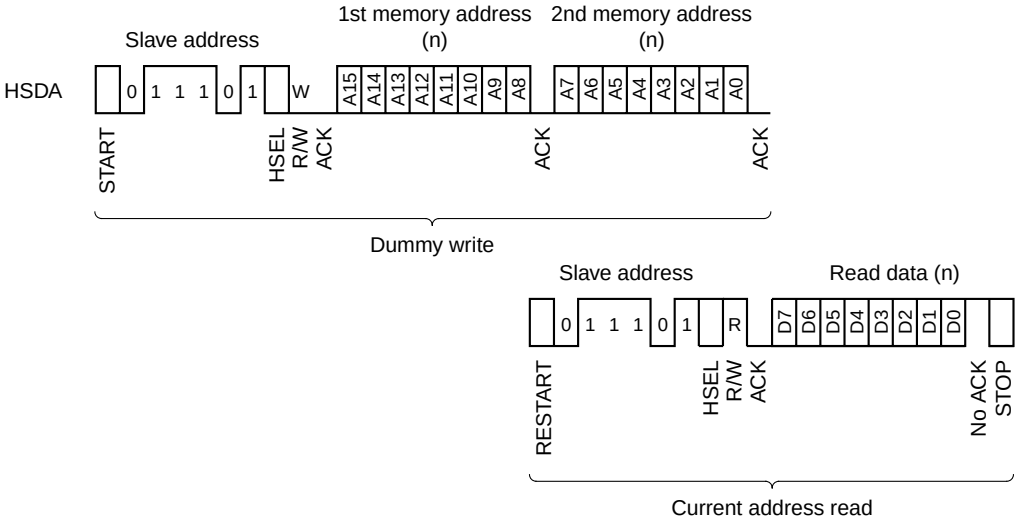
This IC possesses a function which can write data continuously. With the continuous write operation, write data is written in a manner similar to the byte write operation. Continuous write is possible by sending write data continuously before sending "Stop". The address used to write data during the continuous write operation is automatically incremented when each separate write operation terminates.
There is no limit on the number of continuous transfers that are possible to write continuously with this IC.



Continuous Write Operation

(7) Byte read operation

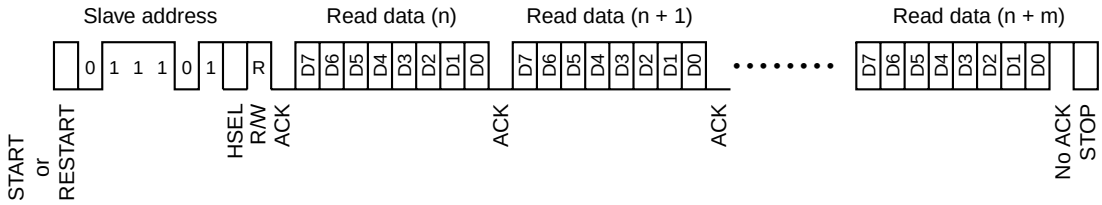
After "Start" is sent, the R/W code is set to low and an 8-bit device address word is input. The IC outputs "Acknowledgment" to the 9th bit and enters write mode. After this, "Acknowledgment" is output every 8 bits after each of the two 8-bit memory addresses are input. Once the addresses are acknowledgment, "Restart" is input, and the R/W code is set to high, an 8-bit device address word is input, and the IC outputs "Acknowledgment" to the 9th bit and enters read mode. Next, 8 bits of read data are output using the address used for the dummy write, and the read operation terminates if "Stop" is input without inputting "Acknowledgment".



Byte Read Operation

(8) Continuous read operation

This IC possesses a function which can read data continuously. With the continuous read operation, data up to the current address is read in a manner similar to the byte read operation. Continuous read is possible by receiving continuous read data and perform "Acknowledgment" before sending "Stop". The address used for reading data during the continuous read operation is automatically incremented when each separate read operation terminates.
There is no limit on the number of continuous transfers that are possible to read continuously with this IC.



Continuous Read Operation

3-2. Conditions for Accessing Gamma RAM and Color Shading RAM

With this IC, there are two way to access the internal RAM: by the host I/F using the serial bus and refresh/write-back for sending/receiving data via external ROM I/F. In the case of Gamma RAM, internal RAM must be accessed by the host I/F in 2-byte units, and memory address must be read from or written to odd memory addresses. Color shading RAM can be accessed in 1-byte units and there is no restriction on which addresses can be read or written.

It is possible to access internal RAM from each I/F when the conditions given in the following table are established.

GAM_ON	Vertical blanking period	Gamma RAM access
0	—	Yes
1	Vertical blanking period	Yes
1	Outside vertical blanking period	No

* GAM_ON represents the setting value of the DSD register.
* Gamma correction is not performed when GAM_ON is "0", and is performed when GAM_ON is "1".

Conditions for Accessing Gamma RAM

CSC_ON	Vertical blanking period	Color shading RAM access
0	—	Yes
1	Vertical blanking period	Yes
1	Outside vertical blanking period	No

* CSC_ON represents the setting value of the color shading register.
* Color shading correction is not performed when CSC_ON is "0", and is performed when CSC_ON is "1".

Conditions for Accessing Color Shading RAM

GAM_ON must be set to "0" when performing a write-back or forced refresh operation for Gamma RAM. Similarly, CSC_ON must be set to "0" when performing a write-back or forced refresh operation for color shading RAM.
In the case of a self-refresh operation, the start of vertical blanking period is automatically detected and operations start automatically at that time, regardless of how GAM_ON and CSC_ON are set. Therefore, be sure to set the external EEPROM transfer count register ROM_TRAN to fit within the vertical blanking period. Furthermore, the vertical blanking period for gamma is set using GAM_H1, GAM_H2, GAM_V1 and GAM_V2, while the vertical blanking period for color shading is set using CSC_HP, CSC_VP, CSC_HNUM, CSC_VNUM, CSC_HINT and CSC_VINT. Make all settings in accordance with the specifications of the video signal attempting to be displayed.

3-3. External ROM I/F

When operating the external ROM I/F, operations start by setting the serial bus register from the host I/F. The serial bus on the ROM side is used to access the external EEPROM. Bus protocol conforms to I^2C bus specifications. Also, the following restrictions are placed on the external ROM I/F of this IC.

- Only master operations are performed.
- Standard mode and fast mode are supported. Hs mode is not supported.
- Multi-master functions are not supported.
- The general call address and start byte of the slave address are not generated.
- C bus compatibility is not supported.
- A memory address space of up to 512K bytes is supported.
- Wait control by RSCL is not supported.
- 10-bit slave addresses are not supported.

(1) External ROM I/F clock settings

The frequency of the clock signal supplied to the external EEPROM by the RSCL pin is set using RSCL_SEL of the serial bus control registers. Set this value based on the operating frequency of the IC as given in the table below so that the frequency output by the RSCL pin is appropriate for the specifications of the external EEPROM.

RSCL_SEL	Operating frequency
00	35MHz or less
01	70MHz or less
10	94.5MHz or less
11	100MHz or less

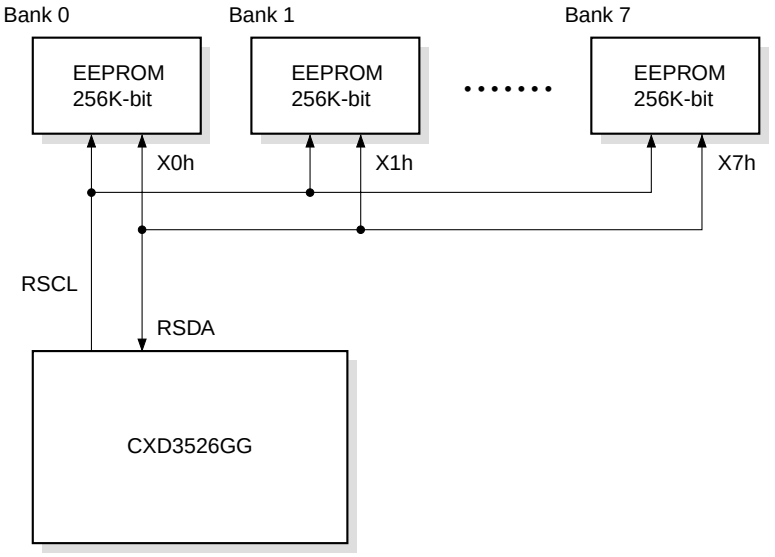
(2) External EEPROM memory capacity setting

With this IC, slave addresses and memory addresses are generated in accordance with the memory capacity set for the external EEPROM. The memory capacity of the external EEPROM is set using ROM_MAP of the serial bus control registers.

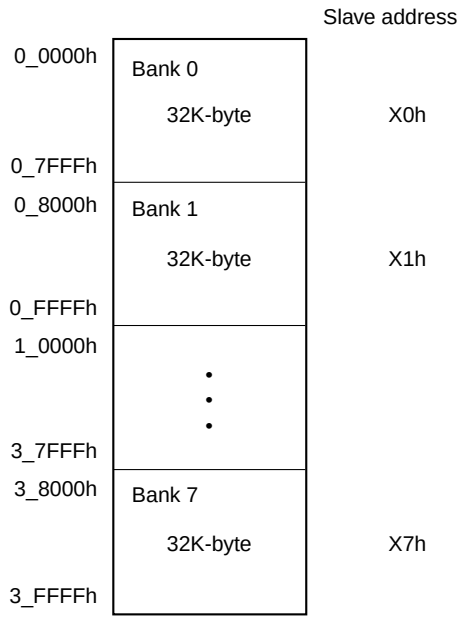
ROM_MAP	Usable memory size
00	512K-bit (65,536 × 8-bit)
01	256K-bit (32,768 × 8-bit)
10	128K-bit (16,384 × 8-bit)
11	64K-bit (8,192 × 8-bit)

[Example] Address output when using eight 256K-byte EEPROMs (ROM_MAP = 01)

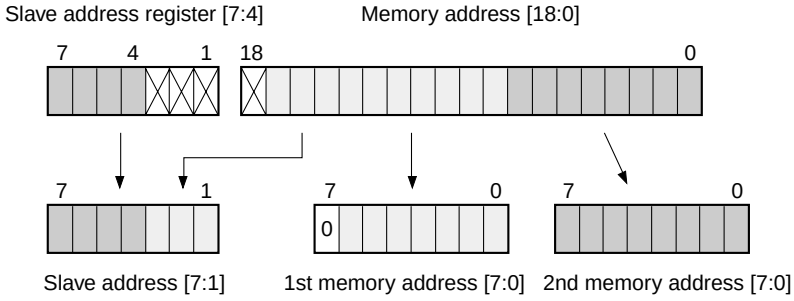
With this IC, the ROM slave address register setting [7:4] is set as is for the serial bus slave address [7:4], and the memory address [17:15] is used for the slave address [3:1]. The memory address [14:0] is used as is for the 1st and 2nd memory addresses. The 1st memory address [7] is fixed to all "0". Furthermore, up to eight external EEPROMs can be connected to this IC.



System Configuration Diagram

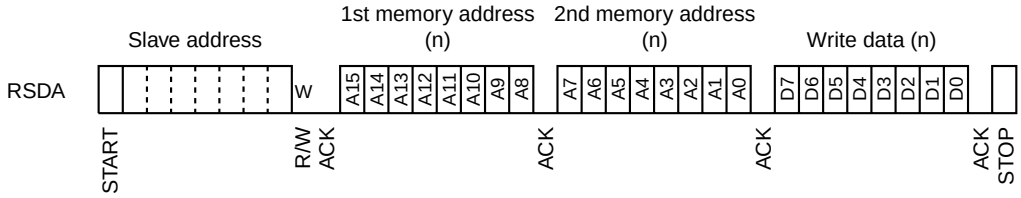


Memory Map
256K-byte space



(3) External ROM I/F slave address setting

The external ROM I/F of this IC transfers data into and out of memory using the serial bus as host I/F. Since operations conform to I^2C bus protocol just as with the host I/F, this section only describes the slave address. To access the external EEPROM, when access conditions are established, "Start" is sent, and then 7 bits representing the slave address are output, and the R/W code is output. "Acknowledgment" is received to the 9th bit from the external EEPROM, and the IC enters either read or write mode. The slave address is determined based on ROM_MAP of the serial bus ROM I/F control register and RSLV_ADDR of the serial bus ROM slave address register as previously described.
The user should set the upper 4 bits of the device address of the EEPROM to be used in RSLV_ADDR and the memory size in ROM_MAP. This allows memory to be used without awareness of memory boundaries of actual memory used for the setting memory space.



Byte Write Operation

(4) Memory location and data size setting for the external EEPROM

Since this IC performs refresh and write-back operations, it is necessary to set which addresses of the external EEPROM gamma data and color shading data have been located in.
The registers used to make these settings are the external EEPROM gamma data start address register and the external EEPROM color shading data start address register. By specifying the starting position of the data area in these registers data access from the specified addresses is possible during refresh or write-back operation.
Units of 1K-byte can be used to set the start addresses which can be set in these registers.

In addition, the size of data transferred during refresh and write-back operations is fixed at 2K bytes for each color in the case of gamma data. The number of bytes transferred in the case of color shading data is the value stored in the color shading data size register plus one.

(5) Refresh and write-back operations

This IC includes a function that allows an external EEPROM to automatically refresh the internal RAM. This function has the four modes described below.

- Self-refresh mode
- Forced refresh mode
- Write-back mode
- Refresh stop mode

Each mode is started by writing the specified mode into REF_MODE of the refresh register.

In self-refresh mode, the IC detects that the vertical blanking period has been entered and, using the value specified in the external EEPROM transfer count register, uses the continuous read operation to transfer data of the size "transfer count plus 1" to the external ROM I/F. The data read using the continuous read transfer is written into the internal RAM.
When the transfer of the all data for the data size is completed, the access area for the internal RAM is changed, continuous read transfer is executed indefinitely until self-refresh mode is exited, and refresh operations are automatically carried out on the internal RAM.

In forced refresh mode, continuous read transfer from the external EEPROM is performed for the RAM area specified by REF_RSEL of the refresh RAM select register, and the read data is written to the internal RAM. When the transfer of all data for the specified RAM area is completed, REF_END of the refresh status register set to a flag indicating the operation has ended, and operations stop.
If forced refresh operations are to be performed for the entire internal RAM, first set the refresh RAM select register to gamma RAM (R) and perform the forced refresh operation. Since the refresh RAM select register is automatically set to the next RAM area after all data is transferred, refresh for the entire RAM can be completed by repeating the forced refresh operation five times.

In write-back mode, continuous write transfer is performed from the RAM area specified by REF_RSEL of the refresh RAM select register to the external EEPROM. When the transfer of all data for the specified RAM area is completed, REF_END of the refresh status register set to a flag indicating the operation has ended, and operations stop.
If write-back operations are to be performed for the entire internal RAM, first set the refresh RAM select register to gamma RAM (R) just as for forced refresh operation, and then perform the write-back operation. Since the refresh RAM select register is automatically set to the next RAM area after all data is transferred, write-back for the entire RAM can be completed by repeating the write-back operation five times.

In refresh stop mode, the external ROM I/F does not operate and nothing is output on the serial bus.

(6) Forced reset of the external ROM I/F control circuit

With this IC, forced reset is possible in case a problem occurs with the external ROM I/F and the internal circuit becomes locked. Forced reset initializes only the external ROM I/F control circuit by writing "1" to ROM_RST of the refresh register. Normal operations are allowed after initialization is complete.

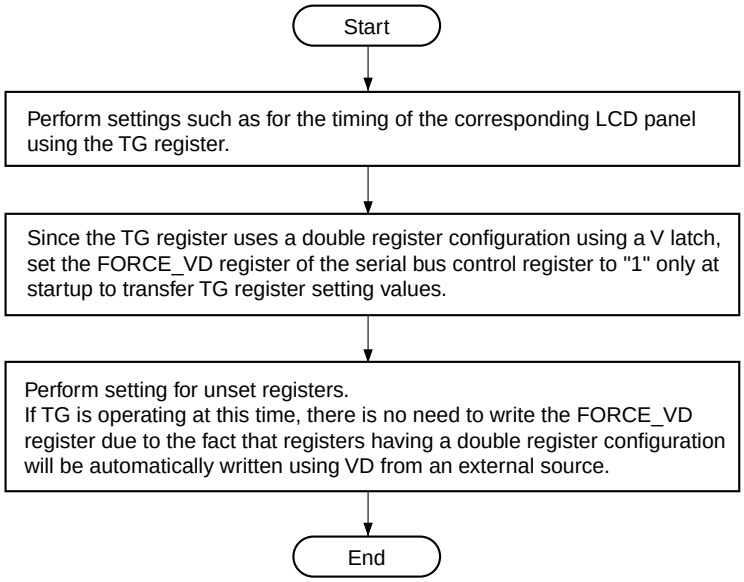
3-4. Register I/F Control Circuit

The register I/F control circuit transfers data between the host I/F and the external ROM I/F. Register data other than RAM data is stored here. Since registers have a double buffer configuration, data in the first buffer is synchronized with the internal VD and reflected in the second buffer, while data in the second buffer is input to each block. Note, however, that data in the serial bus control register has a single buffer configuration.

3-5. Software Flow

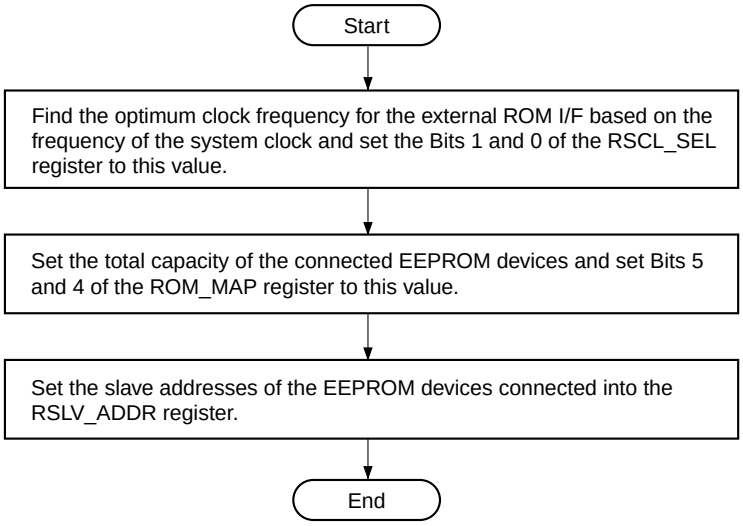
(1) Settings when power is turned on

The following procedure is the setting procedure first performed after power of the IC is turned on. If this procedure is not executed, the internal VD will not be generated and register data cannot be set correctly.



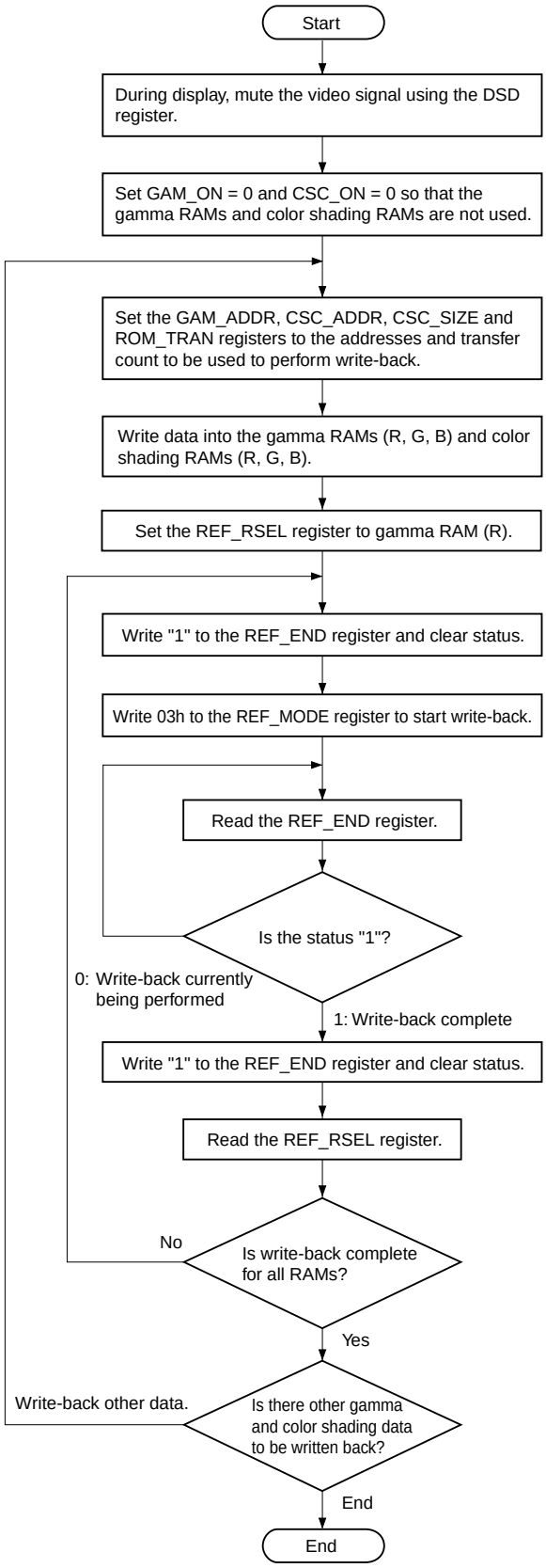
(2) Setting procedure of the serial bus control register

The following procedure is the procedure for setting the serial bus control register in accordance with the external EEPROM to which the IC is connected. Be sure to make settings according to the operating frequency of the IC and the speed, capacity and number of external EEPROMs that are connected.



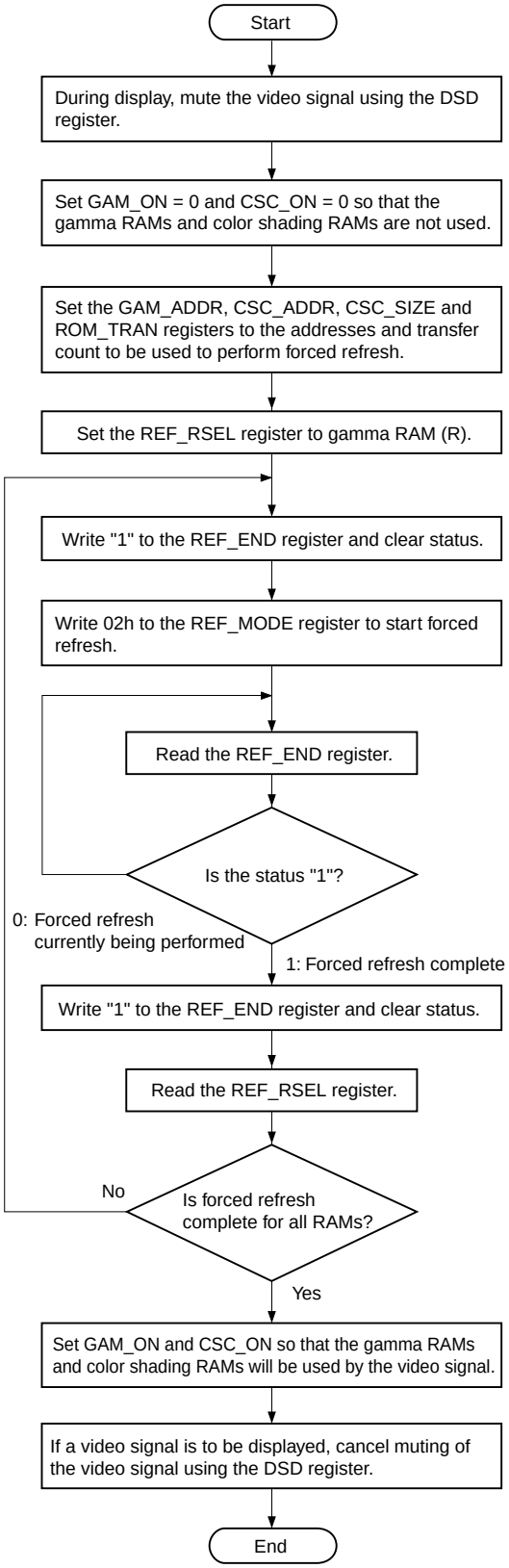
(3) Write-back procedure

The following procedure is the procedure for writing gamma correction and color shading correction data back to the external EEPROM.



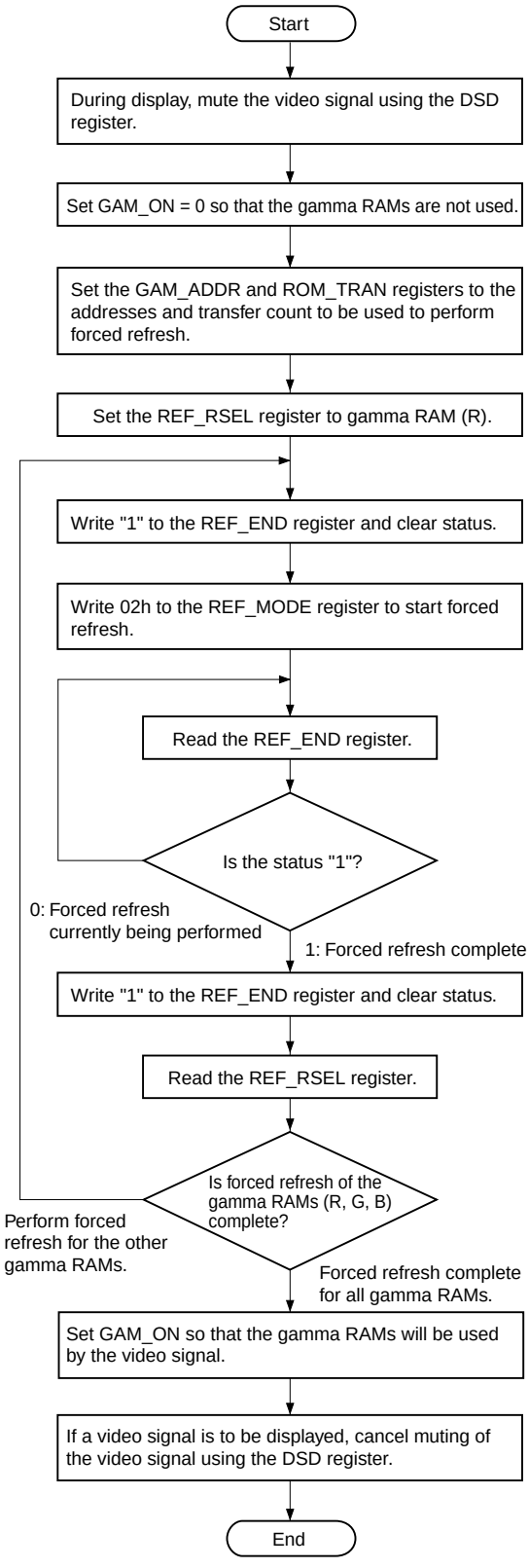
(4) Forced refresh procedure during power-on

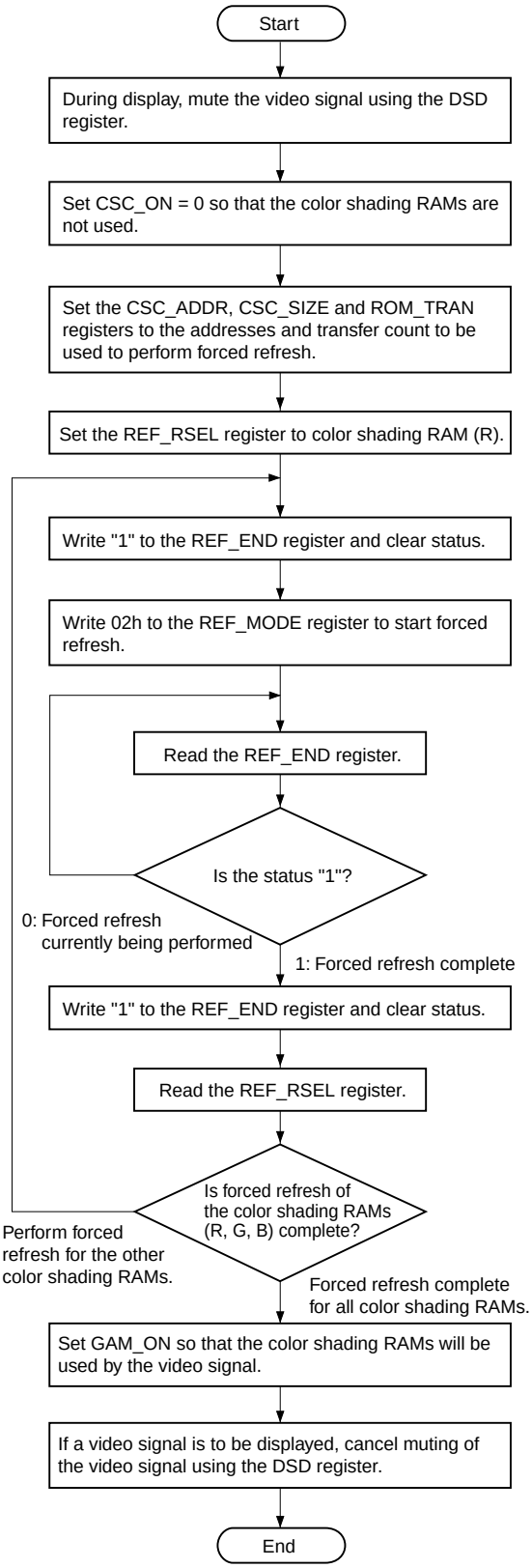
The following procedure is the procedure for setting gamma correction and color shading correction data from an external EEPROM for forced refresh when power is turned on.



(5) Procedure for forced refresh during normal operations

The following procedure is the procedure for selecting either gamma correction or color shading correction data during normal operations.

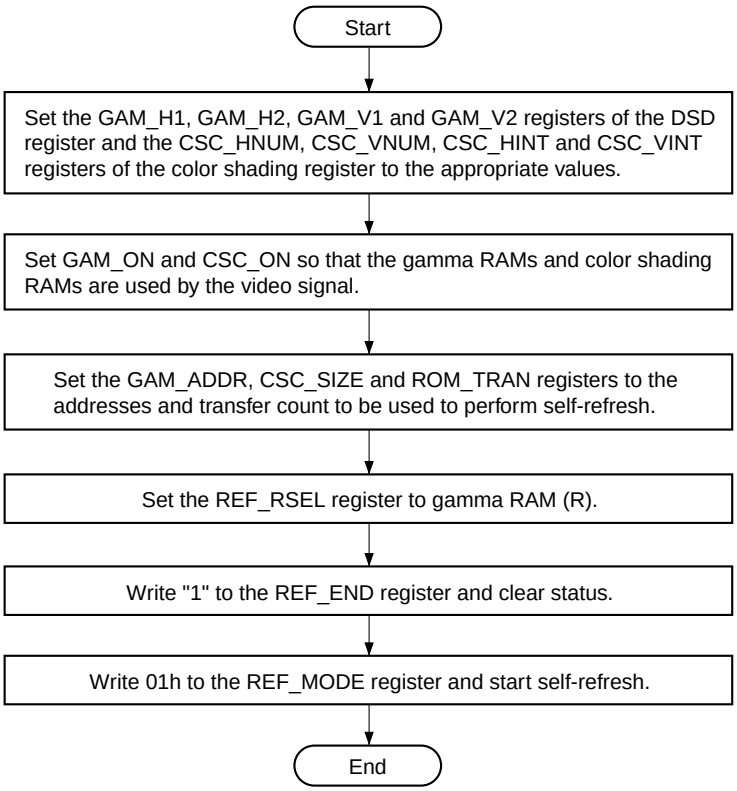




(6) Procedure for self-refresh during normal operations

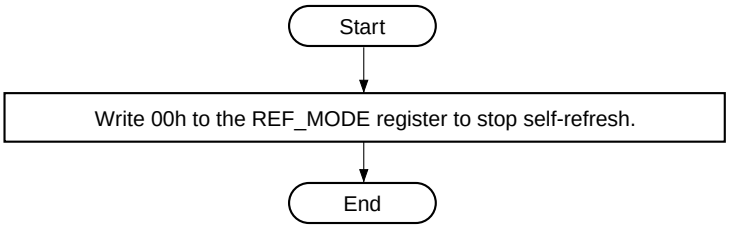
• Starting the refresh operation

The following procedure is the procedure used to set cyclic refreshing of the gamma correction and color shading correction data stored in the built-in RAM during normal operations.



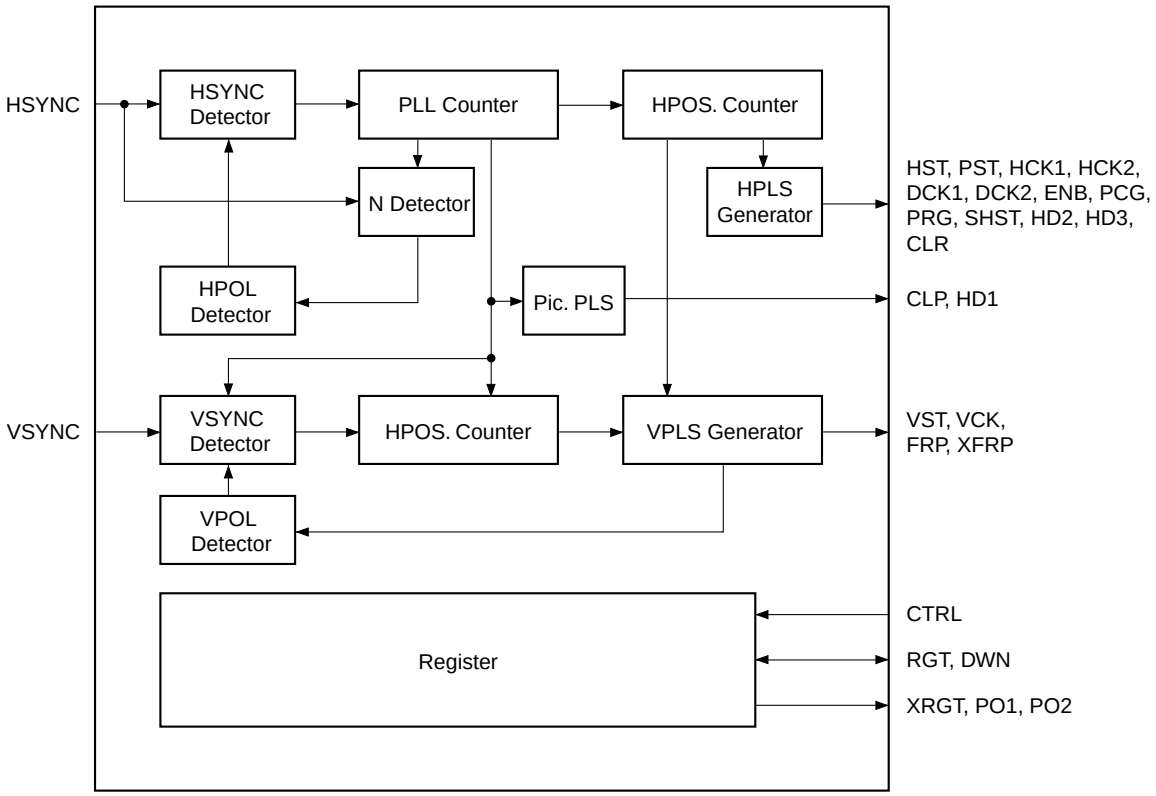
• Stopping the refresh operation

The following procedure is the procedure used to stop the self-refresh operation.



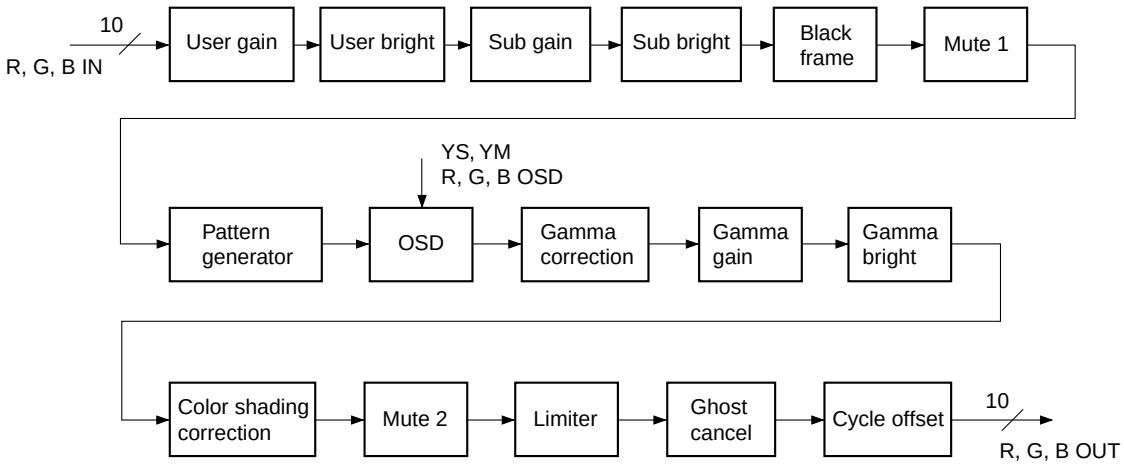
4. Timing Generator (TG) Block

This block generates the timing pulses required to drive Sony LCD panels. Of the output pulses, the required pulses differ according to the LCD panel type, so be sure to also check the specifications of the panel used. The output timing pulses are all set by the serial bus. For a detailed description, see the description of the TG block register setting.



5. DSD Block

The DSD block signal processing flow is shown below.



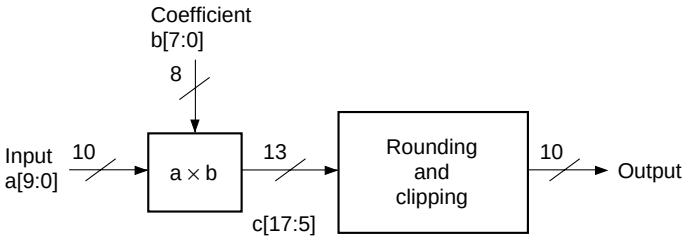
The various signal processing functions are described below. Note that the coefficients used for each arithmetic operation are set through the host I/F. See the descriptions of the DSD block register setting.

(a) User gain

This block performs multiplication processing as the user control gain adjustment. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 3.984375 (= 255/64) times, variable in 256 steps
(Settings shared by R, G and B)

Multiplication is performed using the 10-bit input and an 8-bit coefficient, and the upper 13 bits c[17:5] of the operation results are output. Next, the c[5] value is checked and rounding is performed to 12 bits. The upper 2 bits of the rounded 12 bits is checked, clipping is performed, and the lower 10 bits are output.

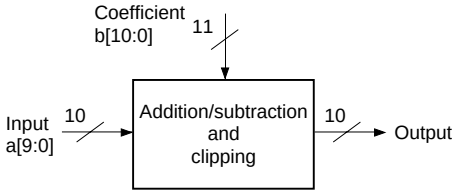


(b) User bright

This block performs addition and subtraction processing as the user control bright adjustment. The settings are as follows.

Coefficient: 11 bits with code, MSB = code bit
Bright setting: –1024 to +1023 graduation, variable with an accuracy of 1 bit
(Settings shared by R, G and B)

Multiplication is performed using the 10-bit input and an 11-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[10] = 0, and subtraction when b[10] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.

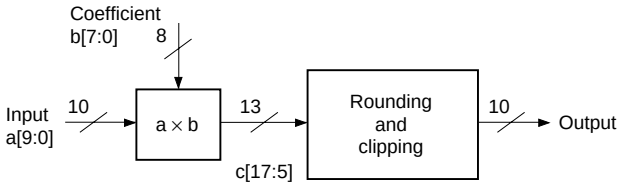


(c) Sub gain

This block performs multiplication processing as the white balance gain adjustment. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 3.984375 (255/64) times, variable in 256 steps
(Set independently for R, G and B)

Multiplication is performed using the 10-bit input and an 8-bit coefficient, and the upper 13 bits c[17:5] of the operation results are output. Next, the c[5] value is checked and rounding is performed to 12 bits. The upper 2 bits of the rounded 12 bits is checked, clipping is performed, and the lower 10 bits are output.

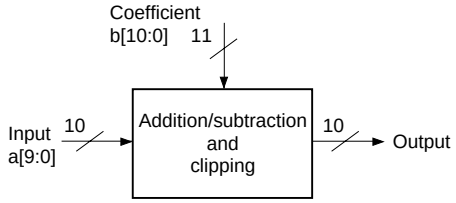


(d) Sub bright

This block performs addition and subtraction processing as the white balance bright adjustment. The settings are as follows.

Coefficient: 11 bits with code, MSB = code bit
Bright setting: –1024 to +1023 graduation, variable with an accuracy of 1 bit
(Set independently for R, G and B)

Multiplication is performed using the 10-bit input and an 11-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[10] = 0, and subtraction when b[10] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.

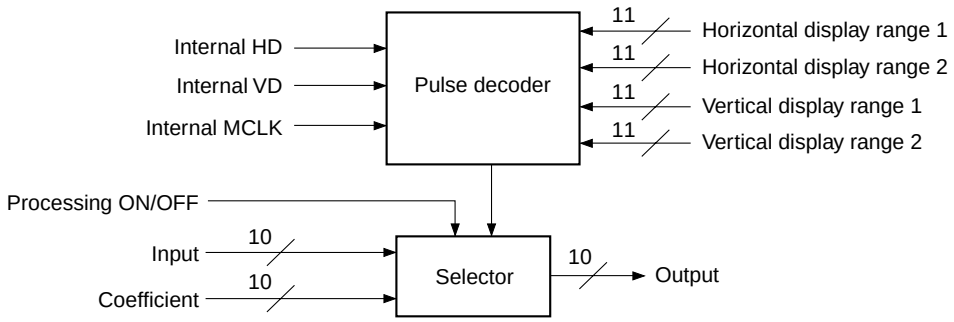


(e) Black frame

This block performs processing to fix the blanking period of the video signal to the desired level regardless of the front-end signal processing results.
If the number of pixels calculated from the effective period of the video signal to be displayed is less than the number of pixels of the LCD panel on which the signal is to be displayed, the blanking period of the video signal is displayed in the excess pixels. At this time, the displayed blanking period can be fixed to the desired level regardless of the gain and bright adjustment or other picture quality adjustment results by processing with this block. The settings are as follows.

FRM_ON: 1 = Black frame processing ON, 0 = OFF
FRM_DAT: Black frame level setting
FRM_H1, FRM_H2: Set the black frame horizontal display range in 1-dot units
FRM_V1, FRM_V2: Set the black frame vertical display range in 1-line units
(All settings shared by R, G and B)

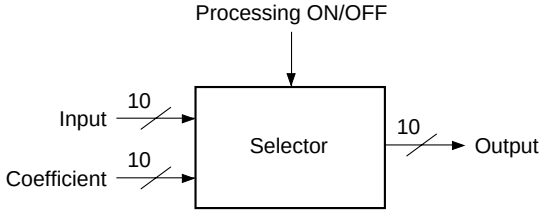
Here, the desired range of the video signal is replaced with 10-bit data (FRM_DAT) by switching the video signal and the coefficients using the pulse output from the pulse decoder.



(f) Mute 1

This block performs mute processing by replacing the video signal with data of the desired level. The settings are as follows.

MUTE1_ON: 1 = Mute processing ON, 0 = OFF (Settings shared by R, G and B)
R, G, B_MUTE1: RGB mute data (Set independently for R, G and B)



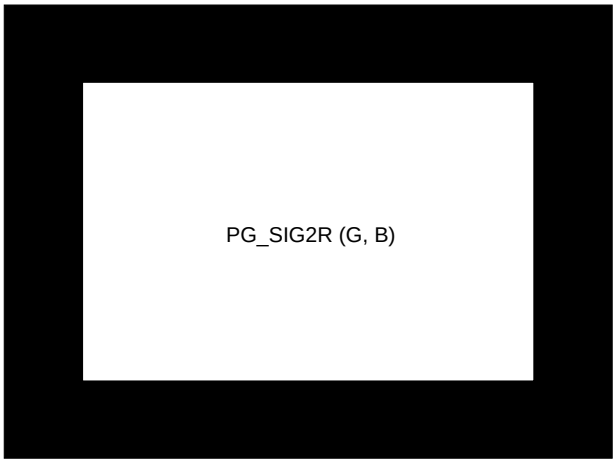
(g) Pattern generator

This block generates and outputs the set fixed pattern independently of the input signal. This function is valid when PG_ON = 1. When PG_R (G, B)_ON is "0", the signal level goes to 000h respectively for R, G and B.
The raster display pattern is displayed in the effective area, and all other display patterns are displayed in the window area. Here, the effective area is set by PG_HST, PG_HSTP, PG_VST and PG_VSTP, and the window area is set by PG_HWST, PG_HWSTP, PG_VWST and PG_VWSTP.
The display pattern signal level is set independently for R, G and B by PG_SIG1R (G, B)[9:0] and PG_SIG2R (G, B)[9:0]. Within the effective area, the pattern and non-pattern signal levels can be switched by PG_R (G, B)_SEL. At this time, the signal level outside the effective area goes to 000h. During horizontal ramp, horizontal stair, vertical ramp and vertical stair display, the PG_SIG1R (G, B)[9:0] and PG_SIG2R (G, B)[9:0] settings are invalid.

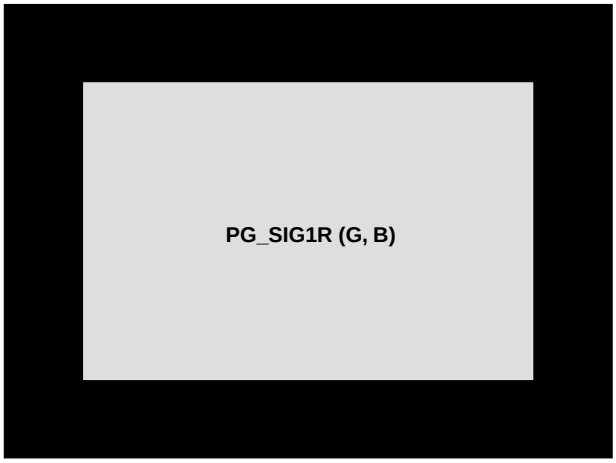
The display patterns and signal levels are as follows.

(1) Raster display

When PG_PAT[2:0] = 0h, a raster is displayed.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	0h
PG_STRP_SW	x
PG_STAIR_SW	x

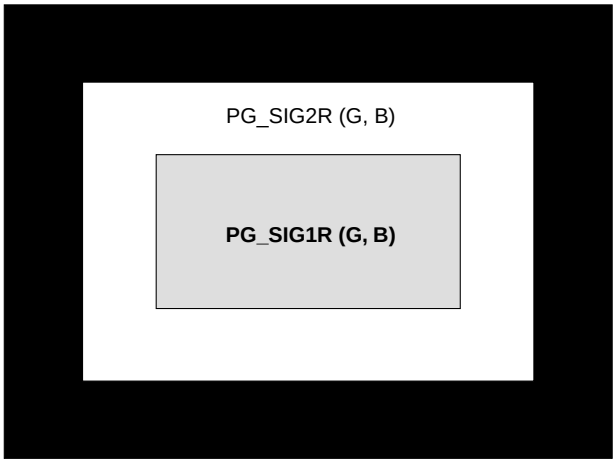


PG_R (G, B)_SEL	1
PG_PAT[2:0]	0h
PG_STRP_SW	x
PG_STAIR_SW	x

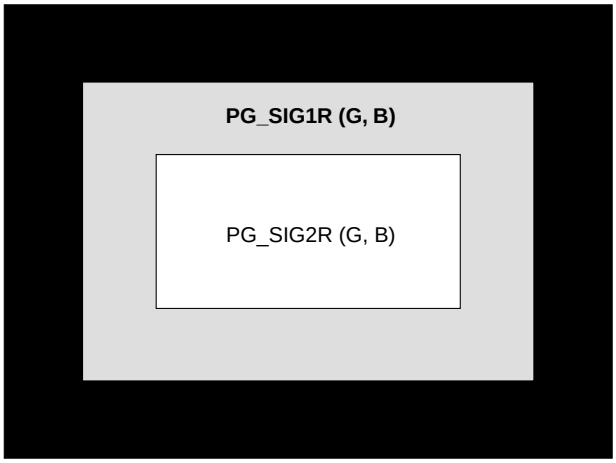
x: Don't care

(2) Window display

When PG_PAT[2:0] = 1h, a window is displayed.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	1h
PG_STRP_SW	x
PG_STAIR_SW	x

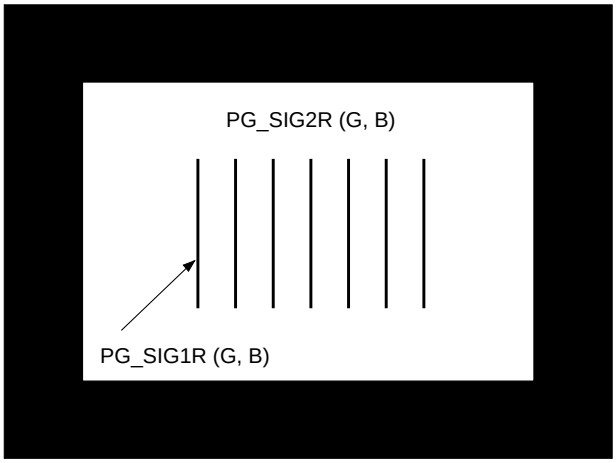


PG_R (G, B)_SEL	1
PG_PAT[2:0]	1h
PG_STRP_SW	x
PG_STAIR_SW	x

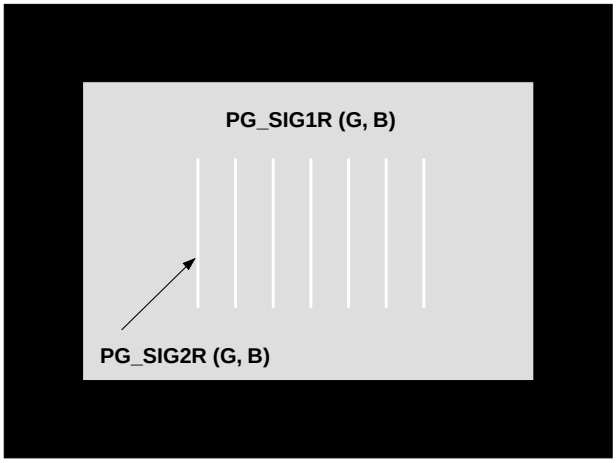
x: Don't care

(3) Vertical stripe display

When PG_PAT[2:0] = 2h and PG_STRP_SW = 0, vertical stripes are displayed.
The stripe period is set by PG_STEP in 1-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	2h
PG_STRP_SW	0
PG_STAIR_SW	x

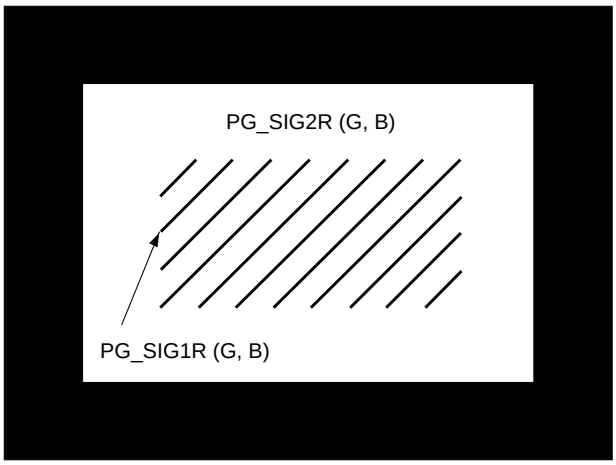


PG_R (G, B)_SEL	1
PG_PAT[2:0]	2h
PG_STRP_SW	0
PG_STAIR_SW	x

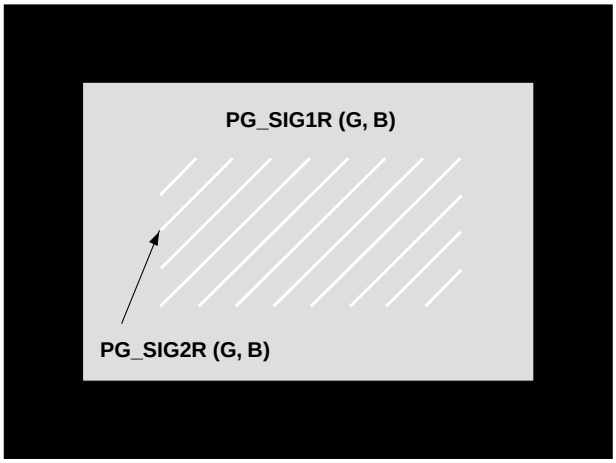
x: Don't care

(4) Diagonal stripes display

When PG_PAT[2:0] = 2h and PG_STRP_SW = 1, diagonal stripes are displayed.
The stripe period is set by PG_STEP in 1-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	2h
PG_STRP_SW	1
PG_STAIR_SW	x

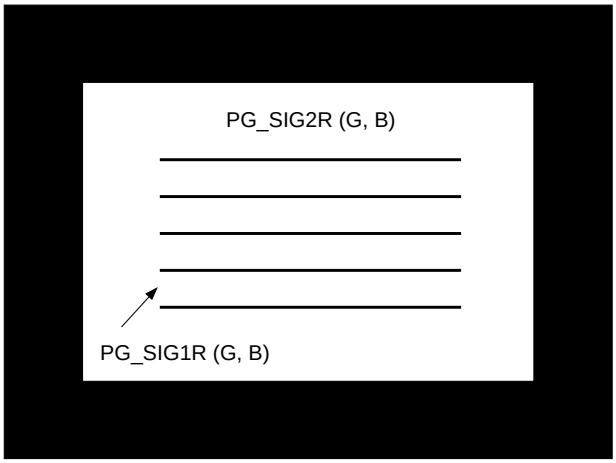


PG_R (G, B)_SEL	1
PG_PAT[2:0]	2h
PG_STRP_SW	1
PG_STAIR_SW	x

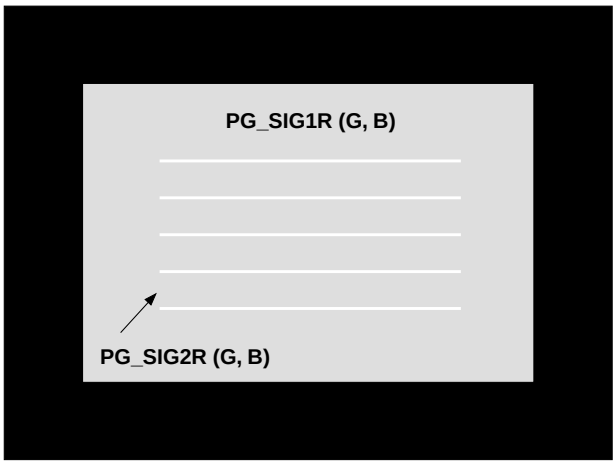
x: Don't care

(5) Horizontal stripes display

When PG_PAT[2:0] = 3h, horizontal stripes are displayed.
The stripe period is set by PG_STEP in 1-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	3h
PG_STRP_SW	x
PG_STAIR_SW	x

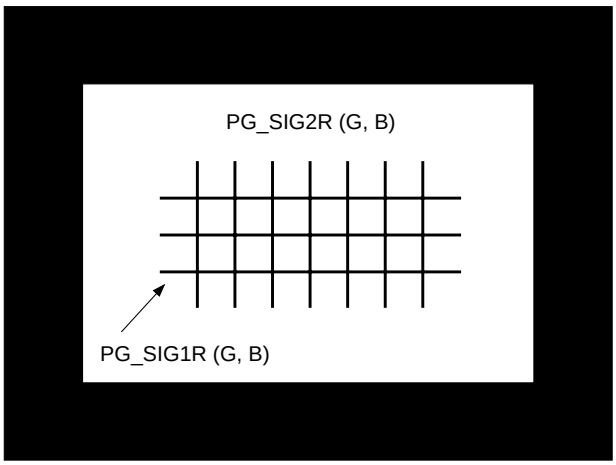


PG_R (G, B)_SEL	1
PG_PAT[2:0]	3h
PG_STRP_SW	x
PG_STAIR_SW	x

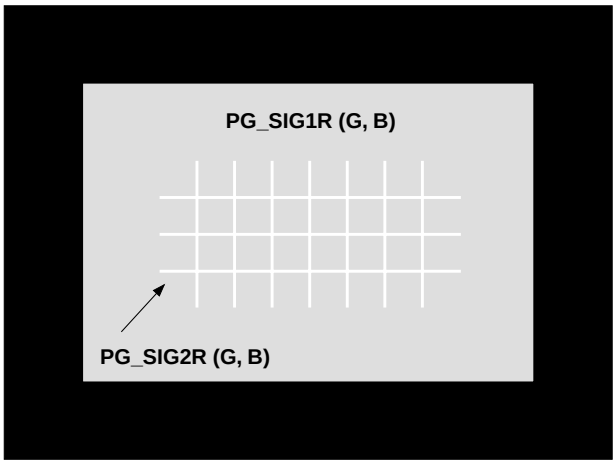
x: Don't care

(6) Cross hatch display

When PG_PAT[2:0] = 4h, a cross hatch is displayed.
The stripe period is set by PG_STEP in 1-dot units. The stripe width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	4h
PG_STRP_SW	x
PG_STAIR_SW	x

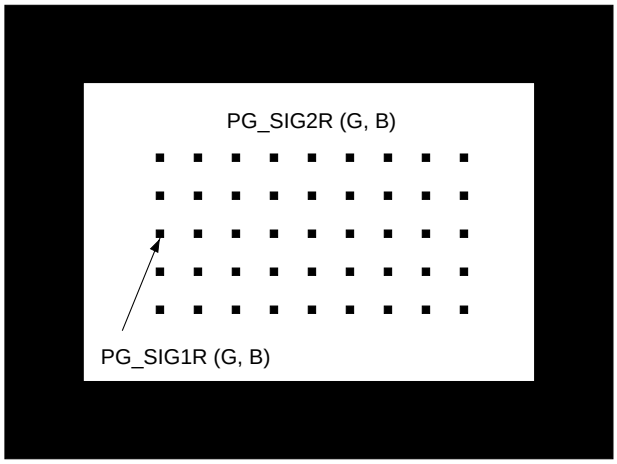


PG_R (G, B)_SEL	1
PG_PAT[2:0]	4h
PG_STRP_SW	x
PG_STAIR_SW	x

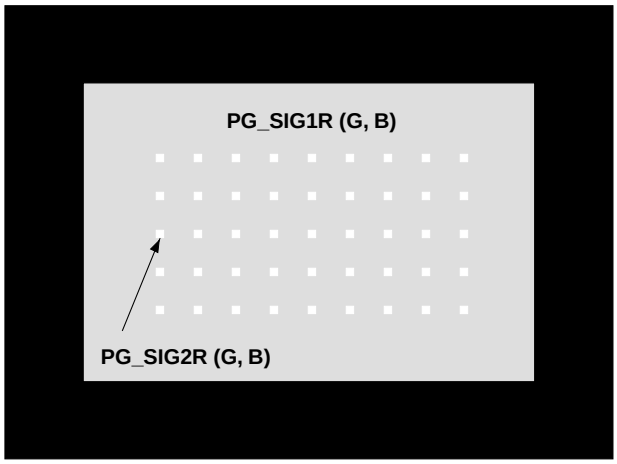
x: Don't care

(7) Dots display

When PG_PAT[2:0] = 5h, a dot pattern is displayed.
The dot period is set by PG_STEP in 1-dot units. The dot width is set by PG_WIDTH in 1-dot units.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	5h
PG_STRP_SW	x
PG_STAIR_SW	x

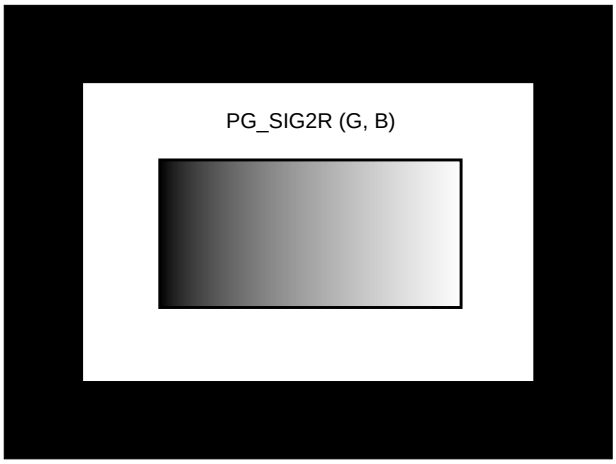


PG_R (G, B)_SEL	1
PG_PAT[2:0]	5h
PG_STRP_SW	x
PG_STAIR_SW	x

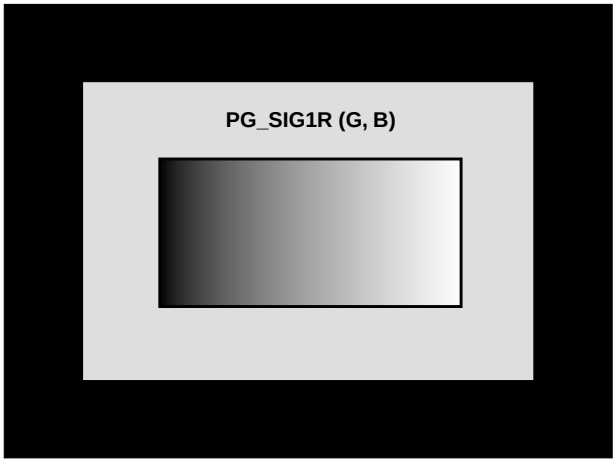
x: Don't care

(8) Horizontal ramp display

When PG_PAT[2:0] = 6h and PG_STAIR_SW = 0, a horizontal ramp is displayed.
The signal level is incremented from 000h by one graduation for each dot.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	0

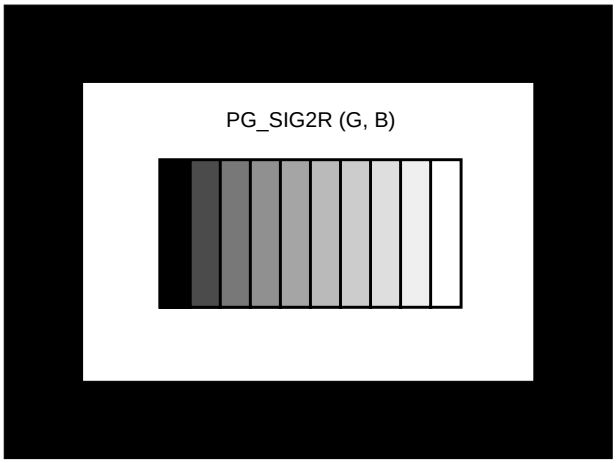


PG_R (G, B)_SEL	1
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	0

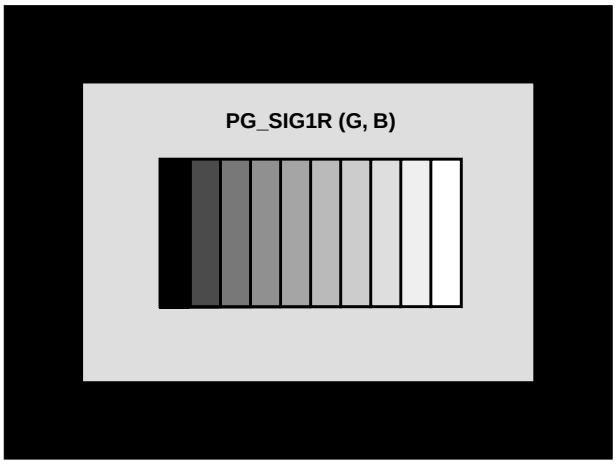
x: Don't care

(9) Horizontal stair display

When PG_PAT[2:0] = 6h and PG_STAIR_SW = 1, a horizontal stair is displayed.
The signal level is incremented from 000h by 64 graduation for each 64 dots.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	1

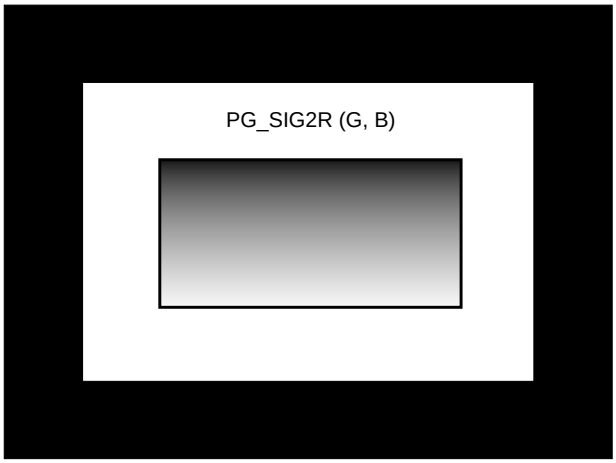


PG_R (G, B)_SEL	1
PG_PAT[2:0]	6h
PG_STRP_SW	x
PG_STAIR_SW	1

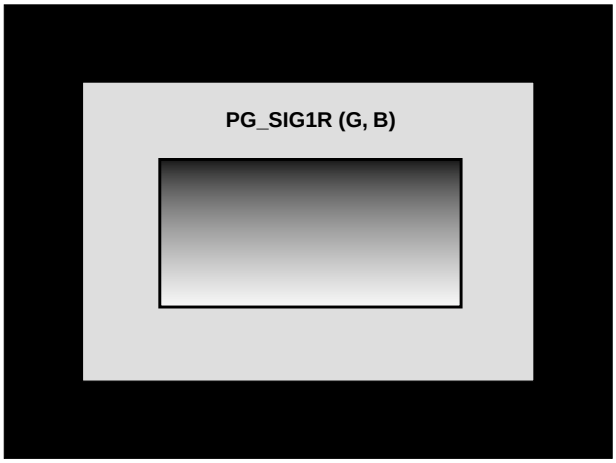
x: Don't care

(10) Vertical ramp display

When PG_PAT[2:0] = 7h and PG_STAIR_SW = 0, a vertical ramp is displayed.
The signal level is incremented from 000h by one graduation for each line.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	0

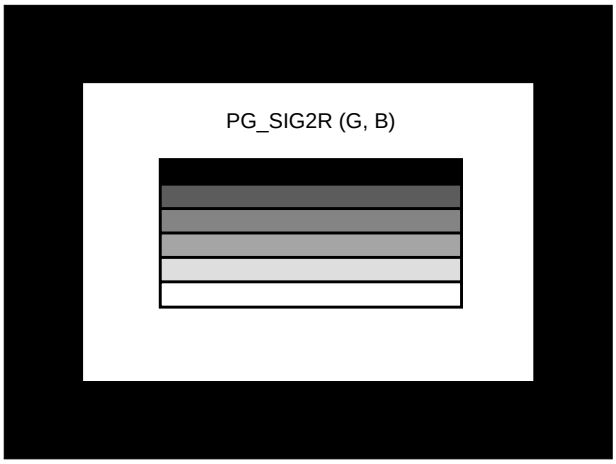


PG_R (G, B)_SEL	1
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	0

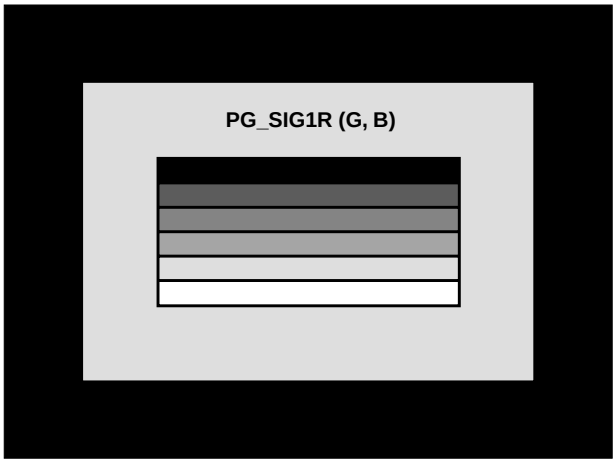
x: Don't care

(11) Vertical stair display

When PG_PAT[2:0] = 7h and PG_STAIR_SW = 1, a vertical stair is displayed.
The signal level is incremented from 000h by 64 graduation for each 32 lines.



PG_R (G, B)_SEL	0
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	1



PG_R (G, B)_SEL	1
PG_PAT[2:0]	7h
PG_STRP_SW	x
PG_STAIR_SW	1

x: Don't care

(h) OSD

This block performs video signal half-tone processing and OSD_MIX processing by inputting the 2-bit OSD signal for each color and the YS and YM signals. The half-tone processing setting is as follows.

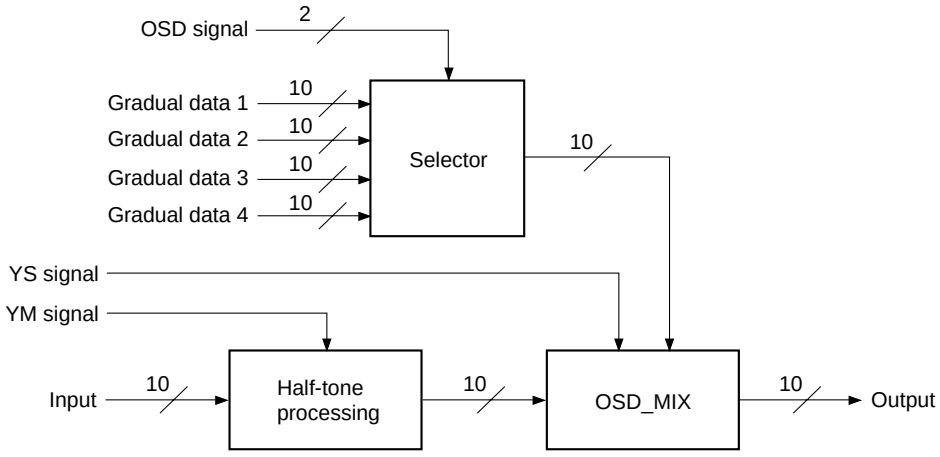
YM signal input: 1 = Half-tone processing ON, 0 = OFF

Here, the video signal level is halved by shifting the input data by one bit to the LSB side when YM = 1. For example, when 0F0h is input, 078h is output.
The selector selects one of four types of data with respect to the OSD signal value as shown in the table below. The selected data becomes the OSD signal gradual data. The selected gradual data can be set independently in 10 bits for R, G and B, so 4 graduation can be selected as desired from among 1024 graduation for each of R, G and B. Therefore, the desired 64 (= 2^6) colors can be selected from among the total 1.07374 billion (= 2^30) colors for R, G and B.

OSD signal input	Selected gradual data
0h	R, G, B_OSD_DAT1
1h	R, G, B_OSD_DAT2
2h	R, G, B_OSD_DAT3
3h	R, G, B_OSD_DAT4

The OSD_MIX processing setting is as follows.

YS signal input: 1 = OSD_MIX processing ON, 0 = OFF

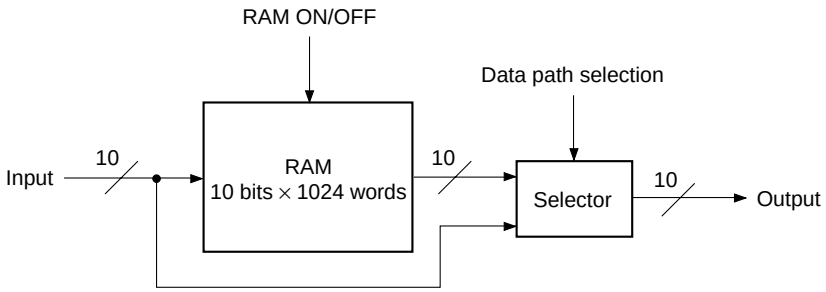


(i) Gamma correction

This block performs gamma correction for the user- and white balance-adjusted signal. Gamma correction uses the LUT system, and the RAM size is 10 bits × 1024 words. The settings are as follows.

GAM_ON: 1 = Gamma correction processing ON, 0 = Gamma correction processing OFF
GAM_MODE: 1 = Normal operation mode, 0 = Power-saving mode
GAM_H1, GAM_H2: 1 = Gamma correction processing range is set in 1-dot units
GAM_V1, GAM_V2: 1 = Gamma correction processing range is set in 1-line units
(All settings shared by R, G and B)

When operating the RAM, be sure to set GAM_MODE = 1. Data cannot be written to or read from the RAM in power-saving mode. The RAM data is set through the host I/F block or external ROM I/F.
Set gamma correction processing range (effective period of video signal) to GAM_H1 and GAM_H2, and GAM_V1, GAM_V2. This setting enables access to RAM from serial bus.
Note that the RAM output is undetermined during power-on.

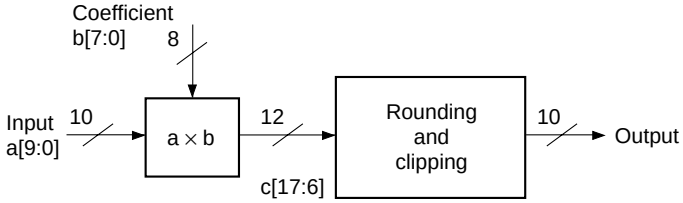


(j) Gamma gain

This block performs multiplication processing to correct VT curve variation of the LCD panel as gain adjustment for the gamma corrected signal. The settings are as follows.

Coefficient: 8 bits
Gain setting: 0 to 1.9921875 (= 255/128) times, variable in 256 steps
(Set independently for R, G and B)

Multiplication is performed using the 10-bit input and an 8-bit coefficient, and the upper 12 bits c[17:6] of the operation results are output. Next, the c[6] value is checked and rounding is performed to 11 bits. The MSB of the rounded 11 bits is checked, clipping is performed, and the lower 10 bits are output.

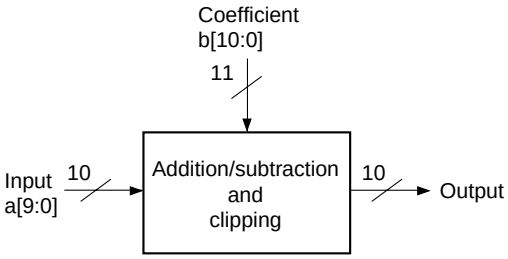


(k) Gamma bright

This block performs addition and subtraction processing to correct VT curve variation of the LCD panel as bright adjustment for the gamma corrected signal. The settings are as follows.

Coefficient: 11 bits with code, MSB = code bit
Bright setting: –1024 to +1023 graduation, variable with an accuracy of 1 bit
(Set independently for R, G and B)

Multiplication is performed using the 10-bit input and a 11-bit coefficient with code. The coefficient MSB is the code bit. Addition is performed when b[10] = 0, and subtraction when b[10] = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.



(I) Color shading correction

This block corrects color shading by adding a correction signal to the video signal. Correction points are set at fixed intervals in the horizontal, vertical and gradual directions of the video signal. The correction data for these correction points is written in the RAM, and a correction curve is created by reading this data and performing interpolation operations. The settings are as follows.

CSC_ON: 1 = Color shading correction processing ON, 0 = Processing OFF
CSC_R (G, B)_RGT*: 1 = Reflects the TG block RGT setting,
0 = Reflects the inverse of the TG block RGT setting
CSC_DWN: 1 = Reflects the TG block DWN setting,
0 = Reflects the inverse of the TG block DWN setting
CSC_HP: Sets the horizontal correction start position
CSC_VP: Sets the vertical correction start position
CSC_HNUM: Sets the number of horizontal correction points
CSC_VNUM: Sets the number of vertical correction points
CSC_HINT: Sets the horizontal correction interval
CSC_VINT: Sets the vertical correction interval
CSC_HOS: Sets the expansion of the horizontal correction area
CSC_VOS: Sets the expansion of the vertical correction area
CSC_GNUM: Sets the gradual correction points
CSC_R (G, B) GP1 to 8*: Sets the gradual correction points
CSC_R (G, B) GD1 to 8*: Sets the expansion of the correction data
CSC_XH_ON: 1 = Cross hatch insertion ON, 0 = OFF
CSC_XH_DAT: Sets the cross hatch display level
*: Set independently for R, G and B, Others: Settings shared by R, G and B

The color shading correction data of the desired gradual level up to 8 screens (max.) can be set in RAM. The RAM size is 8 bits × 1792 words, so up to 1792 correction points can be set. The correction data is set as 8-bit data with code. Correction data can be set in the range of –128 to +127 graduation. The example shown on page 47 is for a 1024-dot × 768-line XGA video signal divided into 9 points at 128-dot intervals in the horizontal direction and 7 points at 128-line intervals in the vertical direction. The relationship between the correction point coordinates (m, n) and the RAM address is obtained as follows.

RAM address = (m – 1) + (n – 1) × (Number of horizontal correction points)

For the example on page 47, this is as follows.

(9 – 1) + (7 – 1) × 9 = 62

Thus, the correction data must be set in the RAM from address 0 to address 62.

If correction is to be performed in the gradual direction as well, the RAM address is found based on the relationship between the coordinates (m, n) of the correction points and the number of gradual correction points using the formula below:

RAM address = (m – 1) + (n – 1) × (number of horizontal correction points)
+ (number of horizontal correction points) × (number of vertical correction points)
× (number of gradual correction points – 1)

If the number of gradual correction points is eight, it is necessary to set correction data into RAM from Address 0 to Address 503 as calculated below:

(9 – 1) + (7 – 1) × 9 + 9 × 7 × 7 = 503

Correction data in the gradual direction for the screen 2 and subsequent planes is set in order from Address 63. This IC supports top/bottom and/or right/left inversion of the LCD panel by controlling the direction in which correction data that has been set into RAM is read. Up/down and/or right/left inversion are set from DWN and RGT of the TG block.
CSC_DWN and CSC_R (G, B)_RGT control the link with the TG block settings. It is therefore unnecessary to reset correction data. The table below gives an example of setting correction points.

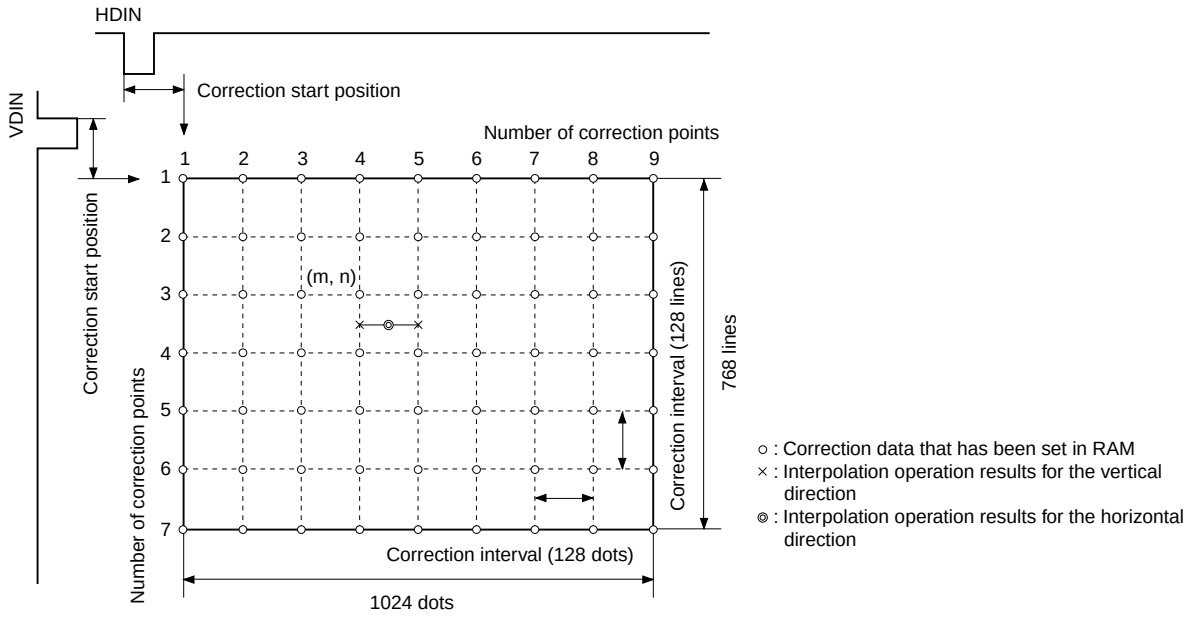
Signal specification	Correction gap		Number of correction points			
	H	V	H	V	G	Total
XGA (1024 × 768)	64	64	17	13	8	1768
	64	64	16	12	8	1536
SVGA (800 × 600)	50	50	17	13	8	1768
	64	64	14	11	8	1232
	64	64	13	10	8	1040

Example of Setting Correction Points

This IC has two ways it can handle interpolation in the horizontal and vertical directions: by dividing the screen into a uniform grid and setting data for points at the intersections or by setting data for points in the center of each area.

(1) When setting data for intersection points (pixels) on the screen

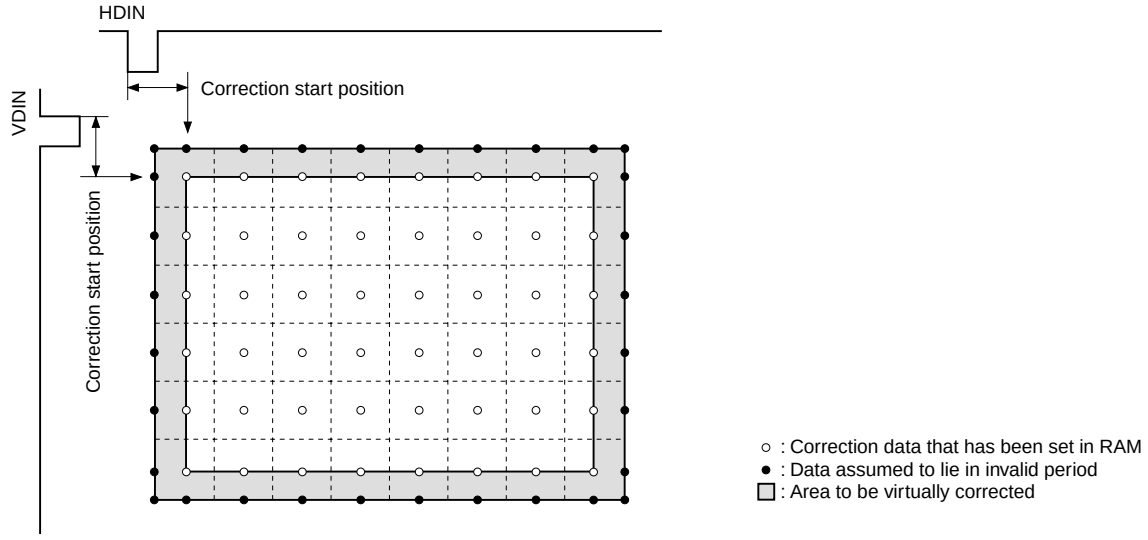
The correction area is set for the entire screen. An interpolation operation uses 4 values nearby intermediate points to perform calculations. The correction start position is set using CSC_HP and CSC_VP. Be sure to set the start position for the effective period of the video signal.



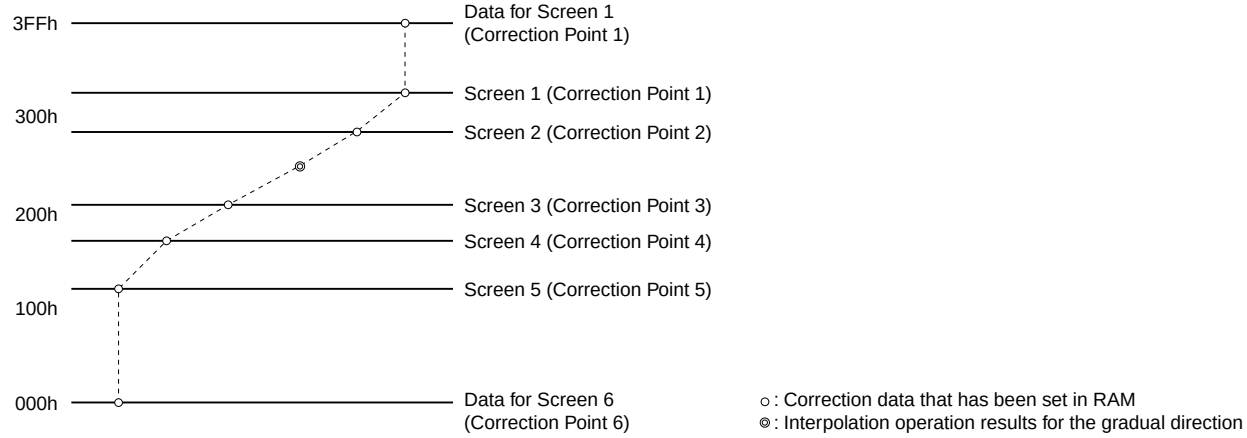
(2) When setting the correction point to the center of the areas dividing the screen

The correction area is set to inside the screen. At this time, be sure to set the correction start position so it lies inside the screen. When the correction point is set to the center of the areas dividing the screen, it is necessary to virtually perform correction outside the correction area for which correction data is set. It is therefore assumed that the same data as at the edge of the correction area applies to outside the interpolation area, and linear interpolation is performed.

Use CSC_HOS and CSC_VOS to set correction areas that are to be expanded.

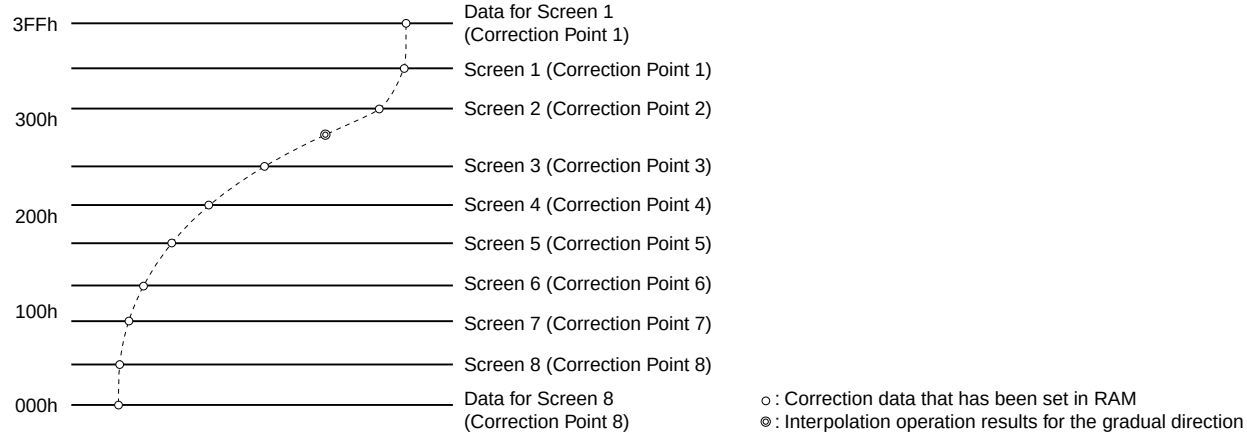


The number of correction points to be used by this IC for correction in the gradual direction can be set using CSC_GNUM. The number of correction points can be varied from 1 to 8 and settings are available for each RGB signal. This means that the gradual level for which correction is to be performed can be independently and freely set for each RGB signal using CSC_R (G, B) GP1 to 8. An interpolation operation uses 2 values nearby intermediate points to perform linear interpolation.
If the number of correction points is 1, no interpolation operation is performed in the gradual direction. The results of interpolation for one screen are added to the video signal regardless of the gradual level of the video signal being input. Correction data for one screen is entered into RAM beginning from Address 0.
When two or more correction points are used, interpolation in the gradual direction is performed according to the gradual level of the video signal being input. If the number of correction points is 2 through 7, be sure to set data into RAM for the number of screens equal to "the number of correction points plus 1", beginning from Address 0.
In the example shown in the figure below, correction data is assigned when there are 5 correction points. In addition to the 5 correction points, data for Screen 1 (Correction Point 1) is assigned to 3FFh. Data for the Screen 6 (Correction Point 6) is assigned to 000h. In the case of the Screen 6, be sure to either set correction data for gradual level 000h or the same correction data as for Screen 5. In this time the value set by using CSC_R (G, B) GP6 is ignored.



Example of Settings for Five Correction Points

When there are 8 correction points, be sure to set the data for the 8 screens into RAM beginning from Address 0. In addition to the 8 correction points, data for Screen 1 (Correction Point 1) is assigned to 3FFh as shown in the figure below. Data for Screen 8 (Correction Point 8) is assigned to 000h.



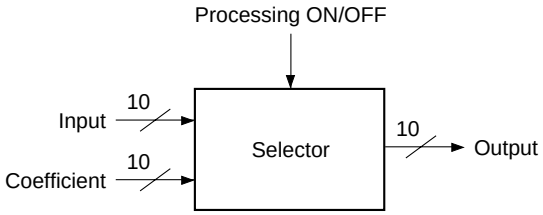
Example of Settings for Eight Correction Points

Furthermore, with this IC, correction data can be extended from 8 bits with code to 9 bits with code. This setting is made using CSC_R (G, B) GD1 to 8. This setting can be made separately for each correction point in the gradual direction as well as independently for each RGB signal.

(m) Mute 2

This block performs mute processing by replacing the video signal with data of the desired level. The settings are as follows.

MUTE2_ON: 1 = Mute processing ON, 0 = OFF (Setting shared by R, G and B)
R, G, B_MUTE2: RGB mute data (Set independently for R, G and B)

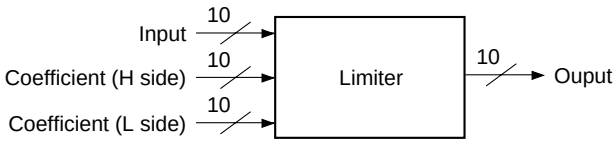


(n) Limiter

This block performs limiter processing so that the output signal does not exceed a certain range. The settings are as follows.

L_LIM_DAT: Low side limiter level
When input data ≤ L_LIM_DAT, the output is clipped to L_LIM_DAT.
H_LIM_DAT: High side limiter level
When H_LIM_DAT ≤ input data, the output is clipped to H_LIM_DAT.
(Both settings shared by R, G and B)

Set data so that the relationship L_LIM_DAT < H_LIM_DAT is constantly maintained. When both coefficient values are 000h, limiter processing is not performed.

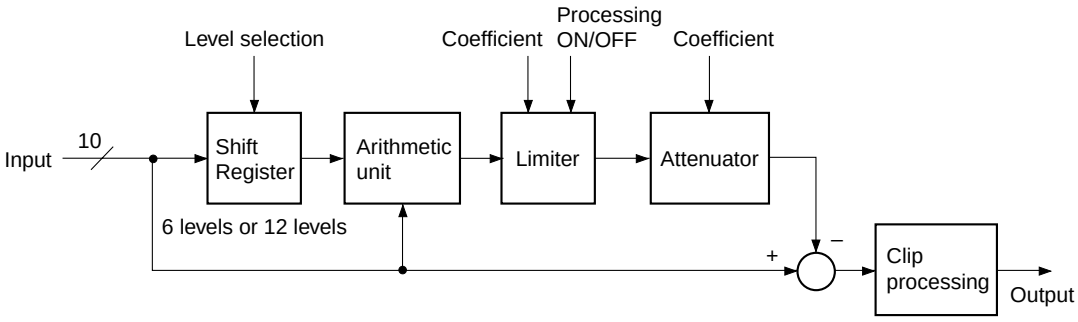


(o) Ghost cancel

This block uses signal processing to correct ghosting generated internally within the LCD panel. Correction is performed by attenuating the video signal and adding after 6 or 12 dots. Equipped with a limiter, the following settings result in processing only for a video signal of a set level or higher.

GC_ON: 1 = Ghost cancel processing ON; 0 = OFF (Settings shared by R, G and B)
GC_MODE: 1 = 12-dot period processing ON; 0 = 6-dot period processing (Settings shared by R, G and B)
R (G, B)_GC_ATT: 8-bit gain data (Set independently for R, G and B)

The difference between the video signal prior to 6 or 12 dots and the video signal of dots for which processing is to be performed is found. Attenuation is performed based on this difference and added to the video signal to correct ghosting. In addition, settings can be made so that a limiter is used to ensure processing is performed only when the difference in the video signals is of a set level or higher.

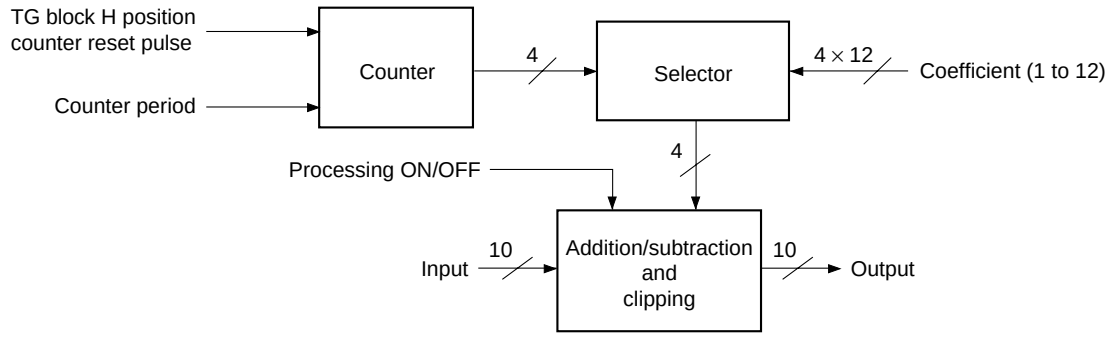


(p) Cycle offset

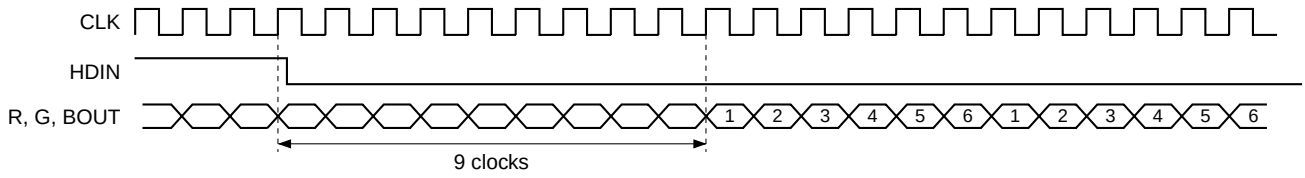
This block performs addition and subtraction processing for port. Arithmetic coefficients are selected sequentially using the counter output value as the select signal. Therefore, a cyclic offset relative to the video signal can be attached. The settings are as follows.

OFFSET_ON: 1 = Offset processing ON, 0 = OFF (Setting shared by R, G and B)
OFFSET_MODE: 0 = 6-dot period, 1 = 12-dot period (Setting shared by R, G and B)
R (G, B)_OFFSET1 to 12: 4-bit offset data with code
–8 to +7 graduation, variable with an accuracy of 1 bit
(Set independently for R, G and B)

The counter operation selects offset data sequentially from R (G, B)_OFFSET1. The offset data MSB is the code bit. Addition is performed when MSB = 0, and subtraction when MSB = 1. However, when performing subtraction, set the two's complement in the lower bits of the coefficient. When the operation results overflow or underflow, clipping is performed.



The counter reset pulse is a reset pulse of TG block H position counter, and that is linked with the HP setting values set by TG block register. The counter reset timing is delayed by 9 clocks from the front edge of the HDIN input when HP[10:0] = 000h.



HP[10:0] = 000h, 6-dot Period Processed Timing

6. Register Interface

With this IC, each register and RAM data are set by the host I/F. Addresses for each data are mapped onto a 64K-byte memory space and can be accessed individually. Note that since this is an interface with an external ROM that mapping of the data area is scattered.

Start address	Block name
0000h	Serial bus control register
1000h	TG block
2000h	DSD block
3000h	Color shading correction block
4000h	Pattern generator
8000h	RAM for gamma correction block (Red)
9000h	RAM for gamma correction block (Green)
A000h	RAM for gamma correction block (Blue)
C000h	RAM for color shading correction block (Red)
D000h	RAM for color shading correction block (Green)
E000h	RAM for color shading correction block (Blue)

Serial Bus Control Registers

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
0000h	TEST1	—	ROM_MAP[1:0]		ROM_RMOD	TEST2	RSCL_SEL[1:0]		00h
0001h	RSLV_ADDR[7:4]				—	—	—	—	00h
0002h	GAM_ADDR[15:10]						—	—	00h
0003h	CSC_ADDR[15:10]						—	—	00h
0004h	—	CSC_ADDR[18:16]			—	GAM_ADDR[18:16]			00h
0005h	CSC_SIZE[7:0]								00h
0006h	—	—	—	—	—	CSC_SIZE[10:8]			00h
0007h	ROM_TRAN[7:0]								00h
0008h	—	—	—	—	—	ROM_TRAN[10:8]			00h
0009h	—	—	—	—	—	ROM_RST	REF_MODE[1:0]		00h
000Ah	—	—	—	—	—	REF_RSEL[2:0]			00h
000Bh	—	—	—	—	—	—	—	FORCE_VD	00h
000Ch	—	—	—	—	—	RAM_FAIL	ROM_FAIL	REF_END	00h

—: Don't care

The detailed setting contents are described below.

(a) ROM_MAP[1:0] (sub address: 0000h)

This sets the size of the external EEPROM. The values are as follows.

00: 512K bits (65,536 × 8 bits)
01: 256K bits (32,768 × 8 bits)
10: 128K bits (16,384 × 8 bits)
11: 64K bits (8,192 × 8 bits)

(b) ROM_RMOD (sub address: 0000h)

This sets the read access mode of the external EEPROM. Setting values are as follows.

0: Normal mode (Default)
A memory address is always output when read access is performed on external EEPROM.
1: High speed mode
Memory access is performed using the address held by external EEPROM in the case of continuous read when read access is performed on external EEPROM.

(c) RSCL_SEL[1:0] (sub address: 0000h)

The clock output on RSCL is set according to the master clock being used. Setting values are as follows.

00: 35MHz or less
01: 70MHz or less
10: 94.5MHz or less
11: 100MHz or less

(d) TEST1 and TEST2 (sub address: 0000h)

These set the test mode. This is fixed to "0".

(e) RSLV_ADDR[7:4] (sub address: 0001h)

This sets the slave address of the external EEPROM. Although addresses of reserved areas can be set, be sure to set appropriate addresses. The lower portion of the slave addresses is determined by memory mapping.

(f) GAM_ADDR[18:10] (sub addresses: 0002h and 0004h)

This sets the start address ([18:10]) used when storing gamma correction data on the external EEPROM. The lower address ([9:0]) is fixed to "0" and settings can be made in 1K-byte units.

(g) CSC_ADDR[18:10] (sub addresses: 0003h and 0004h)

This sets the start address ([18:10]) used when storing color shading correction data on the external EEPROM. The lower address ([9:0]) is fixed to "0" and settings can be made in 1K-byte units.

(h) CSC_SIZE[10:0] (sub addresses: 0005h and 0006h)

This sets "the size of color shading correction data – 1" in 11 bits.

(i) ROM_TRAN[10:0] (sub addresses: 0007h and 0008h)

The lower 11 bits are used to set "the number of bytes – 1" to be transferred per access for the external EEPROM during refresh and write-back operations.

(j) ROM_RST (sub address: 0009h)

This causes forced reset of the external ROM I/F circuit. A reset is executed when "1" is written to this bit. "0" is read during read operations.

(k) REF_MODE[1:0] (sub address: 0009h)

This sets the operation settings for the refresh circuit. Setting values are as follows.

00: Refresh stop mode
During refresh stop mode, internal RAM can be accessed by the host.

01: Self-refresh mode
During self-refresh mode, internal RAM cannot be accessed by the host. Refresh starts when vertical blanking starts.

10: Forced refresh mode
Used to transfer external EEPROM data to internal RAM at times such as during Power ON. The external EEPROM address for data to be transferred is determined based on each start address register. Whether the data being transferred is gamma data or color shading data is determined by REF_RSEL[2].
Refresh starts when this mode is set.

11: Write-back mode
Internal RAM data is transferred to external EEPROM in order to write data to external EEPROM at times such as during manufacture. The external EEPROM address of data to be transferred is determined by each start address register. Whether the data being transferred is gamma data or color shading data is determined by REF_RSEL[2].
Write-back starts when this mode is set.

Each of these modes can be executed by writing these bits.

(l) REF_RSEL[2:0] (sub address: 000Ah)

Sets whether to access the gamma RAM area or color shading RAM area during write-back and refresh modes. In addition, the area to be accessed automatically changes to the next access area when all transfers for a given area have been completed.
The order in which area are accessed is: Gamma (Red) → Gamma (Green) → Gamma (Blue) → Color shading (Red) → Color shading (Green) → Color shading (Blue) → Gamma (Red).
It is possible to read this bit during operations to find out which RAM is currently being accessed. The settings are as follows.

000: Accesses the Gamma RAM (Red) area.
001: Accesses the Gamma RAM (Green) area.
010: Accesses the Gamma RAM (Blue) area.
011: Reserved
100: Accesses the Color shading RAM (Red) area.
101: Accesses the Color shading RAM (Green) area.
110: Accesses the Color shading RAM (Blue) area.
111: Reserved

(m) FORCE_VD (sub address: 000Bh)

Forcibly generates a VD pulse for writing to double registers. VD is generated when "1" is written to this bit. "0" is read during read operations.

(n) RAM_FAIL (sub address: 000Ch)

Indicates whether or not accessing internal RAM succeeded. Cleared when "1" is written to this bit.
Status: 0 = Succeeded in accessing internal RAM; 1 = Failed in accessing internal RAM

(o) ROM_FAIL (sub address: 000Ch)

Indicates whether or not accessing external EEPROM succeeded. Cleared when "1" is written to this bit.
Status: 0 = Succeeded in accessing external EEPROM; 1 = Failed in accessing external EEPROM

If the external EEPROM is being written during write-back, ACK is not returned by Ack Polling. This means that "1" is set for this bit during Ack Polling. However, this bit is automatically cleared when the write operation is complete and ACK is returned by Ack Polling.

(p) REF_END (sub address: 000Ch)

Indicates that forced refresh or write-back operations are complete. Cleared when "1" is written to this bit.
Status: 1 = Access of external EEPROM is complete

TG Block Register

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
1000h	—	POLDET	HPOL	VPOL	HR	RGT	DWN	FRVCLNK	30h
1001h	FRPM[1:0]		HSTPOL	HCKPOL	VSTPOL	VCKPOL	DCKPOL	PSTPOL	FFh
1002h	HSTM	PSTM	HSTFIX	HCKFIX	VSTFIX	VCKFIX	DCKFIX	DCKFINV	FFh
1003h	VFRRN[10:3]								FFh
1004h	—	—	—	—	—	PLLP[10:8]			00h
1005h	PLLP[7:0]								00h
1006h	—	—	—	—	—	HP[10:8]			00h
1007h	HP[7:0]								00h
1008h	VP[7:0]								00h
1009h	PRGU[9:8]		PRGD[9:8]		SHSTU[9:8]		SHSTD[9:8]		00h
100Ah	PRGU[7:0]								00h
100Bh	PRGD[7:0]								00h
100Ch	SHSTU[7:0]								00h
100Dh	SHSTD[7:0]								00h
100Eh	FRPP[9:8]		HD1U[10:8]			HD1D[10:8]			00h
100Fh	FRPP[7:0]								00h
1010h	HD1U[7:0]								00h
1011h	HD1D[7:0]								00h
1012h	—	—	CLPU[10:8]			CLPD[10:8]			00h
1013h	CLPU[7:0]								00h
1014h	CLPD[7:0]								00h
1015h	—	—	SHP[5:0]						00h
1016h	—	—	HSTPC[5:0]						00h
1017h	—	—	HSTPF[5:0]						00h
1018h	—	—	PSTPC[5:0]						00h
1019h	—	—	PSTPF[5:0]						00h
101Ah	—	—	HCKC[5:0]						00h
101Bh	DCKF[3:0]				DCKW[3:0]				00h
101Ch	PCGU[9:8]		PCGD[9:8]		ENBU[9:8]		ENBD[9:8]		00h
101Dh	PCGU[7:0]								00h
101Eh	PCGD[7:0]								00h
101Fh	ENBU[7:0]								00h
1020h	ENBD[7:0]								00h
1021h	CLRU[9:8]		CLRD[9:8]		VCKP[9:8]		VSTP[10:9]		00h
1022h	CLRU[7:0]								00h
1023h	CLRD[7:0]								00h

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
1024h	VCKP[7:0]								00h
1025h	VSTP[8:1]								00h
1026h	—	—	HD2U[10:8]			HD2D[10:8]			00h
1027h	HD2U[7:0]								00h
1028h	HD2D[7:0]								00h
1029h	PO2	PO1	HD3U[10:8]			HD3D[10:8]			00h
102Ah	HD3U[7:0]								00h
102Bh	HD3D[7:0]								00h
102Ch	CLKOUT	HD1OE	CLPOE	PRGOE	SHSTOE	FRPOE	XFRPOE	HD2OE	00h
102Dh	HSTOE	PSTOE	HCKOE	DCKOE	VOE	PCGOE	HD3OE	CLROE	00h

—: Don't care

The detailed setting contents are described below.

(a) Clock settings

(1) CLKOUT (sub address: 102Ch)

This sets the Pin 28 clock output.

Setting value: 1 = Internal clock is inverted and output, 0 = Low is output

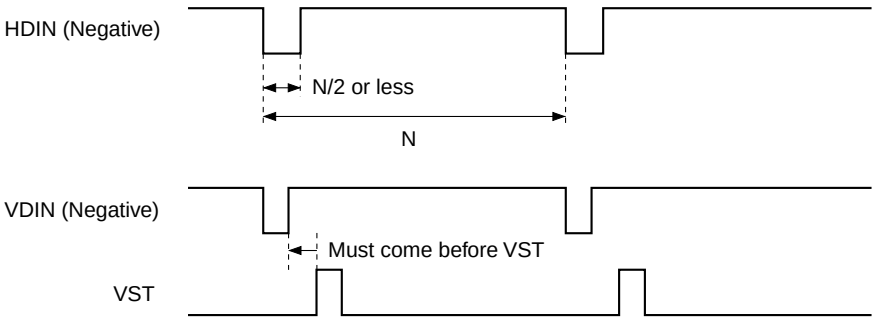
(b) SYNC polarity settings

(1) POLDET (sub address: 1000h)

This sets the sync polarity auto discrimination function ON/OFF.

Setting value: 1 = Auto discrimination function ON, 0 = Auto discrimination function OFF

When POLDET = 1, the HPOL and VPOL settings below are invalid. When using this function, the HDIN sync portion must be 1/2 or less of 1H, and the VDIN sync portion must come before the rise position of the VST pulse.



(2) HPOL and VPOL (sub address: 1000h)

These set the sync signal polarity when POLDET = 0.

Setting value: 1 = Positive polarity, 0 = Negative polarity

The internal operation of this IC is with the input sync signal fixed to positive polarity. Therefore, these HPOL and VPOL must be set in accordance with the polarity of the sync signal input from HDIN and VDIN.
Set HPOL and VPOL to "1" when the input sync signal is positive polarity, or to "0" when negative polarity.

(c) Dots per 1H and lines per 1V settings

(1) HR (sub address: 1000h)

This sets the PLL counter reset ON/OFF.
Setting value: 1 = Reset enabled, 0 = Reset disabled

When HR = 0, the internal frequency divider is used, and the HD1 pulse output should be used as the return pulse. The number of dot clocks per 1H is set by PLLP[11:1] below.

(2) PLLP[10:0] (sub addresses: 1004h and 1005h)

This sets the internal PLL counter reset period in 11 bits. Setting is possible in 1-dot units.
When HR = 0, free-running occurs at the above N. When HR = 1, if the next HDIN is not input before the internal PLL counter counts up to 2047, free-running mode is established and free-running occurs at N.
When HDIN is input, free-running is canceled and normal operation is established.

(3) VFRRN[10:3] (sub address: 1003h)

This sets the number of lines in 9 bits during vertical free running. Setting is possible in 4-line units. To have operation run freely at M lines, set the "(M – 4)/4" value. If the next VDIN is not input before the internal vertical line counter counts up to 2047, free-running mode is established. When VDIN is input, free-running is canceled and normal operation is established.

(d) Scan direction settings

RGT and DWN (sub address: 1000h)

These settings switch the scan directions of the LCD panel.
Setting value: 1 = Forward scan, 0 = Reverse scan

When CTRL (Pin 88) is low, RGT (Pin 2) and DWN (Pin 49) function as output pins, and the data set in the respective registers is reflected. When CTRL is high, this setting is ignored, RGT and DWN function as input pins, and are reflected to internal operation.

(e) PO1 and PO2 output settings

PO1 and PO2 (sub address: 1029h)

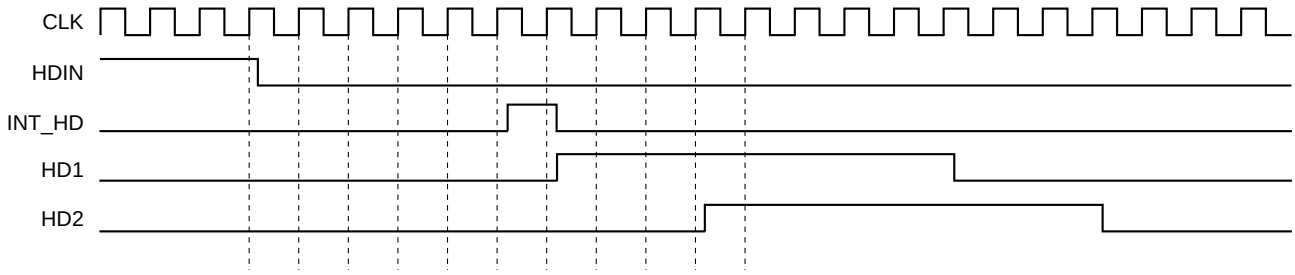
These set the PO1 and PO2 output.
Setting value: 1 = High is output, 0 = Low is output

The set data is reflected to the output pins PO1 (Pin 47) and PO2 (Pin 48) of the same name.

(f) Horizontal display position and horizontal direction pulse settings

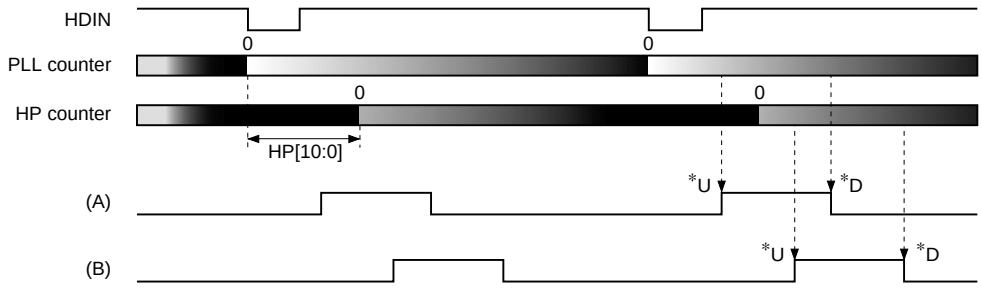
(1) HP[10:0] (sub addresses: 006h and 007h)

HP[10:0] sets the horizontal pulse position for the LCD panel in 11 bits. The position can be set in 1-dot units using the internal pulse INT_HD generated from the front edge of HDIN as the reference. The HP setting range is from "0 to (N – 1)".
If the HP value is set to the number of frequency divisions N or higher, the HP setting is ignored and "(N – 1)" is used as the setting value.
The HST, PST, HCK1, HCK2, DCK1, DCK2, ENB, VST, VCK, FRP, XFRP, PCG, BLK, HD2 and HD3 horizontal timing pulses are linked according to the HP setting.
The internal reference pulse INT_HD rises at the 5th clock from the front edge of the HDIN input, and all the pulses are synchronized using this as the reference. Increasing HP shifts the output positions of the linked pulses toward the rear of the time series. The example below shows the shortest output position from HDIN when HP is set to 000h. (Note that the output position changes according to the settings in (2) below.)



(2) CLPU[10:0], CLPD[10:0], PRGU[9:0], PRGD[9:0], HD1U[10:0], HD1D[10:0], SHSTU[9:0], SHSTD[9:0], PCGU[9:0], PCGD[9:0], ENBU[9:0], ENBD[9:0], HD2U[10:0], HD2D[10:0], HD3U[10:0] and HD3D[10:0] (sub addresses: 1009h to 100Eh, 1010h to 1014h, 01Ch to 020h and 1026h to 102Bh)

These set the horizontal timing pulse output positions in 10 bits or 11 bits. The respective rise and fall positions can be set in 1-dot units. Settings ending in "U" set the rise position, and settings ending in "D" set the fall position. Horizontal pulses are divided into the following two types.
(A) CLP and HD1 → Pulses synchronized to the PLL counter
Set the "rise position/fall position – 5" value.
(B) PRG, SHST, PCG, ENB, HD2 and HD3 → Pulses synchronized to the HP counter
Set the "rise position/fall position – HP setting value – 8" value.
An outline of each type is shown below. When **U and **D are set to the same value, "1" is output.



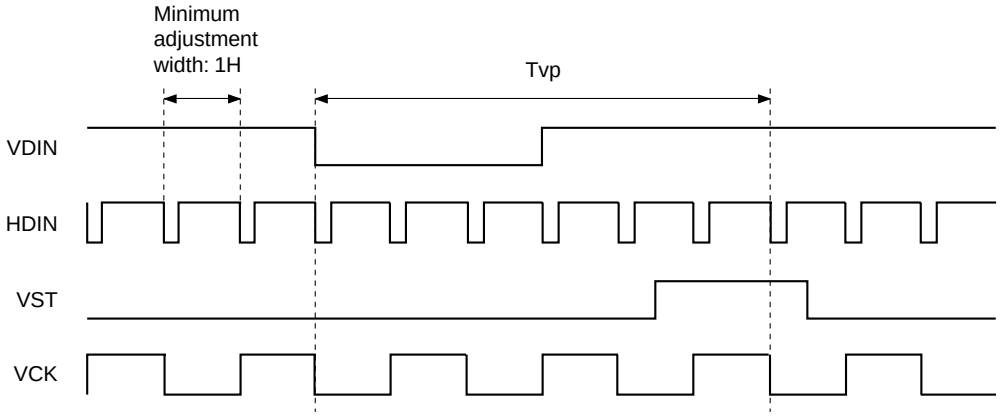
(3) HD1OE, HD2OE, HD3OE, CLPOE, PRGOE, SHSTOE, PCGOE and CLROE (sub addresses: 102Ch and 102Dh)

These set the output limit of HD1, HD2, HD3, CLP, PRG, SHST, PCG and CLR pulses, respectively.
Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(g) Vertical display position setting

VP[7:0] (sub address: 1008h)

This sets the vertical display start position in 8 bits. The position can be set in 1-line units using the front edge of VDIN as the reference. The VST, VCK, FRP and XFRP pulse phases change by linking with this setting.



Tvp minimum and maximum setting values

	Min.	Max.
VP[7:0]	000h	FFh
Tvp	6H	261H

(h) HST and PST pulse settings

(1) HSTM (sub address: 1002h)

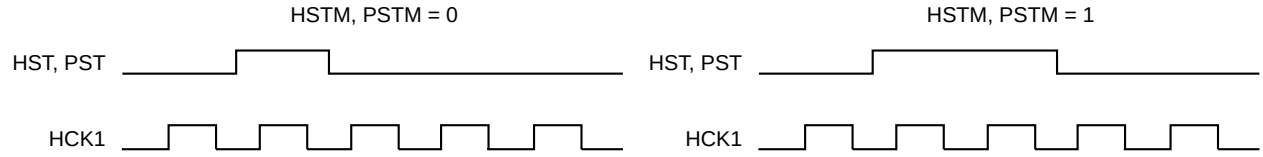
This sets the pulse width for horizontal display start timing pulse HST.
Setting value: 1 = Twice the HCK period width, 0 = HCK period width

Set the width according to the LCD panel specifications.

(2) PSTM (sub address: 1002h)

This sets the pulse width for dot sequential precharge start timing pulse PST.
Setting value: 1 = Twice the HCK period width, 0 = HCK period width

Set the width according to the LCD panel specifications.



(3) HSTFIX, HSTPOL and PSTPOL (sub addresses: 1001h and 1002h)

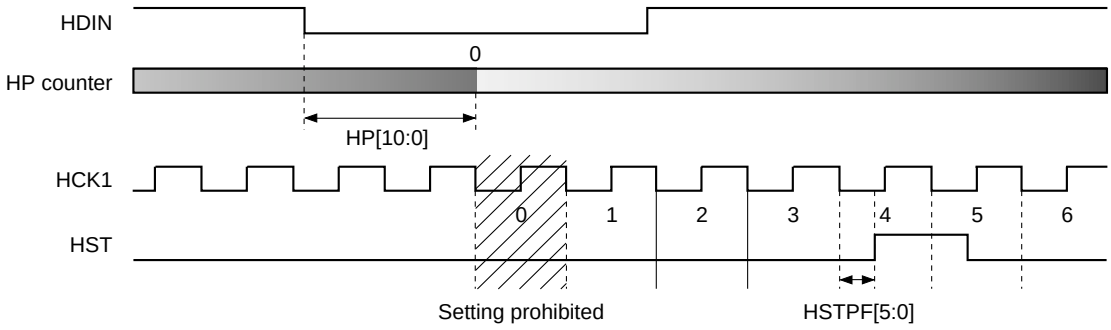
These set the HST and PST pulse output polarities. The polarity changes as follows according to the combination of linked/not linked with control signal RGT.

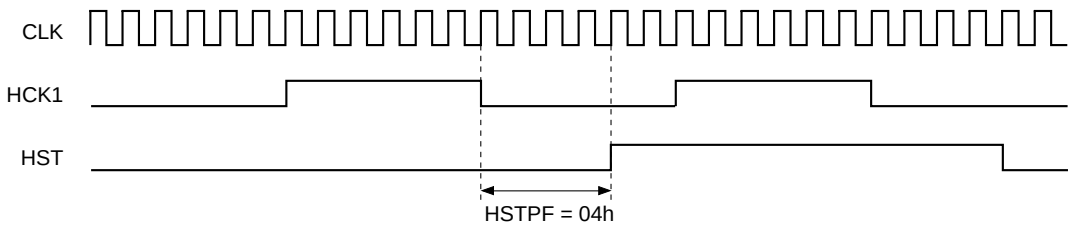
HSTFIX	HSTPOL	RGT	HST pulse output polarity
0	0	0	Positive
0	0	1	Negative
0	1	0	Negative
0	1	1	Positive
1	0	0	Negative
1	0	1	Negative
1	1	0	Positive
1	1	1	Positive

HSTFIX	PSTPOL	RGT	PST pulse output polarity
0	0	0	Positive
0	0	1	Negative
0	1	0	Negative
0	1	1	Positive
1	0	0	Negative
1	0	1	Negative
1	1	0	Positive
1	1	1	Positive

(4) HSTPC[5:0], HSTPF[5:0], PSTPC[5:0] and PSTPF[5:0] (sub addresses: 1016h to 1019h)

These set the HST and PST pulse phases. Reset is applied when the internal HP counter reaches "0", and the HST and PST pulse phases within 1H can be set at the HCK1 and HCK2 period, respectively, by HSTPC and PSTPC.
HSTPF and PSTPF can set the HST and PST pulse phase relative to HCK1 and HCK2 in 1-dot units.
Do not set HSTPC and PSTPC to 00h, as the pulses may not be output correctly in this case.
The HSTPF and PSTPF values can be set up to "(HCKC × 2 – 2)". If higher values are set, the pulses are not output. Set the "(phase difference from HCK pulse)" value.
The figures below show the timings for HSTPC: 04h and HSTPF: 04h, respectively. These timings are the same for the PST pulse.





(5) HSTOE and PSTOE (sub address: 102Dh)

These set the output limit of HST and PST pulses output limits, respectively.

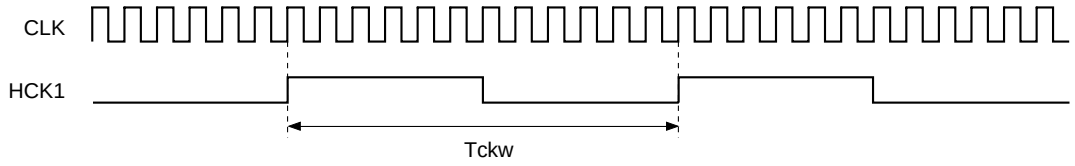
Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(i) HCK1 and HCK2 pulse settings

(1) HCKC[5:0] (sub address: 101Ah)

This sets the HCK1 and HCK2 period (LCD panel sampling period). Settings which result in an odd number for Tckw in the figure below are prohibited, so be sure to set a value that results in an even number. Set the "(Tckw – 1)" value according to the LCD panel specifications. When this setting is changed, the HST and PST pulse phases also change, so first set HCKC to the correct value and then make the HST and PST settings. Example setting values are shown in the table below.

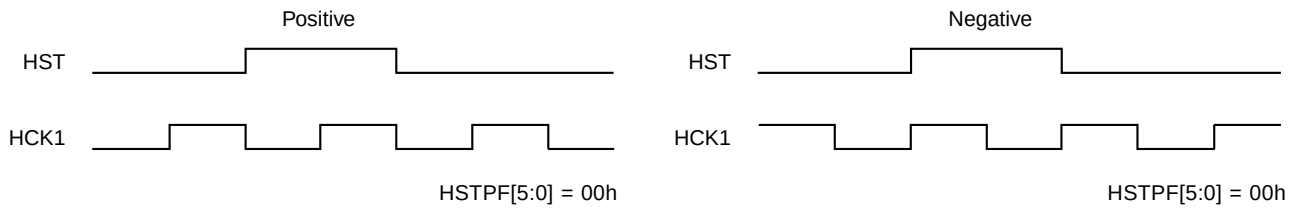
LCD panel	Tckw	HCKC
SVGA	12 clk	0Bh
XGA, WXGA	24 clk	17h



(2) HCKFIX and HCKPOL (sub addresses: 1002h and 1001h)

These set the HCK1 and HCK2 pulse output polarity. The polarity relative to the HST pulse changes as follows according to the combination of linked/not linked with control signal RGT.

HCKFIX	HCKPOL	RGT	Output polarity
0	0	0	Positive
0	0	1	Negative
0	1	0	Negative
0	1	1	Positive
1	0	0	Negative
1	0	1	Negative
1	1	0	Positive
1	1	1	Positive



(3) HCKOE (sub address: 102Dh)

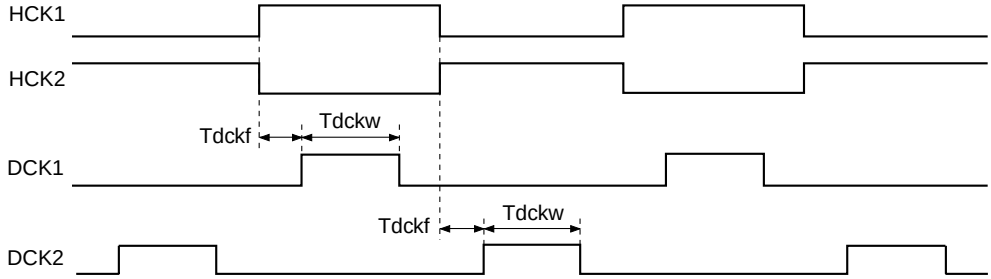
This sets the output limit of HCK1 and HCK2 pulses output limits.

Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(j) DCK1 and DCK2 pulse settings

(1) DCKF[3:0] and DCKW[3:0] (sub address: 101Bh)

These set the DCK1 and DCK2 pulse phases and widths. DCKF sets the DCK1 and DCK2 pulse phases relative to HCK in 0.5-dot units. Set the "Tdckf" value.
The DCKFINV, DCKFIX and RGT settings differ according to whether the phase is synchronized with the rising edge of HCK1 or HCK2.
The DCK1 and DCK2 pulse width can be set in 1-dot units by DCKW. Set the "Tdckw – 1" value.



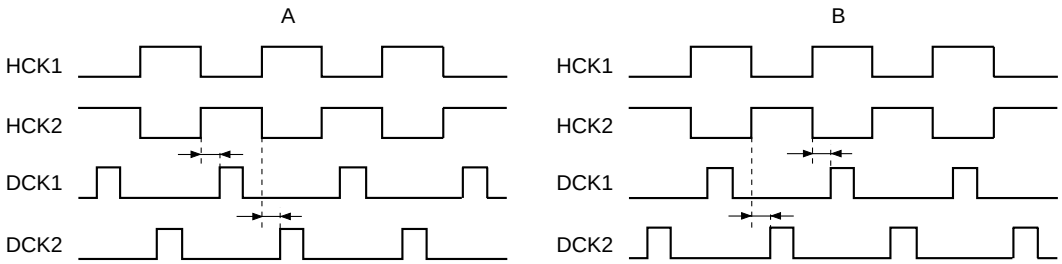
(2) DCKPOL (sub address: 1001h)

This setting switches the DCK1 and DCK2 pulse output polarities.

(3) DCKFINV and DCKFIX (sub address: 1002h)

This setting switches the DCK1 and DCK2 output phases relative to HCK1 and HCK2. The output phase is as follows by setting right/left inversion control signal RGT.

DCKFIX	DCKFINV	RGT	Output phase
0	0	0	A
0	0	1	B
0	1	0	B
0	1	1	A
1	0	0	B
1	0	1	B
1	1	0	A
1	1	1	A



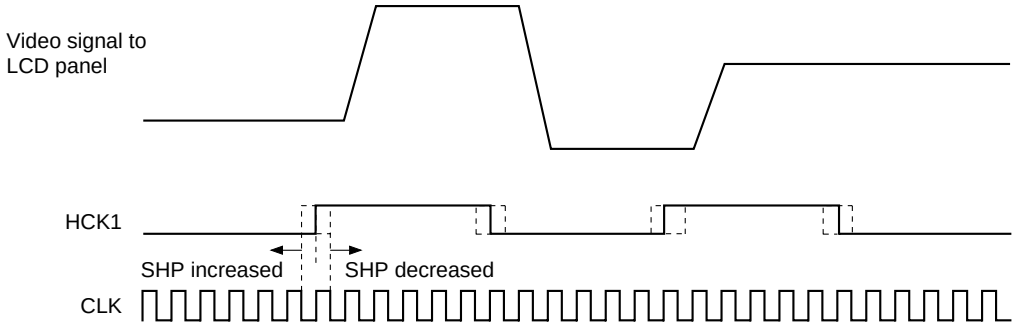
(4) DCKOE (sub address: 102Dh)

This sets the output limit of DCK1 and DCK2 pulses.
Setting value: 1 = Pulses are output, 0 = Output is fixed to "0"

(k) LCD panel sample-and-hold position setting

SHP[5:0] (sub address: 1015h)

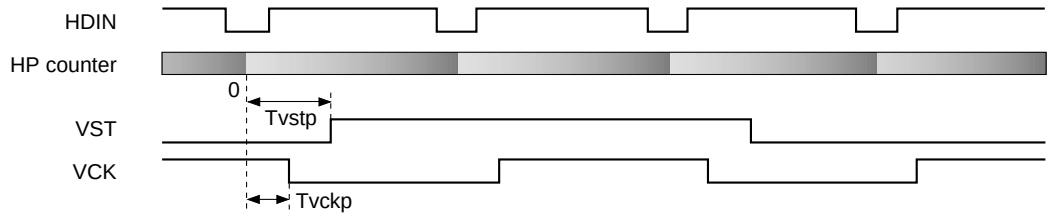
This sets the horizontal transfer start pulse and clock pulse phases relative to the video signal to the LCD panel. The phase can be set in 64 positions with 6 bits. Incrementing SHP by +1 shifts the HST, PST, HCK1, HCK2, DCK1 and DCK2 pulses forward by 0.5 dot (half the internal clock period). The LCD panel sample-and-hold position can be set by shifting the above pulse phases forward or backward relative to the video signal. At this time, the phases between the HST, PST, HCK1, HCK2, DCK1 and DCK2 pulses do not change. The figure below shows an example of HCK1 during 12-dot simultaneous sampling.
This setting eliminates the need to set the sample-and-hold position with a Sony sample-and-hold driver IC, and makes it possible to adjust the phases of the video signal to the LCD panel and the horizontal transfer clock without changing the position of the video signal on the screen.



(I) VST and VCK pulse settings

(1) VSTP[10:1] (sub addresses: 1021h and 1025h)

This sets the VST pulse rise and fall positions within 1H in 10 bits. The positions can be set in 2-dot units using the internal HP counter "0" position as the reference. Set the "(Tvstp – 2)/2" value.



(2) VCKP[9:0] (sub addresses: 1021h and 1024h)

This sets the VCK, FRP and XFRP inversion positions within 1H in 10 bits. The positions can be set in 1-dot units using the internal HP counter "0" position as the reference. Set the "Tvckp – 1" value.

(3) VSTFIX and VCKFIX (sub address: 1002h), VSTPOL and VCKPOL (sub address: 1001h)

These set the VST and VCK pulse output polarities. The VST pulse polarity and the VCK pulse polarity relative to the VST pulse change as follows according to the combination of linked/not linked with control signal DWN.

***FIX	***POL	DWN	Output polarity
0	0	0	Positive
0	0	1	Negative
0	1	0	Negative
0	1	1	Positive
1	0	0	Negative
1	0	1	Negative
1	1	0	Positive
1	1	1	Positive

***: VST or VCK

(4) VOE (sub address: 102Dh)

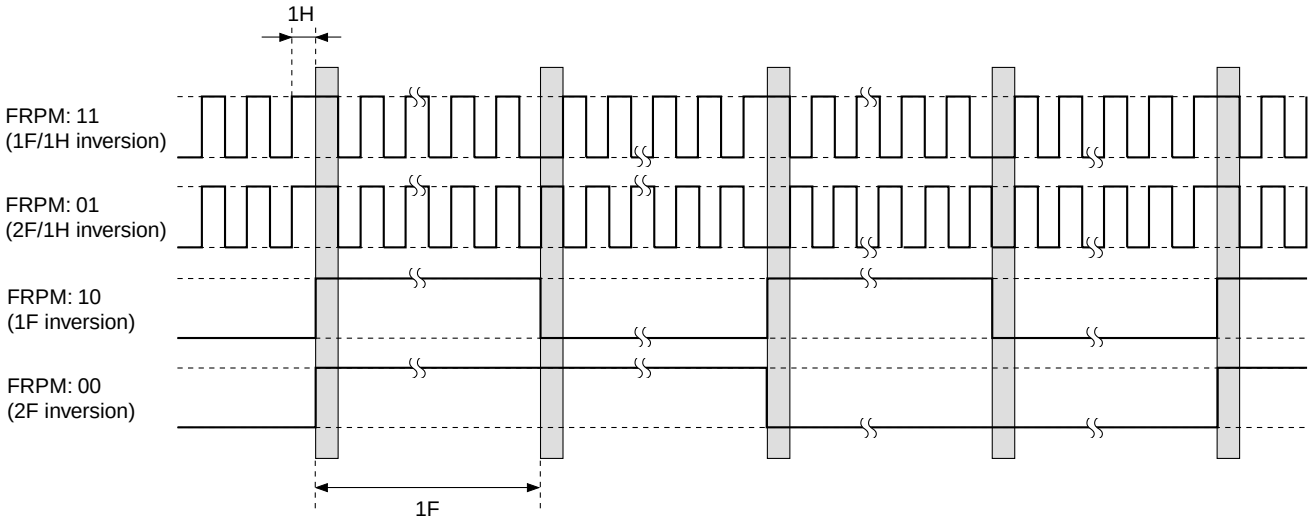
This sets the output limit of VST, VCK and ENB pulses.

Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

(m) FRP and XFRP pulse settings

(1) FRPM[1:0] (sub address: 1001h)

This sets the period for switching the LCD AC conversion signal FRP pulse. 1F/1H, 2F/1H, 1F and 2F inversion can be set as shown in the figure below. Normally use FRPM: 11.



(2) FRPP[9:0] (sub addresses: 100Eh and 100Fh)

This sets the FRP and XFRP inversion positions within 1H in 10 bits. The positions can be set in 1-dot units using the internal HP counter "0" position as the reference. Set the "FRP inversion position – HP counter "0" position – 1" value.
XFRP is output as the polarity inverted FRP pulse.

(3) FRPOE and XFRPOE (sub address: 102Ch)

These set the output limit of FRP and XFRP pulses, respectively.
Setting value: 1 = Pulse is output, 0 = Output is fixed to "0"

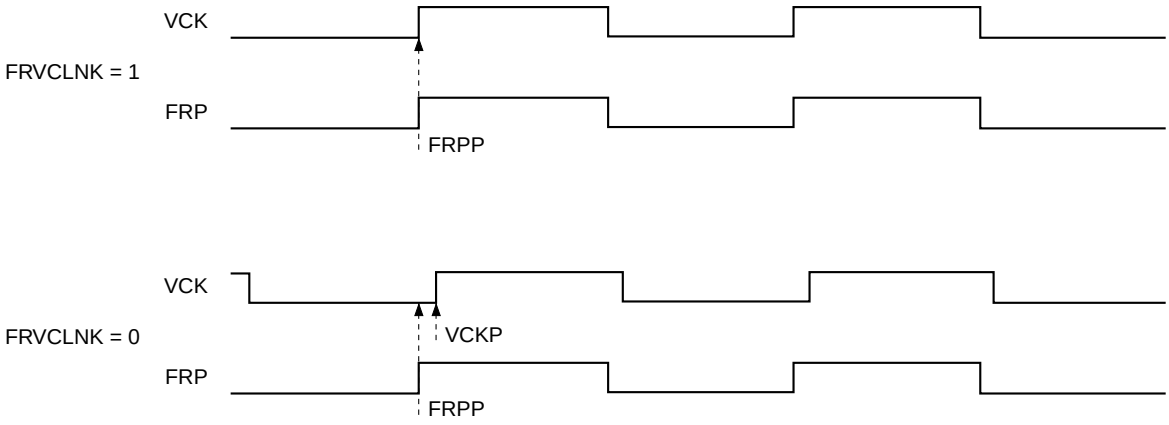
(n) VCK and FRP transition point shared setting and V block pulse right/left inversion link setting

FRVCLNK (sub address: 1000h)

This sets the VCK pulse transition point.

Setting value: 1 = FRP and VCK transition points are shared,
0 = FRP and VCK transition points are independent

When FRVCLNK = 1, the VCK inversion timing is forcibly synchronized with the FRP inversion timing.
When FRVCLNK = 0, the VCK transition point is independent of FRP.



DSD Register

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
2000h	—	OFFSET_ON	GC_ON	LIM_ON	MUTE2_ON	GAM_ON	MUTE1_ON	FRM_ON	00h
2001h	—	—	—	—	—	OFFSET_MODE	GC_MODE	GAM_MODE	00h
2002h	USR_GAIN[7:0]								00h
2003h	USR_BRT[7:0]								00h
2004h	R_SUB_GAIN[7:0]								00h
2005h	G_SUB_GAIN[7:0]								00h
2006h	B_SUB_GAIN[7:0]								00h
2007h	R_SUB_BRT[7:0]								00h
2008h	G_SUB_BRT[7:0]								00h
2009h	B_SUB_BRT[7:0]								00h
200Ah	—	R_SUB_BRT[10:8]			—	USR_BRT[10:8]			00h
200Bh	—	B_SUB_BRT[10:8]			—	G_SUB_BRT[10:8]			00h
200Ch	FRM_H1[7:0]								00h
200Dh	FRM_H2[7:0]								00h
200Eh	—	FRM_H2[10:8]			—	FRM_H1[10:8]			00h
200Fh	FRM_V1[7:0]								00h
2010h	FRM_V2[7:0]								00h
2011h	—	FRM_V2[10:8]			—	FRM_V1[10:8]			00h
2012h	FRM_DAT[7:0]								00h
2013h	R_MUTE1[7:0]								00h
2014h	G_MUTE1[7:0]								00h
2015h	B_MUTE1[7:0]								00h
2016h	FRM_DAT[9:8]		B_MUTE1[9:8]		G_MUTE1[9:8]		R_MUTE1[9:8]		00h
2017h	R_OSD_DAT1[7:0]								00h
2018h	R_OSD_DAT2[7:0]								00h
2019h	R_OSD_DAT3[7:0]								00h
201Ah	R_OSD_DAT4[7:0]								00h
201Bh	R_OSD_DAT4[9:8]		R_OSD_DAT3[9:8]		R_OSD_DAT2[9:8]		R_OSD_DAT1[9:8]		00h
201Ch	G_OSD_DAT1[7:0]								00h
201Dh	G_OSD_DAT2[7:0]								00h
201Eh	G_OSD_DAT3[7:0]								00h
201Fh	G_OSD_DAT4[7:0]								00h
2020h	G_OSD_DAT4[9:8]		G_OSD_DAT3[9:8]		G_OSD_DAT2[9:8]		G_OSD_DAT1[9:8]		00h
2021h	B_OSD_DAT1[7:0]								00h
2022h	B_OSD_DAT2[7:0]								00h
2023h	B_OSD_DAT3[7:0]								00h

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
2024h	B_OSD_DAT4[7:0]								00h
2025h	B_OSD_DAT4[9:8]		B_OSD_DAT3[9:8]		B_OSD_DAT2[9:8]		B_OSD_DAT1[9:8]		00h
2026h	GAM_H1[7:0]								00h
2027h	GAM_H2[7:0]								00h
2028h	—	GAM_H2[10:8]			—	GAM_H1[10:8]			00h
2029h	GAM_V1[7:0]								00h
202Ah	GAM_V2[7:0]								00h
202Bh	—	GAM_V2[10:8]			—	GAM_V1[10:8]			00h
202Ch	R_GAM_GAIN[7:0]								00h
202Dh	G_GAM_GAIN[7:0]								00h
202Eh	B_GAM_GAIN[7:0]								00h
202Fh	R_GAM_BRT[7:0]								00h
2030h	G_GAM_BRT[7:0]								00h
2031h	B_GAM_BRT[7:0]								00h
2032h	—	G_GAM_BRT[10:8]			—	R_GAM_BRT[10:8]			00h
2033h	—	—	—	—	—	B_GAM_BRT[10:8]			00h
2034h	R_MUTE2[7:0]								00h
2035h	G_MUTE2[7:0]								00h
2036h	B_MUTE2[7:0]								00h
2037h	L_LIM_DAT[9:8]		B_MUTE2[9:8]		G_MUTE2[9:8]		R_MUTE2[9:8]		00h
2038h	L_LIM_DAT[7:0]								00h
2039h	H_LIM_DAT[7:0]								00h
203Ah	H_LIM_DAT[9:8]		B_GC_LIM_DAT[9:8]		G_GC_LIM_DAT[9:8]		R_GC_LIM_DAT[9:8]		00h
203Bh	R_GC_LIM_DAT[7:0]								00h
203Ch	G_GC_LIM_DAT[7:0]								00h
203Dh	B_GC_LIM_DAT[7:0]								00h
203Eh	R_GC_ATT[7:0]								00h
203Fh	G_GC_ATT[7:0]								00h
2040h	B_GC_ATT[7:0]								00h
2041h	R_OFFSET2[3:0]				R_OFFSET1[3:0]				00h
2042h	R_OFFSET4[3:0]				R_OFFSET3[3:0]				00h
2043h	R_OFFSET6[3:0]				R_OFFSET5[3:0]				00h
2044h	R_OFFSET8[3:0]				R_OFFSET7[3:0]				00h
2045h	R_OFFSET10[3:0]				R_OFFSET9[3:0]				00h
2046h	R_OFFSET12[3:0]				R_OFFSET11[3:0]				00h
2047h	G_OFFSET2[3:0]				G_OFFSET1[3:0]				00h
2048h	G_OFFSET4[3:0]				G_OFFSET3[3:0]				00h

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
2049h	G_OFFSET6[3:0]				G_OFFSET5[3:0]				00h
204Ah	G_OFFSET8[3:0]				G_OFFSET7[3:0]				00h
204Bh	G_OFFSET10[3:0]				G_OFFSET9[3:0]				00h
204Ch	G_OFFSET12[3:0]				G_OFFSET11[3:0]				00h
204Dh	B_OFFSET2[3:0]				B_OFFSET1[3:0]				00h
204Eh	B_OFFSET4[3:0]				B_OFFSET3[3:0]				00h
204Fh	B_OFFSET6[3:0]				B_OFFSET5[3:0]				00h
2050h	B_OFFSET8[3:0]				B_OFFSET7[3:0]				00h
2051h	B_OFFSET10[3:0]				B_OFFSET9[3:0]				00h
2052h	B_OFFSET12[3:0]				B_OFFSET11[3:0]				00h

—: Don't care

The detailed setting contents of DSD are described below.

(a) USR_GAIN[7:0] (sub address: 2002h)

This sets the user adjustment gain block arithmetic coefficients in 8 bits.

(b) USR_BRT[10:0] (sub addresses: 2003h and 200Ah)

This sets the user adjustment bright block arithmetic coefficients in 11 bits with code.

(c) R_SUB_GAIN[7:0], G_SUB_GAIN[7:0] and B_SUB_GAIN[7:0] (sub addresses: 2004h to 2006h)

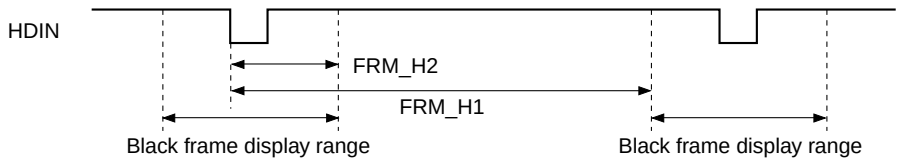
These set the sub gain block arithmetic coefficients for the R, G and B white balance adjustment in 8 bits.

(d) R_SUB_BRT[10:0], G_SUB_BRT[10:0] and B_SUB_BRT[10:0] (sub addresses: 2007h to 200Bh)

These set the sub bright block arithmetic coefficients for the R, G and B white balance adjustment in 11 bits with code.

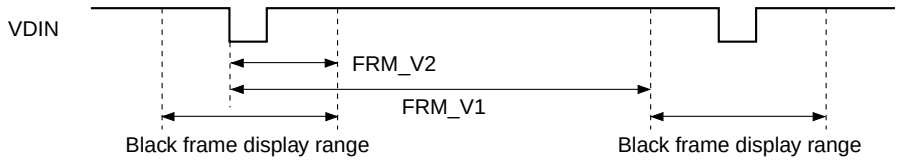
(e) FRM_H1[10:0] and FRM_H2[10:0] (sub addresses: 200Ch to 200Eh)

These set the horizontal black frame display range for the black frame block in 11 bits. The range can be set in 1-dot units. Set the "display range – 2" value.



(f) FRM_V1[10:0] and FRM_V2[10:0] (sub addresses: 200Fh to 2011h)

These set the vertical black frame display range for the black frame block in 11 bits. The range can be set in 1-line units. Set the "display range – 2" value.



(g) FRM_ON (sub address: 2000h)

This sets the processing ON/OFF for the black frame block.

Setting value: 1 = Black frame processing ON, 0 = Black frame processing OFF

(h) FRM_DAT[9:0] (sub addresses: 2012h and 2016h)

This sets the data for the black frame processing block in 10 bits.

(i) MUTE1_ON (sub address: 2000h)

This sets the mute 1 block processing ON/OFF.
Setting value: 1 = Mute 1 processing ON, 0 = Mute 1 processing OFF

(j) R_MUTE1[9:0], G_MUTE1[9:0] and B_MUTE1[9:0] (sub addresses: 2013h to 2016h)

These set the R, G and B mute 1 block data in 10 bits.

(k) R_OSD_DAT1 to 4[9:0], G_OSD_DAT1 to 4[9:0] and B_OSD_DAT1 to 4[9:0] (sub addresses: 2017h to 2025h)

These set the OSD block signal gradual level of R, G and B in 10 bits.

(l) GAM_ON (sub address: 2000h)

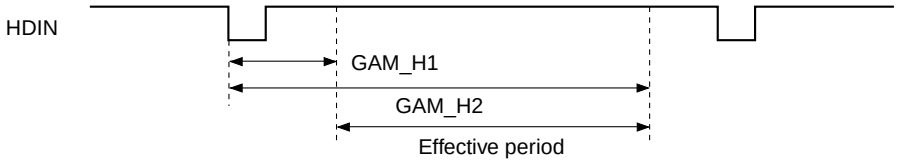
This sets the gamma correction block processing ON/OFF.
Setting value: 1 = Gamma correction processing ON, 0 = Gamma correction processing OFF

(m) GAM_MODE (sub address: 2001h)

This sets the gamma correction block RAM operation.
Setting value: 1 = Normal operation mode, 0 = Power-saving mode

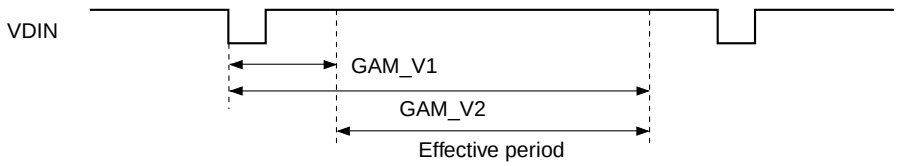
(n) GAM_H1[10:0] and GAM_H2[10:0] (sub addresses: 2026h to 2028h)

These set the horizontal gamma correction processing range in 11 bits. The range can be set in 1-dot units. Set it to match the effective period of the video signal. Set the "effective period" value.



(o) GAM_V1[10:0] and GAM_V2[10:0] (sub addresses: 2029h to 202Bh)

These set the vertical gamma correction processing range in 11 bits. The range can be set in 1-line units. Set it to match the effective period of the video signal. Set the "effective period – 2" value.



(p) R_GAM_GAIN[7:0], G_GAM_GAIN[7:0] and B_GAM_GAIN[7:0] (sub addresses: 202Ch to 202Eh)

These set the R, G and B gamma gain block arithmetic coefficient in 8 bits.

(q) R_GAM_BRT[10:0], G_GAM_BRT[10:0] and B_GAM_BRT[10:0] (sub addresses: 202Fh to 2033h)

These set the R, G and B gamma bright block arithmetic coefficient 11 bits with code.

(r) MUTE2_ON (sub address: 2000h)

This selects the mute 2 block processing ON/OFF.
Setting value: 1 = Mute 2 processing ON, 0 = Mute 2 processing OFF

(s) R_MUTE2[9:0], G_MUTE2[9:0] and B_MUTE2[9:0] (sub addresses: 2034h to 2037h)

These set the R, G and B mute 2 block data in 10 bits.

(t) LIM_ON (sub address: 2000h)

This sets the limiter block processing ON/OFF.
Setting value: 1 = Limiter processing ON, 0 = Limiter processing OFF

(u) L_LIM_DAT[9:0] and H_LIM_DAT[9:0] (sub addresses: 2037h and 203Ah)

These set the limiter block data in 10 bits.

(v) GC_ON (sub address: 2000h)

This sets the ghost cancel block processing ON/OFF.
Setting value: 1 = Ghost cancel ON, 0 = Ghost cancel OFF

(w) GC_MODE (sub address: 2001h)

This sets the signal processing period of ghost cancel block.
Setting value: 1 = 12-dot period, 0 = 6-dot period

(x) R_GC_LIM_DAT[9:0], G_GC_LIM_DAT[9:0] and B_GC_LIM_DAT[9:0] (sub addresses: 203Ah to 203Dh)

These set the limiter data of the R, G and B ghost cancel block in 10 bits.

(y) R_GC_ATT[7:0], G_GC_ATT[7:0] and B_GC_ATT[7:0] (sub addresses: 203Fh to 2040h)

These set the multiplier arithmetic coefficient of the R, G and B ghost cancel block in 8 bits.

(z) OFFSET_ON (sub address: 2000h)

This sets the cycle offset block processing ON/OFF.

Setting value: 1 = Offset processing ON, 0 = Offset processing OFF

(A) OFFSET_MODE (sub address: 2001h)

This sets the counter cycle of cycle offset block.

Setting value: 1 = 12-dot period, 0 = 6-dot period

(B) R_OFFSET1 to 12[3:0], G_OFFSET1 to 12[3:0] and B_OFFSET1 to 12[3:0] (sub addresses: 2041h to 2052h)

These set the offset data for the cycle offset block in 4 bits with code.

Color Shading Correction Block Register

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
3000h	—	CSC_ON	CSC_XH	CSC_DWN	CSC_R_RGT	CSC_G_RGT	CSC_B_RGT	CSC_HP[8]	00h
3001h	CSC_HP[7:0]								00h
3002h	CSC_VP[7:0]								00h
3003h	—	—	CSC_HNUM[5:0]						00h
3004h	—	—	CSC_VNUM[5:0]						00h
3005h	—	—	CSC_HINT[7:2]						00h
3006h	—	—	CSC_VINT[7:2]						00h
3007h	—	—	CSC_HOS[7:2]						00h
3008h	—	—	CSC_VOS[7:2]						00h
3009h	—	—	—	—	—	CSC_GNUM[2:0]			00h
300Ah	CSC_RGP1[9]	CSC_RGP2[9]	CSC_RGP3[9]	CSC_RGP4[9]	CSC_RGP5[9]	CSC_RGP6[9]	CSC_RGP7[9]	CSC_RGP8[9]	00h
300Bh	CSC_RGP1[8:1]								00h
300Ch	CSC_RGP2[8:1]								00h
300Dh	CSC_RGP3[8:1]								00h
300Eh	CSC_RGP4[8:1]								00h
300Fh	CSC_RGP5[8:1]								00h
3010h	CSC_RGP6[8:1]								00h
3011h	CSC_RGP7[8:1]								00h
3012h	CSC_RGP8[8:1]								00h
3013h	CSC_GGP1[9]	CSC_GGP2[9]	CSC_GGP3[9]	CSC_GGP4[9]	CSC_GGP5[9]	CSC_GGP6[9]	CSC_GGP7[9]	CSC_GGP8[9]	00h
3014h	CSC_GGP1[8:1]								00h
3015h	CSC_GGP2[8:1]								00h
3016h	CSC_GGP3[8:1]								00h
3017h	CSC_GGP4[8:1]								00h
3018h	CSC_GGP5[8:1]								00h
3019h	CSC_GGP6[8:1]								00h
301Ah	CSC_GGP7[8:1]								00h
301Bh	CSC_GGP8[8:1]								00h
301Ch	CSC_BGP1[9]	CSC_BGP2[9]	CSC_BGP3[9]	CSC_BGP4[9]	CSC_BGP5[9]	CSC_BGP6[9]	CSC_BGP7[9]	CSC_BGP8[9]	00h
301Dh	CSC_BGP1[8:1]								00h
301Eh	CSC_BGP2[8:1]								00h
301Fh	CSC_BGP3[8:1]								00h
3020h	CSC_BGP4[8:1]								00h
3021h	CSC_BGP5[8:1]								00h
3022h	CSC_BGP6[8:1]								00h
3023h	CSC_BGP7[8:1]								00h

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
3024h	CSC_BGP8[8:1]								00h
3025h	CSC_RGD1	CSC_RGD2	CSC_RGD3	CSC_RGD4	CSC_RGD5	CSC_RGD6	CSC_RGD7	CSC_RGD8	00h
3026h	CSC_GGD1	CSC_GGD2	CSC_GGD3	CSC_GGD4	CSC_GGD5	CSC_GGD6	CSC_GGD7	CSC_GGD8	00h
3027h	CSC_BGD1	CSC_BGD2	CSC_BGD3	CSC_BGD4	CSC_BGD5	CSC_BGD6	CSC_BGD7	CSC_BGD8	00h
3028h	CSC_XH_DAT[9:2]								00h

—: Don't care

The detailed setting contents of color shading correction are described below.

(a) CSC_ON (sub address: 3000h)

This sets the processing ON/OFF for the color shading correction block.
Setting value: 1 = ON, 0 = OFF

(b) CSC_R_RGT, CSC_G_RGT and CSC_B_RGT (sub address: 3000h)

These set the right/left inversion for the color shading correction block.
Setting value: 1 = Reflects the TG block RGT setting, 0 = Reflects the inverse of TG block RGT setting

(c) CSC_DWN (sub address: 3000h)

This sets the up/down inversion for the color shading correction block.
Setting value: 1 = Reflects the TG block DWN setting, 0 = Reflects the inverse of TG block DWN setting

(d) CSC_HP[8:0] (sub addresses: 3000h and 3001h)

This sets the horizontal correction start position for the color shading correction block in 9 bits. The position can be set in 1-dot units. The setting range is 020h to 1FEh. Set the "correction start position + 7" value.

(e) CSC_VP[7:0] (sub address: 3002h)

This sets the vertical correction start position for the color shading correction block in 8 bits. The position can be set in 1-line units. The setting range is 00h to FEh. Set the "correction start position – 4" value.

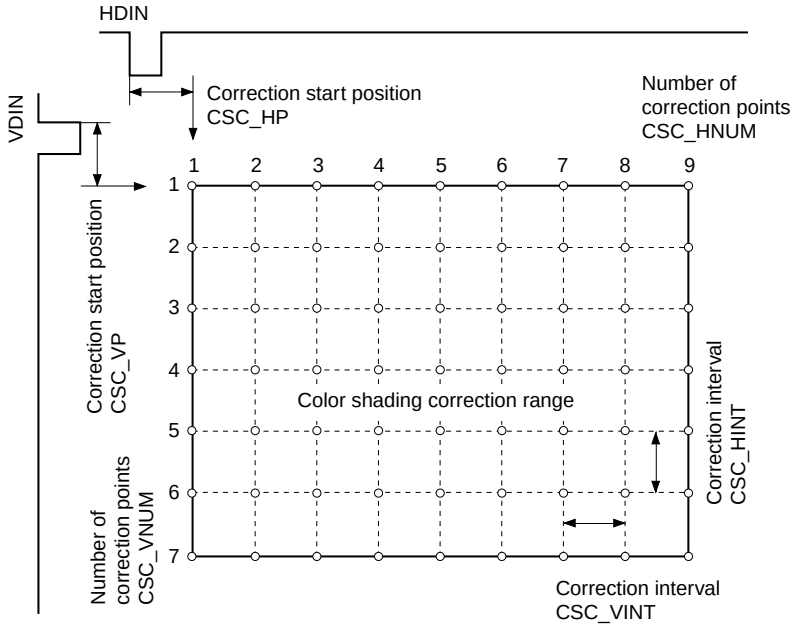
(f) CSC_HNUM[5:0] and CSC_VNUM[5:0] (sub addresses: 3003h and 3004h)

These set the number of horizontal and vertical correction points for the color shading correction block in 6 bits in the range of 2 to 64 points. Set the "number of correction points – 1" value. The size of the RAM for setting the correction data is 1792 words, so set the number of correction points as follows.

Number of horizontal correction points $\times$ Number of vertical correction points
$\times$ Number of gradual correction points $\leq$ 1792

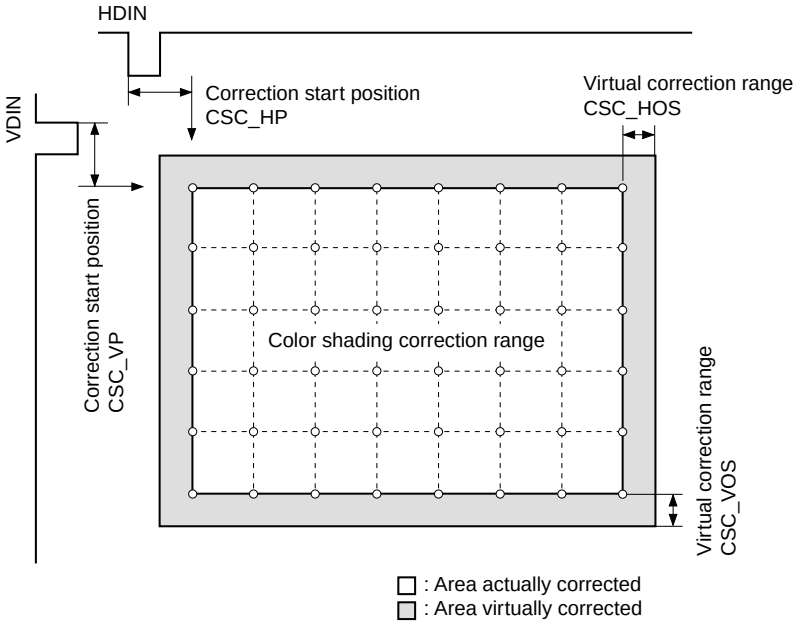
(g) CSC_HINT[7:2] and CSC_VINT[7:2] (sub addresses: 3005h and 3006h)

These set the correction interval for the horizontal and vertical directions of the color shading correction block in 6 bits. This setting has a setting range from 32 to 256 dots (lines) and can be set in 4-dot (-line) units.
Set the "correction interval/4 – 1" value.



(h) CSC_HOS[7:2] and CSC_VOS[7:2] (sub addresses: 3007h and 3008h)

These set the range for which virtual corrections are to be made. The same data as at the edge of the correction area for color shading correction is assumed for outside the correction area. It is possible to independently set values from 0 to 256 dots (lines) for the horizontal and vertical directions in 4-dot (-line) units.

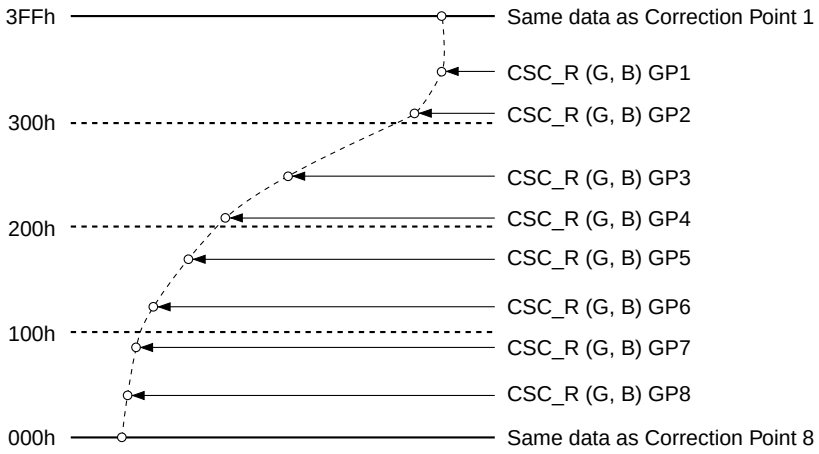


(i) CSC_GNUM [2:0] (sub address: 3009h)

This sets the number of correction points in the gradual direction for color shading correction. It is possible to set 1 to 8 points. Set the "number of correction points – 1" value.

(j) CSC_RGP1 to 8[9:1], CSC_GGP1 to 8[9:1] and CSC_BGP1 to 8[9:1] (sub addresses: 300Ah to 3024h)

These set the correction points for color shading correction in the gradual direction in 2-gradual units independently for each R, G and B signal. Registers are set in order of lowest number beginning from 3FFh. Always keep this order in mind when setting data.



(k) CSC_RGD1 to 8, CSC_GGD1 to 8 and CSC_BGD1 to 8 (sub addresses: 3025h to 3027h)

These set to expand data set in RAM for color shading correction by ± 8bits by shifting data 1 bit in the MSB direction. This setting can be made independently for correction points in the gradual direction for each R, G and B signal.

Setting value: 1 = Expand by ±8 bits; 0 = Not expanded

(l) CSC_XH (sub address: 3000h)

This sets the cross hatch display ON/OFF used during color shading correction.

Setting value: 1 = Display; 0 = Not displayed

(m) CSC_XH_DAT (sub address: 3028h)

This sets the display level (gradual level) of the cross hatch pattern used for color shading correction in 2-gradual units, 9 bits.

Pattern Generator Block Register

Sub address	Data								Initial value
	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	
4000h	PG_ON	PG_R_ON	PG_G_ON	PG_B_ON	—	PG_PAT[2:0]			00h
4001h	—	—	—	PG_STRP_SW	PG_R_SEL	PG_G_SEL	PG_B_SEL	PG_STAIR_SW	00h
4002h	—	PG_HST[10:8]			—	PG_HSTP[10:8]			00h
4003h	PG_HST[7:0]								00h
4004h	PG_HSTP[7:0]								00h
4005h	—	PG_HWST[10:8]			—	PG_HWSTP[10:8]			00h
4006h	PG_HWST[7:0]								00h
4007h	PG_HWSTP[7:0]								00h
4008h	—	PG_VST[10:8]			—	PG_VSTP[10:8]			00h
4009h	PG_VST[7:0]								00h
400Ah	PG_VSTP[7:0]								00h
400Bh	—	PG_VWST[10:8]			—	PG_VWSTP[10:8]			00h
400Ch	PG_VWST[7:0]								00h
400Dh	PG_VWSTP[7:0]								00h
400Eh	PG_STEP[7:0]								00h
400Fh	PG_WIDTH[7:0]								00h
4010h	—	—	—	—	PG_SIG1R[9:8]		PG_SIG2R[9:8]		00h
4011h	PG_SIG1R[7:0]								00h
4012h	PG_SIG2R[7:0]								00h
4013h	PG_SIG1G[9:8]		PG_SIG2G[9:8]		PG_SIG1B[9:8]		PG_SIG2B[9:8]		00h
4014h	PG_SIG1G[7:0]								00h
4015h	PG_SIG2G[7:0]								00h
4016h	PG_SIG1B[7:0]								00h
4017h	PG_SIG2B[7:0]								00h

—: Don't care

The detailed setting contents of PG block are described below.

(a) PG_ON (sub address: 4000h)

This sets the test signal output ON/OFF.
Setting value: 1 = Test pattern output mode enabled, 0 = Normal signal output

(b) PG_R (G, B)_ON (sub address: 4000h)

These set the test signal level setting ON/OFF.
Setting value: 1 = Various settings enabled, 0 = Output fixed to "0"

(c) PG_PAT[2:0] (sub address: 4000h)

This switches the display pattern within the window area.
Setting value: See the table below.

0	Raster
1	Window
2	Vertical stripe/diagonal stripe
3	Horizontal stripe
4	Cross hatch
5	Dot
6	Horizontal ramp/horizontal stair
7	Vertical ramp/vertical stair

(d) PG_R (G, B)_SEL (sub address: 4001h)

These switch the pattern and non-pattern signal levels within the effective area.
Setting value: 1 = Pattern signal level is PG_SIG1R (G, B), 0 = Pattern signal level is PG_SIG2R (G, B)

(e) PG_STRP_SW (sub address: 4001h)
(Valid only when PG_PAT[2:0] = 2h)

This switches between vertical stripe and diagonal stripe.
Setting value: 1 = Diagonal stripe, 0 = Vertical stripe

(f) PG_STAIR_SW (sub address: 4001h)
(Valid only when PG_PAT[2:0] = 6h or 7h)

This switches between ramp and stair.
Setting value: 1 = Stair, 0 = Ramp

(g) PG_HST[10:0] (sub addresses: 4002h and 4003h)
PG_HSTP[10:0] (sub addresses: 4002h and 4004h)

These set the horizontal effective area in 11 bits. The area can be set in 1-dot units.

(h) PG_HWST[10:0] (sub addresses: 4005h and 4006h)
PG_HWSTP[10:0] (sub addresses: 4005h and 4007h)

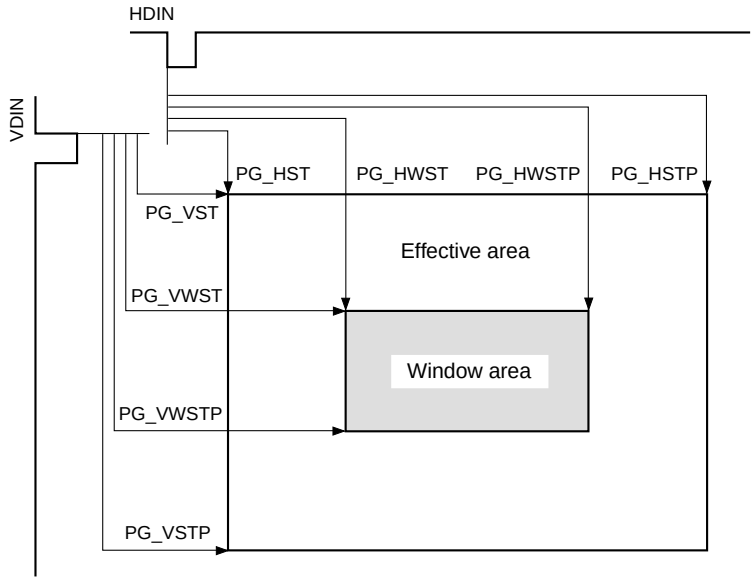
These set the horizontal window area in 11 bits. The area can be set in 1-dot units.

(i) PG_VST[10:0] (sub addresses: 4008h and 4009h)
PG_VSTP[10:0] (sub addresses: 4008h and 400Ah)

These set the vertical effective area in 11 bits. The area can be set in 1-line units.

(j) PG_VWST[10:0] (sub addresses: 400Bh and 400Ch)
PG_VWSTP[10:0] (sub addresses: 400Bh and 400Dh)

These set the vertical window area in 11 bits. The area can be set in 1-line units.



(k) PG_STEP[7:0] (sub address: 400Eh)
(Valid for PG_PAT[2:0] = 2h, 3h, 4h and 5h)

This sets the vertical stripe, diagonal stripe, horizontal stripe, cross hatch and dot period in 8 bits. The period can be set in 1-dot units.

(l) PG_WIDTH[7:0] (sub address: 400Fh)
(Valid for PG_PAT[2:0] = 2h, 3h, 4h and 5h)

This sets the vertical stripe, diagonal stripe, horizontal stripe, cross hatch and dot line width in 8 bits. The width can be set in 1-dot units.

(m) PG_SIG1R (G, B)[9:0] and PG_SIG2R (G, B)[9:0] (sub addresses: 4010h to 4017h)

These set the output signal level inside and outside the pattern area within the effective area in 10 bits. The level can be set with an accuracy of 1 bit.

Gamma Correction Block

Set the data for the internal RAM of the gamma correction block by dividing 10-bit gamma correction data with 2 bytes as shown in the figure below. First, set 1-byte data of LSB.

Sub address	MSB							LSB	RAM address
8000h	D7	D6	D5	D4	D3	D2	D1	D0	000h
8001h	—	—	—	—	—	—	D9	D8	
8002h	D7	D6	D5	D4	D3	D2	D1	D0	001h
8003h	—	—	—	—	—	—	D9	D8	
. . . . . .									. . . . . .
87FEh	D7	D6	D5	D4	D3	D2	D1	D0	3FFh
87FFh	—	—	—	—	—	—	D9	D8	

—: Don't care

Red Gamma Correction Block Setting Example

Color Shading Correction Block

Set the data for the internal RAM of the color shading correction block by putting in order from the correction data at the upper left of the Screen 1 (correction start position).
The following is a setting example of 17 horizontal points × 13 vertical points × 3 gradual points = 663 points.

Sub address	MSB							LSB	RAM address	
C000h	D7	D6	D5	D4	D3	D2	D1	D0	000h (Upper left)	
. . . .									. . . .	Screen 1 correction data
C0DCh	D7	D6	D5	D4	D3	D2	D1	D0	0DCh (Lower right)	
C0DDh	D7	D6	D5	D4	D3	D2	D1	D0	0DDh (Upper left)	
. . . .									. . . .	Screen 2 correction data
C1B9h	D7	D6	D5	D4	D3	D2	D1	D0	1B9h (Lower right)	
C1BAh	D7	D6	D5	D4	D3	D2	D1	D0	1BAh (Upper left)	
. . . .									. . . .	Screen 3 correction data
C296h	D7	D6	D5	D4	D3	D2	D1	D0	296h (Lower right)	

Red Color Shading Correction Block Setting Example

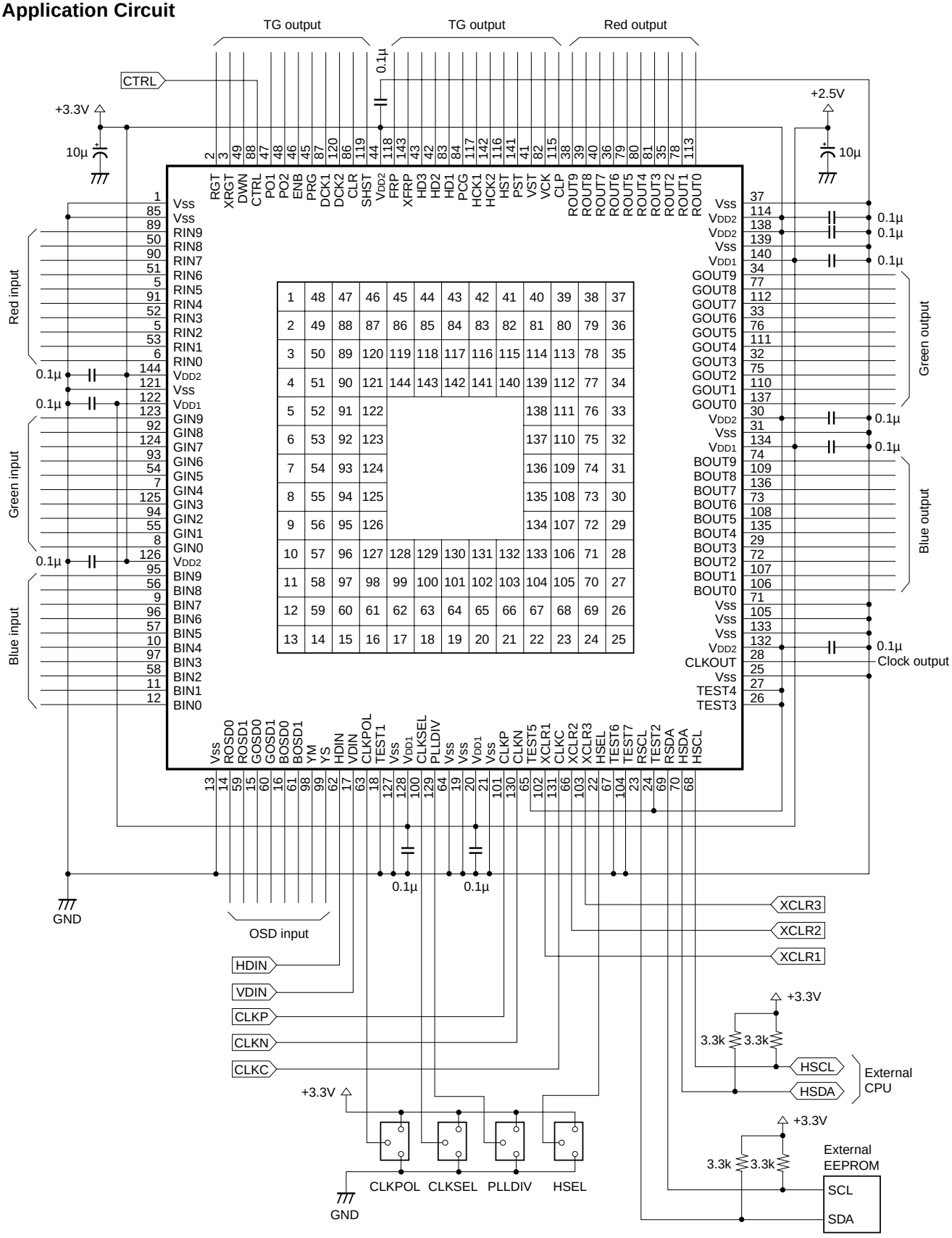
Notes on Handling

- The power supply and GND patterns have a large effect on undesired radiation on the substrate and interference to analog circuits, etc.

General precautions are as follows.

- Make the GND pattern as wide as possible. Using a multi-layer substrate and a solid ground is recommended.
- Connect each power supply pin to GND via a ceramic chip capacitor of 0.1µF or more located as close to each pin as possible.
- Do not use this IC under conditions other than the recommended operating conditions.
- Absolute maximum rating values should not be exceeded even momentarily. Exceeding that ratings may damage the device, leading to eventual breakdown.
- This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.
- Since this IC utilizes a MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, interface with two power supplies of another circuit, or the order in which power is supplied to circuits. Make a thorough study of measures against the possibility of latch up before use.
- When the initialization of this IC is performed at power-on, system clear cancellation is performed after the supply voltage is set in the range of the recommended operating conditions and stabilized. Keep in mind that the internal circuit may not be initialized correctly if system clear cancellation is performed before the supply voltage is set in the range of the recommended operating conditions.
- When designing the substrate, take sufficient care for the surrounding temperature and heat radiation, and make sure the IC junction temperature does not exceed the maximum value.
- Be sure to make the number of dot clocks input to the CXD3526GG in 1H an even number. Note that if there is an odd number of dot clocks, the internal phase compensation PLL will not operate properly.
- Be sure to make a thorough evaluation of any items not listed in this data sheet.

Application Circuit

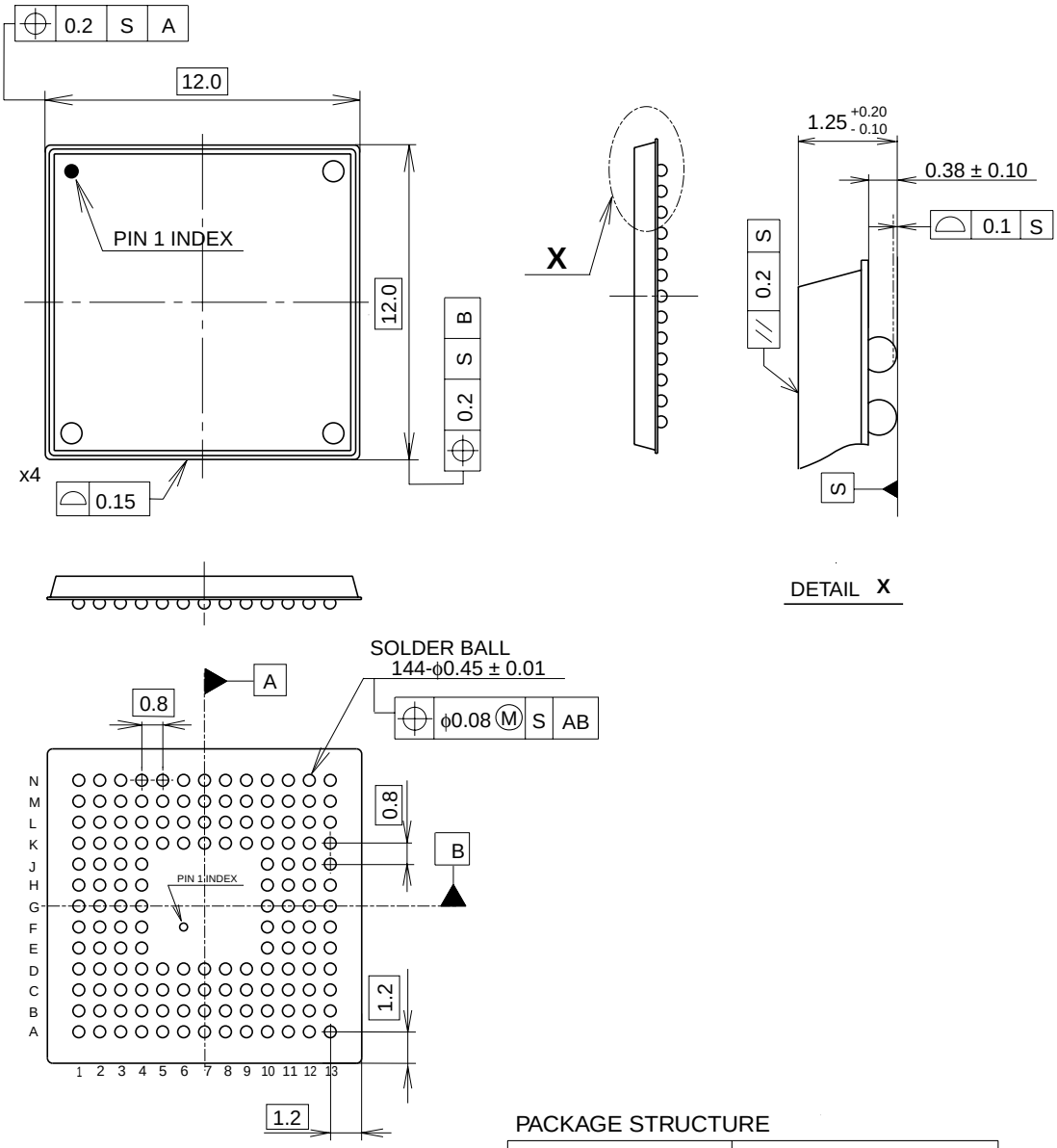


1	48	47	46	45	44	43	42	41	40	39	38	37
2	49	88	87	86	85	84	83	82	81	80	79	36
3	50	89	120	119	118	117	116	115	114	113	78	35
4	51	90	121	144	143	142	141	140	139	112	77	34
5	52	91	122						138	111	76	33
6	53	92	123						137	110	75	32
7	54	93	124						136	109	74	31
8	55	94	125						135	108	73	30
9	56	95	126						134	107	72	29
10	57	96	127	128	129	130	131	132	133	106	71	28
11	58	97	98	99	100	101	102	103	104	105	70	27
12	59	60	61	62	63	64	65	66	67	68	69	26
13	14	15	16	17	18	19	20	21	22	23	24	25

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

144PIN BGA



SONY CODE	BGA-144P-021
JEITA CODE	P-BGA144-12X12-0.8
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
BOARD MATERIAL	COPPER-CLAD LAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE MASS	0.31g