CS4172

Single Air-Core Gauge Driver

Description

The CS4172 is a monolithic BiCMOS integrated circuit used to translate a digital 10-bit word from a microprocessor/microcontroller to complementary DC outputs. The DC outputs drive an air-core meter commonly used in vehicle instrument panels. The 10 bits of data are used to linearly control the quadrature coils of the meter directly with a 0.35° resolution and ±1.0° accuracy over the full 360° range of the gauge. The interface from the microcontroller is by a Serial Peripheral Interface (SPI) compatible serial connection using up to a 2MHz shift clock rate.

The digital code, which is directly proportional to the desired gauge pointer deflection, is shifted into a DAC and multiplexer. These two blocks provide a tangential conversion function to change the digital data into the appropriate DC coil voltage for the angle demanded. The tangential algorithm creates approximately 40% more torque in the meter movement than does a sin-cos algorithm at 45°, 135°,

225°, and 315° angles. This increased torque reduces the error due to pointer droop at these critical angles.

Each output buffer is capable of supplying up to 80mA per coil and are controlled by a common enable pin. When OE is low the output buffers are turned off but the logic portion of the chip remains powered and continues to operate normally.

The Serial Gauge Driver is self-protected against output short circuit conditions. The output drivers are disabled anytime the on-chip protection circuitry detects a short circuit condition. The outputs remain off until a falling edge is presented on CS. If the short circuit is still present the output drivers automatically disable themselves again. A thermal protection circuit limits the junction temperature to approximately 160°C for conditions of high supply voltage and high ambient temperature.

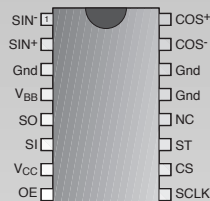The status pin (ST) reflects the state of the outputs and is low whenever the outputs are disabled.
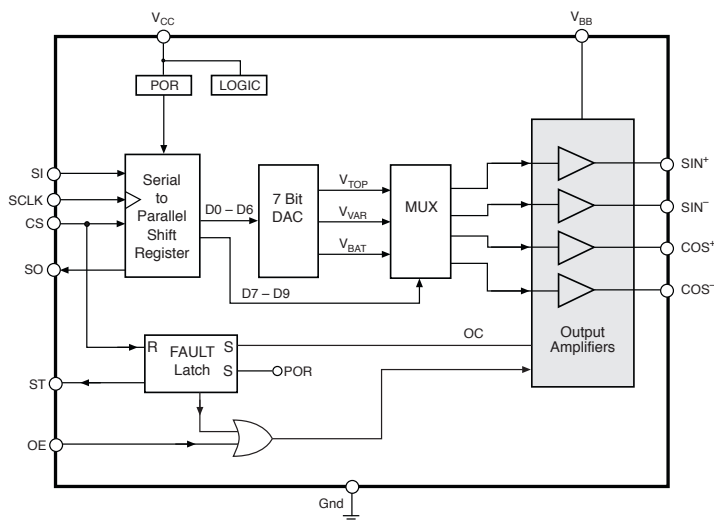
Features

- **Serial Input Bus**
- **2 MHz Operating Frequency**
- **Tangential Drive Algorithm**
- **80mA Drive Circuits**
- **0.5° Accuracy (Typ.)**
- **Power-On-Reset**
- **Protection Features
  Output Short Circuit
  Overtemperature**

Package Options

16 Lead PDIP

```
SIN⁻  1          COS⁺
SIN⁺             COS⁻
Gnd              Gnd
V_BB             Gnd
SO               NC
SI               ST
V_CC             CS
OE               SCLK
```

16 Lead SO Wide
(internally fused leads)
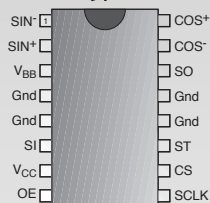
```
SIN⁻  1          COS⁺
SIN⁺             COS⁻
V_BB             SO
Gnd              Gnd
Gnd              Gnd
SI               ST
V_CC             CS
OE               SCLK
```

Block Diagram

Absolute Maximum Ratings

Supply Voltage

V_{BB} ....-1.0V to 15.0V

V_{CC} ....-1.0V to 6.0V

Digital Inputs ....-1.0V to 6.0V

Ground Potential Difference (|AGnd-DGnd|)...0.5V

Steady State Output Current ....±100mA

Forced Injection Current (Inputs and Supply)..±10mA

Operating Junction Temperature (T_J) ....150°C

Storage Temperature Range ....-65°C to 150°C

Lead Temperature Soldering

Wave Solder (through hole styles only) ....10 sec. max, 260°C peak

Reflow (SMD styles only) ....60 sec. max above 183°C, 230°C peak

ESD Susceptibility (Human Body Model)..2kV

Electrical Characteristics: -40°C ≤ T_A ≤ 105°C; 7.5V ≤ V_{BB} ≤ 14V; 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **Supply Voltages and Currents**					
V_{BB} Quiescent Current	Output disabled (OE = 0V)		1	5	mA
	[R_{COS}, R_{SIN} = $R_{L(MIN)}$] @45° (code = X'080) V_{BB} = 14V			175	mA
V_{CC} Quiescent Current	OE = high, V_{BB} = 0V SCLK = 2.0MHz			1	mA
■ **Digital Inputs and Outputs**					
Output High Voltage	SO, I_{OH} = 0.8mA	V_{CC} - 0.8			V
Output Low Voltage	SO, I_{OL} =0.8mA			0.4	V
	ST, I_{OL} = 2.5mA			0.8	V
Output High Current	ST, V_{CC} = 5.0V			25	μA
Input High Voltage	CS, SCLK, SI, OE	$0.7 \times V_{CC}$			V
Input Low Voltage	CS, SCLK, SI, OE			$0.3 \times V_{CC}$	V
Input High Current	CS, SCLK, SI, OE; V_{IN} = $0.7 \times V_{CC}$			1	μA
Input Low Current	CS, SCLK, SI, OE; V_{IN} = $0.3 \times V_{CC}$			1	μA
■ **Analog Outputs**					
Output Function Accuracy		-1.2		+1.2	deg
Output Shutdown Current, Source	V_{BB} = 14.0V	70		250	mA
Output Shutdown Current, Sink	V_{BB} = 14.0V	70		250	mA
Output Shutdown Current, Source	V_{BB} = 7.5V	43		250	mA
Output Shutdown Current, Sink	V_{BB} = 7.5V	43		250	mA
Coil Drive Output Voltage			$0.748 \times V_{BB}$		V
Minimum Load Resistance	T_A = 105°C		229		Ω
	T_A = 25°C		171		Ω
	T_A = -40°C		150		Ω

Electrical Characteristics: -40°C ≤ T_A ≤ 105°C; 7.5V ≤ V_{BB} ≤ 14V; 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shift Clock Frequency				2.0	MHz
SCLK High Time		175			ns
SCLK Low Time		175			ns
SO Rise Time	0.75V to V_{CC} - 1.2V; C_L = 90pF			150	ns
SO Fall Time	0.75V to V_{CC} - 1.2V; C_L = 90pF			150	ns
SO Delay Time	C_L = 90pF			150	ns
SI Setup Time		75			ns
SI Hold Time		75			ns
CS Setup Time		0			ns
CS Hold Time		75			ns

Package Pin Description

PACKAGE PIN#		PIN SYMBOL	FUNCTION
16 Lead SO Wide	16 Lead PDIP		
1	1	SIN⁻	Negative output for SINE coil.
2	2	SIN⁺	Positive output for SINE coil.
3	4	V_{BB}	Analog supply. Nominally 13.5V.
4,5,12,13	3,13,14	Gnd	Ground.
6	6	SI	Serial data input. Data present at the rising edge of the clock signal is shifted into the internal shift register.
7	7	V_{CC}	5V logic supply. The internal registers and latches are reset by a POR generated by the rising edge of the voltage on this pin.
8	8	OE	Controls the state of the output buffers. A logic low on this pin turns them off.
9	9	SCLK	Serial clock for shifting in/out of data. Rising edge shifts data on SI into the shift register and the falling edge changes the data on SO.
10	10	CS	When high allows data at SI to be shifted into part with the rising edges of SCLK. The falling edge transfers the shift register contents into the DAC and multiplexer to update the output buffers. The falling edge also re-enables the output drivers if they have been disabled by a fault.
11	11	ST	STATUS reflects the state of the outputs and is low anytime the outputs are disabled, either by OE or the internal protection circuitry. Requires external pull-up resistor.
14	5	SO	Serial data output. Existing 10-bit data is shifted out when new data is shifted in. Allows cascading of multiple devices on common serial port.
15	15	COS⁻	Negative output for COSINE coil.
16	16	COS⁺	Positive output for COSINE coil.
	12	NC	No connection.

The SACD is for interfacing between a microcontroller or microprocessor and air-core meter movements commonly used in automotive vehicles for speedometers and tachometers. These movements are built using 2 coils placed at a 90° orientation to each other. A magnetized disc floats in the middle of the coils and responds to the magnetic field generated by each coil. The disc has a shaft attached to it that protrudes out of the assembly. A pointer indicator is attached to this shaft and in conjunction with a separate printed scale displays the vehicle's speed or the engine's speed.

The disc (and pointer) respond to the vector sum of the voltages applied to the coils. Ideally, this relationship follows a $\frac{sine}{cosine}$ equation. Since this is a transcendental and non-linear function, devices of this type use an approximation for this relationship. The SACD uses a tangential algorithm as shown in Figure 1. Only 1 output varies in any 45 degree range.
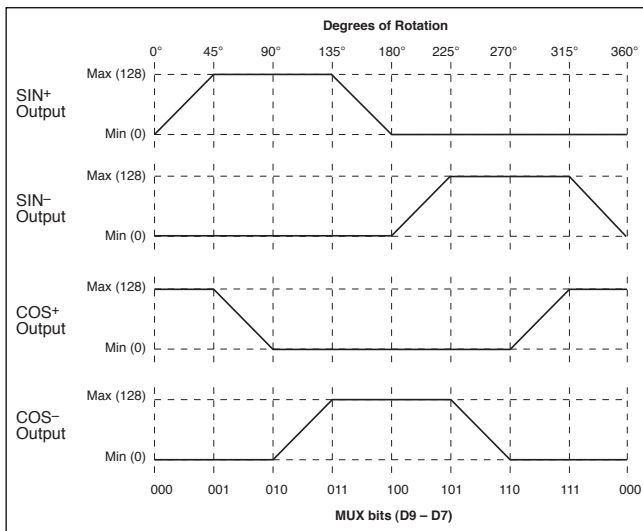

Figure 1. Major gauge outputs.

Quadrant I

$$\theta = \text{Tan}^{-1}\left[\frac{V_{SIN+} - V_{SIN-}}{V_{COS+} - V_{COS-}}\right]$$

For $\theta = 0.176°$ to $44.824°$:
$\qquad V_{SIN} = \text{Tan}\theta \times 0.748 \times V_{BB}$
$\qquad V_{COS} = 0.748 \times V_{BB}$

For $\theta = 45.176°$ to $89.824°$:
$\qquad V_{SIN} = 0.748 \times V_{BB}$
$\qquad V_{COS} = \text{Tan}(90° - \theta) \times 0.748 \times V_{BB}$

Quadrant II

$$\theta = 180° - \text{Tan}^{-1}\left[\frac{V_{SIN+} - V_{SIN-}}{V_{COS+} - V_{COS-}}\right]$$

For $\theta = 90.176°$ to $134.824°$:
$\qquad V_{SIN} = 0.748 \times V_{BB}$
$\qquad V_{COS} = -\text{Tan}(\theta - 90°) \times 0.748 \times V_{BB}$

For $\theta = 135.176°$ to $179.824°$:
$\qquad V_{SIN} = \text{Tan}(180° - \theta) \times 0.748 \times V_{BB}$
$\qquad V_{COS} = -0.748 \times V_{BB}$

Quadrant III

$$\theta = 180° + \text{Tan}^{-1}\left[\frac{V_{SIN+} - V_{SIN-}}{V_{COS+} - V_{COS-}}\right]$$

For $\theta = 180.176°$ to $224.824°$:
$\qquad V_{SIN} = -\text{Tan}(\theta - 180°) \times 0.748 \times V_{BB}$
$\qquad V_{COS} = -0.748 \times V_{BB}$

For $\theta = 225.176° - 269.824°$:
$\qquad V_{SIN} = -0.748 \times V_{BB}$
$\qquad V_{COS} = -\text{Tan}(270° - \theta) \times 0.748 \times V_{BB}$

Quadrant IV

$$\theta = 360° - \text{Tan}^{-1}\left[\frac{V_{SIN+} - V_{SIN-}}{V_{COS+} - V_{COS-}}\right]$$

For $\theta = 270.176°$ to $314.824°$:
$\qquad V_{SIN} = -0.748 \times V_{BB}$
$\qquad V_{COS} = \text{Tan}(\theta - 270°) \times 0.748 \times V_{BB}$

For $\theta = 315.176° - 359.824°$:
$\qquad V_{SIN} = -\text{Tan}(360° - \theta) \times 0.748 \times V_{BB}$
$\qquad V_{COS} = 0.748 \times V_{BB}$
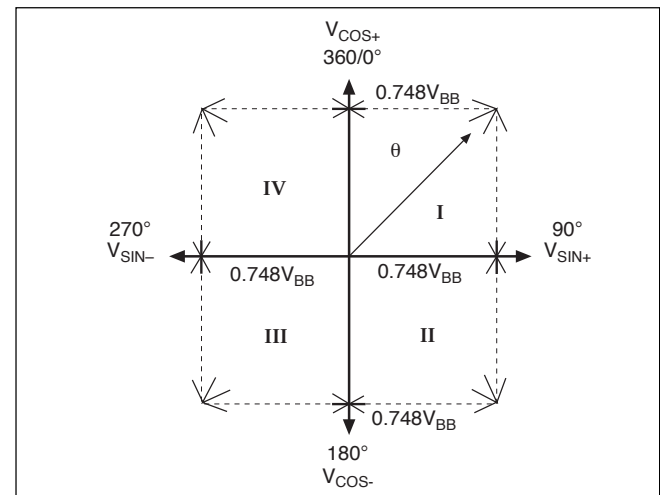
Graph 1. Major gauge response.

To drive the gauge's pointer to a particular angle, the microcontroller sends a 10-bit digital word into the serial port. These 10 bits are divided as shown in Figure 2. However, from a software programmers viewpoint, a 360° circle is divided into 1024 equal parts of .35° each. Table 1 shows the data associated with the 45° divisions of the 360° driver.
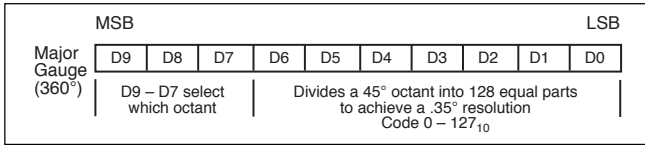

Figure 2. Definition of serial word.

Input Code (Decimal)	Ideal Degrees	Nominal Degrees	V_{SIN} (V)	V_{COS} (V)
0	0	0.176	0.032	10.476
128	45	45.176	10.476	10.412
256	90	90.176	10.476	-0.032
384	135	135.176	10.412	-10.476
512	180	180.176	-0.032	-10.476
640	225	225.176	-10.476	-10.412
768	270	270.176	-10.476	0.032
896	315	315.176	-10.476	10.476
1023	359.65	359.826	-0.032	10.476

Table 1. Nominal output for major gauge (V_{BB} = 14V).

The 10 bits are shifted into the device's shift register MSB first using an SPI compatible scheme. This method is shown in Figure 3. The CS must be high and remain high for SCLK to be enabled. Data on SI is shifted in on the rising edge of the synchronous clock signal. Data in the shift register changes at SO on the falling edge of SCLK. This arrangement allows the cascading of devices. SO is always enabled. Data shifts through without affecting the outputs until CS is brought low. At this time the internal DAC is updated and the outputs change accordingly.
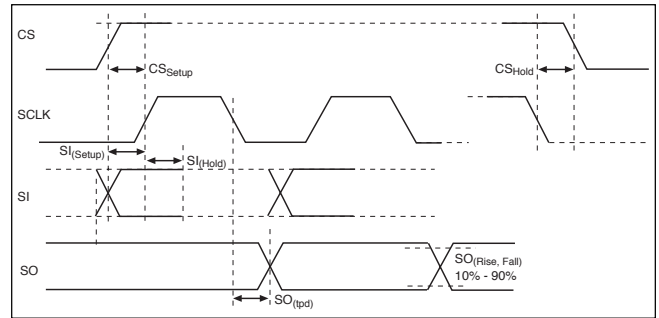

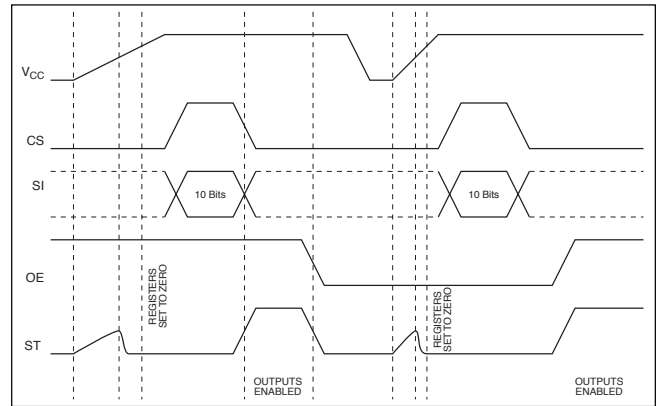**Figure 3. Serial data timing diagram.**

Figure 4. Power-up sequence.

Application Diagram

Package Specification

PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 Lead PDIP	19.69	18.67	.775	.735
16 Lead SO Wide*	10.50	10.10	.413	.398

PACKAGE THERMAL DATA

Thermal Data	16 Lead PDIP	16 Lead SO Wide*	
$R_{\Theta JC}$ typ	42	18	°C/W
$R_{\Theta JA}$ typ	80	75	°C/W

Plastic DIP (N); 300 mil wide

7.11 (.280) / 6.10 (.240)

8.26 (.325) / 7.62 (.300)

1.77 (.070) / 1.14 (.045)

2.54 (.100) BSC

3.68 (.145) / 2.92 (.115)

.356 (.014) / .203 (.008)

0.39 (.015) MIN.

.558 (.022) / .356 (.014)

D

Some 8 and 16 lead packages may have 1/2 lead at the end of the package. All specs are the same.

REF: JEDEC MS-001

Surface Mount Wide Body (DW); 300 mil wide

7.60 (.299) / 7.40 (.291)

10.65 (.419) / 10.00 (.394)

0.51 (.020) / 0.33 (.013)

1.27 (.050) BSC

2.49 (.098) / 2.24 (.088)

2.65 (.104) / 2.35 (.093)

1.27 (.050) / 0.40 (.016)

0.32 (.013) / 0.23 (.009)

D

0.30 (.012) / 0.10 (.004)

REF: JEDEC MS-013

Ordering Information

Part Number	Description
CS4172XN16	16 Lead PDIP
CS4172XDWF16	16 Lead SO Wide*
CS4172XDWFR16	16 Lead SO Wide* *(tape & reel)*

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Internally Fused Leads