Real-Time Analog Computational Unit (ACU)

AD538

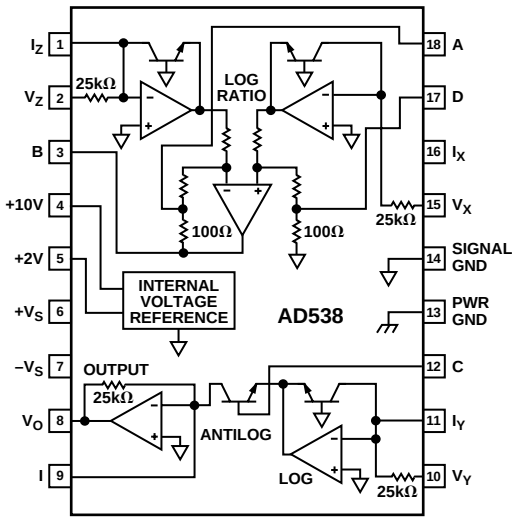
FEATURES

$V_{OUT} = V_Y \left(\frac{V_Z}{V_X}\right)^m$ Transfer Function
Wide Dynamic Range (Denominator) –1000:1
Simultaneous Multiplication and Division
Resistor-Programmable Powers and Roots
No External Trims Required
Low Input Offsets <100 μV
Low Error ±0.25% of Reading (100:1 Range)
+2 V and +10 V On-Chip References
Monolithic Construction

APPLICATIONS

One- or Two-Quadrant Mult/Div
Log Ratio Computation
Squaring/Square Rooting
Trigonometric Function Approximations
Linearization Via Curve Fitting
Precision AGC
Power Functions

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD538 is a monolithic real-time computational circuit that provides precision analog multiplication, division and exponentiation. The combination of low input and output offset voltages and excellent linearity results in accurate computation over an unusually wide input dynamic range. Laser wafer trimming makes multiplication and division with errors as low as 0.25% of reading possible, while typical output offsets of 100 μV or less add to the overall off-the-shelf performance level. Real-time analog signal processing is further enhanced by the device's 400 kHz bandwidth.

The AD538's overall transfer function is $V_O = V_Y (V_Z/V_X)^m$. Programming a particular function is via pin strapping. No external components are required for one-quadrant (positive input) multiplication and division. Two-quadrant (bipolar numerator) division is possible with the use of external level shifting and scaling resistors. The desired scale factor for both multiplication and division can be set using the on-chip +2 V or +10 V references, or controlled externally to provide simultaneous multiplication and division. Exponentiation with an *m* value from 0.2 to 5 can be implemented with the addition of one or two external resistors.

Direct log ratio computation is possible by using only the log ratio and output sections of the chip. Access to the multiple summing junctions adds further to the AD538's flexibility. Finally, a wide power supply range of ±4.5 V to ±18 V allows operation from standard ±5 V, ±12 V and ±15 V supplies.

The AD538 is available in two accuracy grades (A and B) over the industrial (–25°C to +85°C) temperature range and one grade (S) over the military (–55°C to +125°C) temperature range. The device is packaged in an 18-lead TO-118 hermetic side-brazed ceramic DIP. A-grade chips are also available.

PRODUCT HIGHLIGHTS

1. Real-time analog multiplication, division and exponentiation.
2. High accuracy analog division with a wide input dynamic range.
3. On-chip +2 V or +10 V scaling reference voltages.
4. Both voltage and current (summing) input modes.
5. Monolithic construction with lower cost and higher reliability than hybrid and modular circuits.

REV. C

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AD538—SPECIFICATIONS (V_S = ±15 V, T_A = +25°C unless otherwise noted)

Parameters	Conditions	AD538AD Min	AD538AD Typ	AD538AD Max	AD538BD Min	AD538BD Typ	AD538BD Max	AD538SD Min	AD538SD Typ	AD538SD Max	Units
MULTIPLIER DIVIDER PERFORMANCE											
Nominal Transfer Function	$10\ V \geq V_X, V_Y, V_Z \geq 0$	$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$			$V_O = Vy \left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$			
	$400\ \mu A \geq I_X, I_Y, I_Z \geq 0$	$V_O = 25\ k\Omega \times I_Y \left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y \left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y \left(\frac{I_Z}{I_X}\right)^m$			
Total Error Terms	100 mV ≤ V_X ≤ 10 V		±0.5	**±1**		±0.25	**±0.5**		±0.5	**±1**	% of Reading +
100:1 Input Range[1]	100 mV ≤ V_Y ≤ 10 V		±200	**±500**		±100	**±250**		±200	**±500**	µV
	100 mV ≤ V_Z ≤ 10 V $V_Z \leq 10\ V_X$, m = 1.0										
	$T_A = T_{MIN}$ to T_{MAX}		±1	**±2**		±0.5	**±1**		±1.25	**±2.5**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	µV
Wide Dynamic Range[2]	10 mV ≤ V_X ≤ 10 V		±1	**±2**		±0.5	**±1**		±1	**±2**	% of Reading +
	1 mV ≤ V_Y ≤ 10 V		±200	**±500**		±100	**±250**		±200	**±500**	µV +
	0 mV ≤ V_Z ≤ 10 V $V_Z \leq 10\ V_X$, m = 1.0		±100	**±250**		±750	**±150**		±200	**±250**	µV × (V_Y + V_Z)/V_X
	$T_A = T_{MIN}$ to T_{MAX}		±1	**±3**		±1	**±2**		±2	**±4**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	µV +
			±450	**±750**		±350	**±500**		±750	**±1000**	µV × (V_Y + V_Z)/V_X
Exponent (m) Range	$T_A = T_{MIN}$ to T_{MAX}	0.2		5	0.2		5	0.2		5	
OUTPUT CHARACTERISTICS											
Offset Voltage	V_Y = 0, V_C = –600 mV		±200	**±500**		±100	**±250**		±200	**±500**	µV
	$T_A = T_{MIN}$ to T_{MAX}		±450	**±750**		±350	**±500**		±750	**±1000**	µV
Output Voltage Swing	R_L = 2 kΩ	–11		**+11**	–11		**+11**	–11		**+11**	V
Output Current		5	10		5	10		5	10		mA
FREQUENCY RESPONSE											
Slew Rate			1.4			1.4			1.4		V/µs
Small Signal Bandwidth	100 mV ≤ 10 V_Y, V_Z, V_X ≤ 10 V		400			400			400		kHz
VOLTAGE REFERENCE											
Accuracy	V_{REF} = 10 V or 2 V		±25	**±50**		±15	**±25**		±25	**±50**	mV
Additional Error	$T_A = T_{MIN}$ or T_{MAX}		±20	**±30**		±20	**±30**		±30	**±50**	mV
Output Current	V_{REF} = 10 V to 2 V	1	2.5		1	2.5		1	2.5		mA
Power Supply Rejection											
+2 V = V_{REF}	±4.5 V ≤ V_S ≤ ±18 V		300	**600**		300	**600**		300	**600**	µV/V
+10 V = V_{REF}	±13 V ≤ V_S ≤ ±18 V		200	**500**		200	**500**		200	**500**	µV/V
POWER SUPPLY											
Rated	R_L = 2 kΩ		±15			±15			±15		V
Operating Range[3]		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
PSRR	±4.5 V < V_S < ±18 V V_X = V_Y = V_Z = 1 V V_{OUT} = 1 V		0.5	**0.1**		0.05	**0.1**		0.5	**0.1**	%/V
Quiescent Current			4.5	7		4.5	7		4.5	7	mA
TEMPERATURE RANGE											
Rated		–25		+85	–25		+85	–55		+125	°C
Storage		–65		+150	–65		+150	–65		+150	°C
PACKAGE OPTIONS											
Ceramic (D-18)			AD538AD			AD538BD			AD538SD AD538SD/883B		
Chips			AD538ACHIPS								

NOTES

[1]Over the 100 mV to 10 V operating range total error is the sum of a percent of reading term and an output offset. With this input dynamic range the input offset contribution to total error is negligible compared to the percent of reading error. Thus, it is specified indirectly as a part of the percent of reading error.

[2]The most accurate representation of total error with low level inputs is the summation of a percent of reading term, an output offset and an input offset multiplied by the incremental gain (V_Y + V_Z) V_X.

[3]When using supplies below ±13 V, the 10 V reference pin *must* be connected to the 2 V pin in order for the AD538 to operate correctly.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

RE-EXAMINATION OF MULTIPLIER/DIVIDER ACCURACY

Traditionally, the "accuracy" (actually the errors) of analog multipliers and dividers have been specified in terms of percent of full scale. Thus specified, a 1% multiplier error with a 10 V full-scale output would mean a worst case error of +100 mV at "any" level within its designated output range. While this type of error specification is easy to test evaluate, and interpret, it can leave the user guessing as to how useful the multiplier actually is at low output levels, those approaching the specified error limit (in this case) 100 mV.

The AD538's error sources do not follow the percent of full-scale approach to specification, thus it more optimally fits the needs of the very wide dynamic range applications for which it is best suited. Rather than as a percent of full scale, the AD538's error as a multiplier or divider for a 100:1 (100 mV to 10 V) input range is specified as the sum of two error components: a percent of reading (ideal output) term plus a fixed output offset. Following this format the AD538AD, operating as a multiplier or divider with inputs down to 100 mV, has a maximum error of ±1% of reading ±500 μV. Some sample total error calculations for both grades over the 100:1 input range are illustrated in the chart below. This error specification format is a familiar one to designers and users of digital voltmeters where error is specified as a percent of reading ± a certain number of digits on the meter readout.

For operation as a multiplier or divider over a wider dynamic range (>100:1), the AD538 has a more detailed error specification that is the sum of three components: a percent of reading term, an output offset term and an input offset term for the V_Y/V_X log ratio section. A sample application of this specification, taken from Table I, for the AD538AD with V_Y = 1 V, V_Z = 100 mV and V_X = 10 mV would yield a maximum error of ±2.0% of reading ±500 μV ±(1 V + 100 mV)/10 mV × 250 μV or ±2.0% of reading ±500 μV ± 27.5 mV. This example illustrates that with very low level inputs the AD538's incremental gain $(V_Y + V_Z)/V_X$ has increased to make the input offset contribution to error substantial.

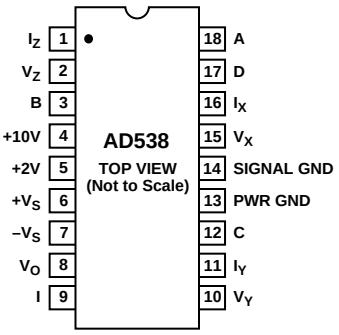
Table I. Sample Error Calculation Chart (Worst Case)

	V_Y Input (in V)	V_Z Input (in V)	V_X Input (in V)	Ideal Output (in V)	Total Offset Error Term (in mV)	% of Reading Error Term (in mV)	Total Error Summation (in mV)	Total Error Summation as a % of the Ideal Output
100:1 INPUT RANGE	10	10	10	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
Total Error = ±% rdg ±Output V_{OS}	10	0.1	0.1	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	1	1	1	1	0.5 (AD) 0.25 (BD)	10 (AD) 5 (BD)	10.5 (AD) 5.25 (BD)	1.05 (AD) 0.5 (BD)
	0.1	0.1	0.1	0.1	0.5 (AD) 0.25 (BD)	1 (AD) 0.5 (BD)	1.5 (AD) 0.75 (BD)	1.5 (AD) 0.75 (BD)
WIDE DYNAMIC RANGE	1	0.10	0.01	10	28 (AD) 16.75 (BD)	200 (AD) 100 (BD)	228 (AD) 116.75 (BD)	2.28 (AD) 1.17 (BD)
Total Error = ±% rdg ±Output V_{OS} ±Input $V_{OS} \times (V_Y + V_Z)/V_X$	10	0.05	2	0.25	1.76 (AD) 1 (BD)	5 (AD) 2.5 (BD)	6.76 (AD) 3.5 (BD)	2.7 (AD) 1.4 (BD)
	5	0.01	0.01	5	125.75 (AD) 75.4 (BD)	100 (AD) 50 (BD)	225.75 (AD) 125.4 (BD)	4.52 (AD) 2.51 (BD)
	10	0.01	0.1	1	25.53 (AD) 15.27 (BD)	20 (AD) 10 (BD)	45.53 (AD) 25.27 (BD)	4.55 (AD) 2.53 (BD)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 250 mW
Output Short Circuit-to-Ground . . . . . Indefinite
Input Voltages V_X, V_Y, V_Z . . . . . $(+V_S - 1\ V)$, –1 V
Input Currents I_X, I_Y, I_Z, I_O . . . . . 1 mA
Operating Temperature Range . . . . . –25°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Storage . . . . . 60 sec, +300°C
Thermal Resistance
θ_{JC} . . . . . 35°C/W
θ_{JA} . . . . . 120°C/W

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD538AD	–25°C to +85°C	Side-Brazed Ceramic DIP	D-18
AD538BD	–25°C to +85°C	Side-Brazed Ceramic DIP	D-18
AD538ACHIPS	–25°C to +85°C	Chips	
AD538SD	–55°C to +125°C	Side-Brazed Ceramic DIP	D-18
AD538SD/883B	–55°C to +125°C	Side-Brazed Ceramic DIP	D-18

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD538 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

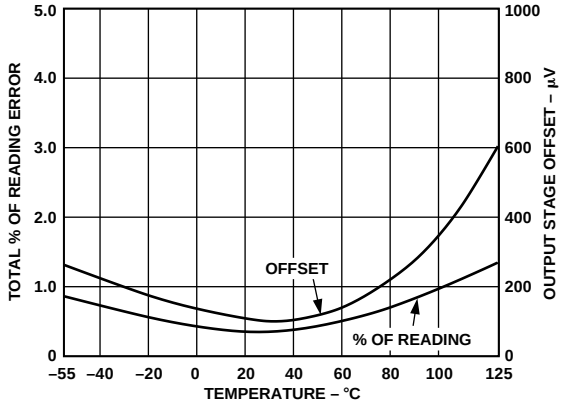


Figure 1. Multiplier Error vs. Temperature (100 mV < V_X, V_Y, $V_Z \leq$ 10 V)

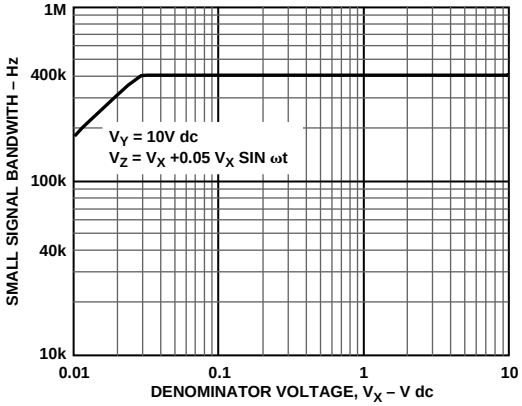


Figure 4. Small Signal Bandwidth vs. Denominator Voltage (One-Quadrant Mult/Div)

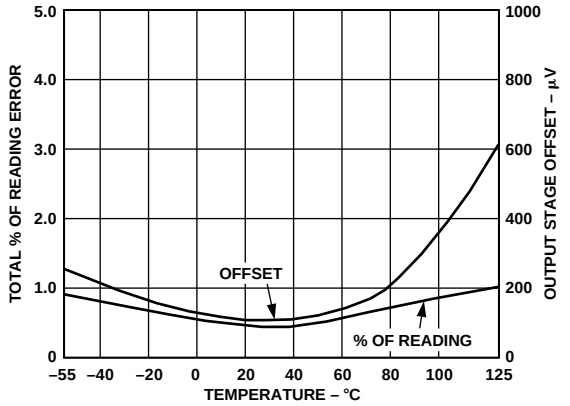


Figure 2. Divider Error vs. Temperature (100 mV < V_X, V_Y, $V_Z \leq$ 10 V)

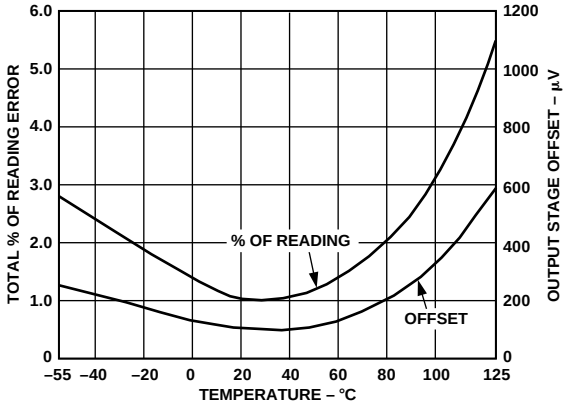


Figure 5. Multiplier Error vs. Temperature (10 mV < V_X, V_Y, $V_Z \leq$ 100 mV)

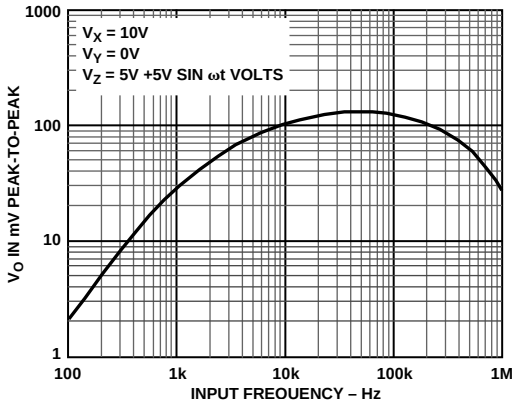


Figure 3. V_Z Feedthrough vs. Frequency

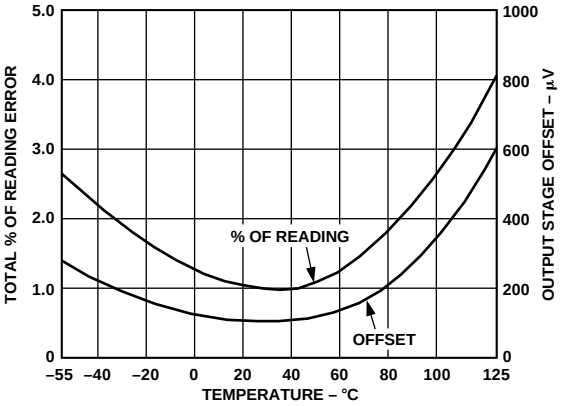


Figure 6. Divider Error vs. Temperature (10 mV < V_X, V_Y, $V_Z \leq$ 100 mV)

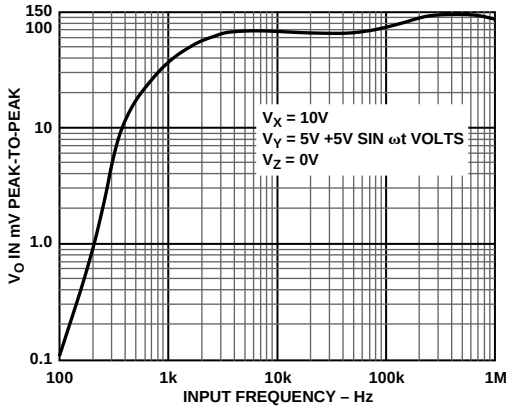


Figure 7. V_Y Feedthrough vs. Frequency

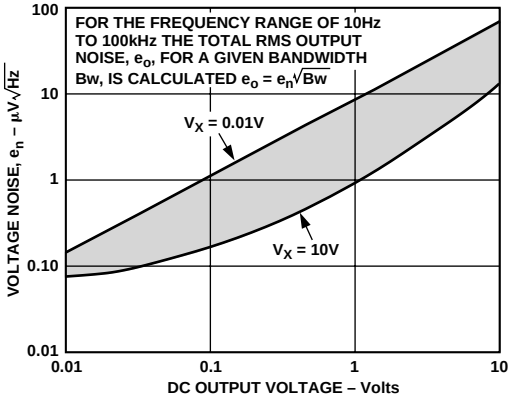


Figure 8. 1 kHz Output Noise Spectral Density vs. DC Output Voltage

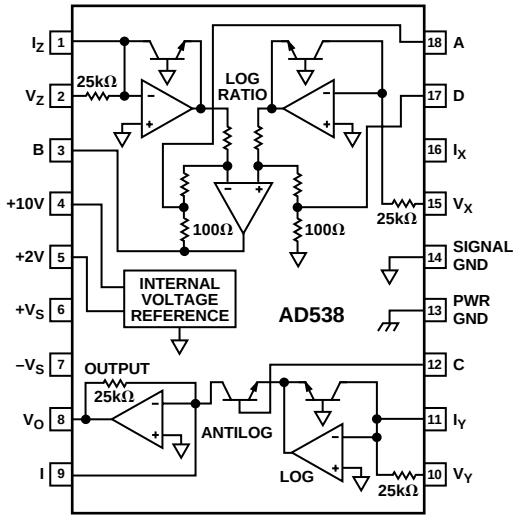


Figure 9. Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figures 9 and 10, the V_Z and V_X inputs connect directly to the AD538's input log ratio amplifiers. This subsection provides an output voltage proportional to the natural log of input voltage V_Z, minus the natural log of input voltage V_X. The output of the log ratio subsection at B can be expressed by the transfer function:

$$V_B = \frac{kT}{q} ln\left(\frac{V_Z}{V_X}\right)$$

where $k = 1.3806 \times 10^{-23}$ J/K,
$q = 1.60219 \times 10^{-19}$ C,
T is in Kelvins.

The log ratio configuration may be used alone, if correctly temperature compensated and scaled to the desired output level (see Applications section).

Under normal operation, the log-ratio output will be directly connected to a second functional block at input C, the antilog subsection. This section performs the antilog according to the transfer function:

$$V_O = V_Y e^{\left(V_C \frac{q}{kT}\right)}$$

As with the log-ratio circuit included in the AD538, the user may use the antilog subsection by itself. When both subsections are combined, the output at B is tied to C, the transfer function of the AD538 computational unit is:

$$V_O = V_Y e^{\left[\left(\frac{kT}{q}\right)\left(\frac{q}{kT}\right) ln\left(\frac{V_Z}{V_X}\right)\right]}; V_B = V_C$$

which reduces to:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)$$

Finally, by increasing the gain, or attenuating the output of the log ratio subsection via resistor programming, it is possible to raise the quantity V_Z/V_X to the m^{th} power. Without external programming, m is unity. Thus the overall AD538 transfer function equals:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$$

where $0.2 < m < 5$.

When the AD538 is used as an analog divider, the V_Y input can be used to multiply the ratio V_Z/V_X by a convenient scale factor. The actual multiplication by the V_Y input signal is accomplished by adding the log of the V_Y input signal to the signal at C, which is already in the log domain.

STABILITY PRECAUTIONS

At higher frequencies, the multistaged signal path of the AD538, as illustrated in Figure 10, can result in large phase shifts. If a condition of high incremental gain exists along that path (e.g., $V_O = V_Y \times V_Z/V_X = 10\ V \times 10\ mV/10\ mV = 10\ V$ so that $\Delta V_O/\Delta V_X = 1000$), then small amounts of capacitive feedback from V_O to the current inputs I_Z or I_X can result in instability. Appropriate care should be exercised in board layout to prevent capacitive feedback mechanisms under these conditions.

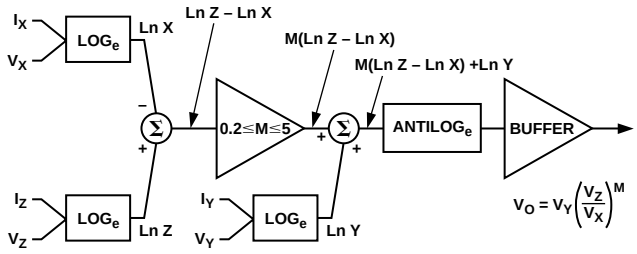


Figure 10. Model Circuit

USING THE VOLTAGE REFERENCES

A stable bandgap voltage reference for scaling is included in the AD538. It is laser-trimmed to provide a selectable voltage output of +10 V buffered (Pin 4), +2 V unbuffered (Pin 5) or any voltages between +2 V and +10.2 V buffered as shown in Figure 11. The output impedance at Pin 5 is approximately 5 kΩ. Note that any loading of this pin will produce an error in the +10 V reference voltage. External loads on the +2 V output should be greater than 500 kΩ to maintain errors less than 1%.

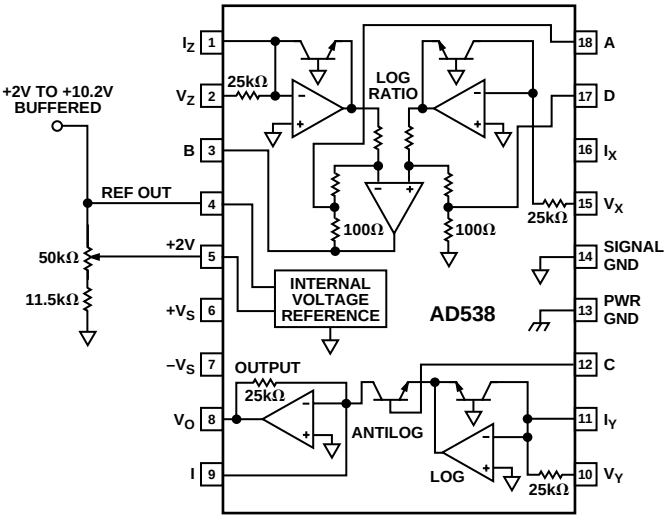


Figure 11. +2 V to +10.2 V Adjustable Reference

In situations not requiring both reference levels, the +2 V output can be converted to a buffered output by tying Pins 4 and 5 together. If both references are required simultaneously, the +10 V output should be used directly and the +2 V output should be externally buffered.

ONE-QUADRANT MULTIPLICATION/DIVISION

Figure 12 shows how the AD538 may be easily configured as a precision one-quadrant multiplier/divider. The transfer function $V_{OUT} = V_Y (V_Z/V_X)$ allows "three" independent input variables, a calculation not available with a conventional multiplier. In addition, the 1000:1 (i.e., 10 mV to 10 V) input dynamic range of the AD538 greatly exceeds that of analog multipliers computing one-quadrant multiplication and division.

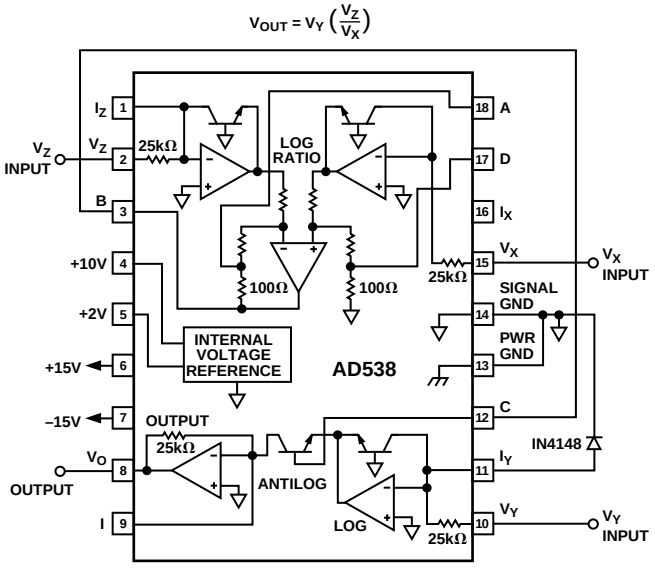


Figure 12. One-Quadrant Combination Multiplier/Divider

By simply connecting the input V_X (Pin 15) to the +10 V reference (Pin 4), and tying the log-ratio output at B to the antilog input at C, the AD538 can be configured as a one-quadrant analog multiplier with 10-volt scaling. If 2-volt scaling is desired, V_X can be tied to the +2 V reference.

When the input V_X is tied to the +10 V reference terminal, the multiplier transfer function becomes:

$$V_O = V_Y \left(\frac{V_Z}{10\ V} \right)$$

As a multiplier, this circuit provides a typical bandwidth of 400 kHz with values of V_X, V_Y or V_Z varying over a 100:1 range (i.e., 100 mV to 10 V). The maximum error with a 100 mV to 10 V range for the two input variables will typically be +0.5% of reading. Using the optional Z offset trim scheme, as shown in Figure 13, this error can be reduced to +0.25% of reading.

By using the +10 V reference as the V_Y input, the circuit of Figure 12 is configured as a one-quadrant divider with a fixed scale factor. As with the one-quadrant multiplier, the inputs accept only single (positive) polarity signals. The output of the one-quadrant divider with a +10 V scale factor is:

$$V_O = 10V \left(\frac{V_Z}{V_X} \right)$$

The typical bandwidth of this circuit is 370 kHz with 1 V to 10 V denominator input levels. At lower amplitudes, the bandwidth gradually decreases to approximately 200 kHz at the 2 mV input level.

TWO-QUADRANT DIVISION

The two-quadrant linear divider circuit illustrated in Figure 13 uses the same basic connections as the one-quadrant version. However, in this circuit the numerator has been offset in the positive direction by adding the denominator input voltage to it. The offsetting scheme changes the divider's transfer function from:

$$V_O = 10V\left(\frac{V_Z}{V_X}\right)$$

to:

$$V_O = 10V\,\frac{\left(V_Z + AV_X\right)}{V_X} = 10\,V\left(1\,A + \frac{V_Z}{V_X}\right)$$

$$= 10\,A + 10\,V\left(\frac{V_Z}{V_X}\right)$$

where $A = \left(\frac{35\,k\Omega}{25\,k\Omega}\right)$

As long as the magnitude of the denominator input is equal to or greater than the magnitude of the numerator input, the circuit will accept bipolar numerator voltages. However, under the conditions of a 0 V numerator input, the output would incorrectly equal +14 V. The offset can be removed by connecting the +10 V reference through resistors R1 and R2 to the output section's summing node I at Pin 9 thus providing a gain of 1.4 at the center of the trimming potentiometer. The pot R2 adjusts out or corrects this offset, leaving the desired transfer function of 10 V (V_Z/V_X).

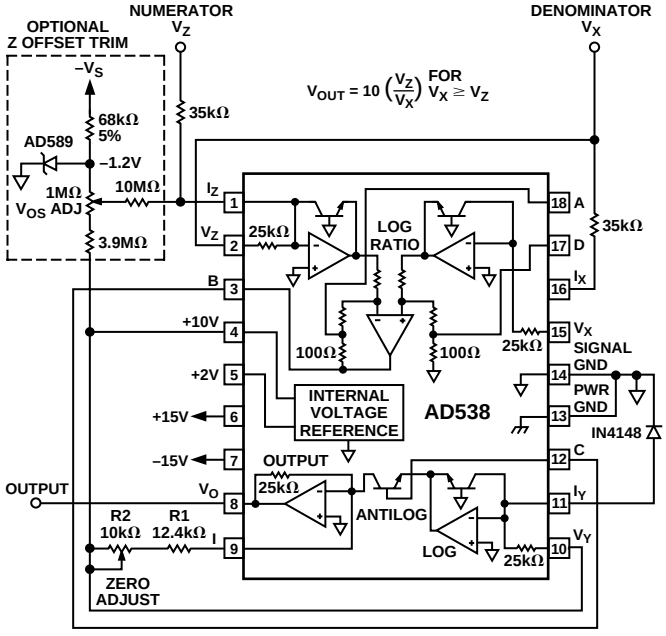


Figure 13. Two-Quadrant Division with 10 V Scaling

LOG RATIO OPERATION

Figure 14 shows the AD538 configured for computing the log of the ratio of two input voltages (or currents). The output signal from B is connected to the summing junction of the output amplifier via two series resistors. The 90.9 Ω metal film resistor effectively degrades the temperature coefficient of the ±3500 ppm/°C resistor to produce a 1.09 kΩ +3300 ppm/°C equivalent value. In this configuration, the V_Y input must be tied to some voltage less than zero (–1.2 V in this case) removing this input from the transfer function.

The 5 kΩ potentiometer controls the circuit's scale factor adjustment providing a +1 V per decade adjustment. The output offset potentiometer should be set to provide a zero output with $V_X = V_Z = 1$ V. The input V_Z adjustment should be set for an output of 3 V with $V_Z = 1$ mV and $V_X = 1$ V.

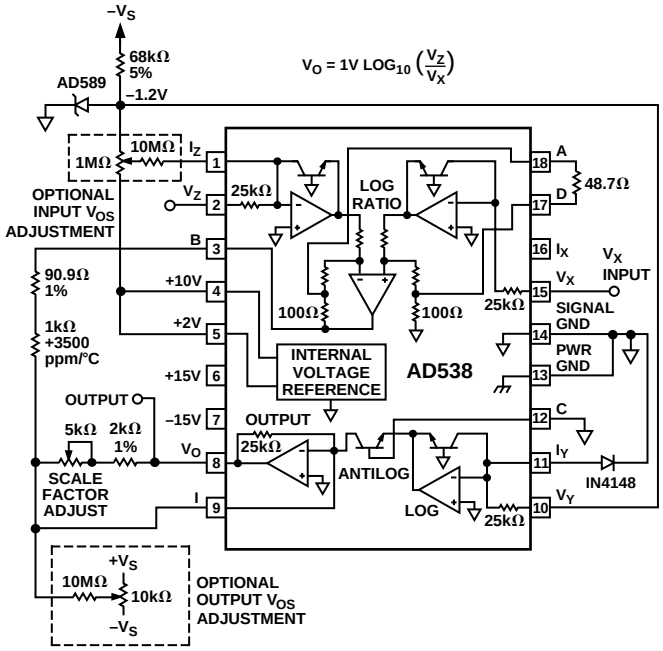


Figure 14. Log Ratio Circuit

The log ratio circuit shown achieves ±0.5% accuracy in the log domain for input voltages within three decades of input range: 10 mV to 10 V. This error is not defined as a percent of full-scale output, but as a percent of input. For example, using a 1 V/decade scale factor, a 1% error in the positive direction at the INPUT of the log ratio amplifier translates into a 4.3 mV deviation from the ideal OUTPUT (i.e., 1 V × $\log_{10}$ (1.01) = 4.3214 mV). An input error 1% in the negative direction is slightly different, giving an output deviation of 4.3648 mV.

ANALOG COMPUTATION OF POWERS AND ROOTS

It is often necessary to raise the quotient of two input signals to a power or take a root. This could be squaring, cubing, square-rooting or exponentiation to some noninteger power. Examples include power series generation. With the AD538, only one or two external resistors are required to set ANY desired power, over the range of 0.2 to 5. Raising the basic quantity V_Z/V_X to a power greater than one requires that the gain of the AD538's log ratio subtractor be increased, via an external resistor between pins A and D. Similarly, a voltage divider that attenuates the log ratio output between points B and C will program the power to a value less than one.

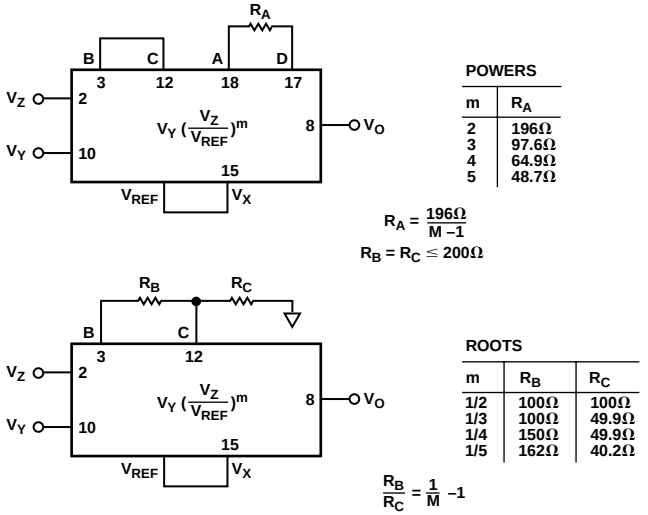


Figure 15. Basic Configurations and Transfer Functions for the AD538

SQUARE ROOT OPERATION

The explicit square root circuit of Figure 16 illustrates a precise method for performing a real-time square root computation. For added flexibility and accuracy, this circuit has a scale factor adjustment.

The actual square rooting operation is performed in this circuit by raising the quantity V_Z/V_X to the one-half power via the resistor divider network consisting of resistors R_B and R_C. For maximum linearity, the two resistors should be 1% (or better) ratio-matched metal film types.

One volt scaling is achieved by dividing-down the 2 V reference and applying approximately 1 V to both the V_Y and V_X inputs. In this circuit, the V_X input is intentionally set low, to about 0.95 V, so that the V_Y input can be adjusted high, permitting a ±5% scale factor trim. Using this trim scheme, the output voltage will be within ±3 mV ± 0.2% of the ideal value over a 10 V to 1 mV input range (80 dB). For a decreased input dynamic range of 10 mV to 10 V (60 dB) the error is even less; here the output will be within ±2 mV ± 0.2% of the ideal value. The bandwidth of the AD538 square root circuit is approximately 280 kHz with a 1 V p-p sine wave with a +2 V dc offset.

This basic circuit may also be used to compute the cube, fourth or fifth roots of an input waveform. All that is required for a given root is that the correct ratio of resistors, R_C and R_B, be selected such that their sum is between 150 Ω and 200 Ω.

The optional absolute value circuit shown preceding the AD538 allows the use of bipolar input voltages. Only one op amp is required for the absolute value function because the I_Z input of the AD538 functions as a summing junction. If it is necessary to preserve the sign of the input voltage, the polarity of the op amp output may be sensed and used after the computation to switch the sign bit of a D.V.M. chip.

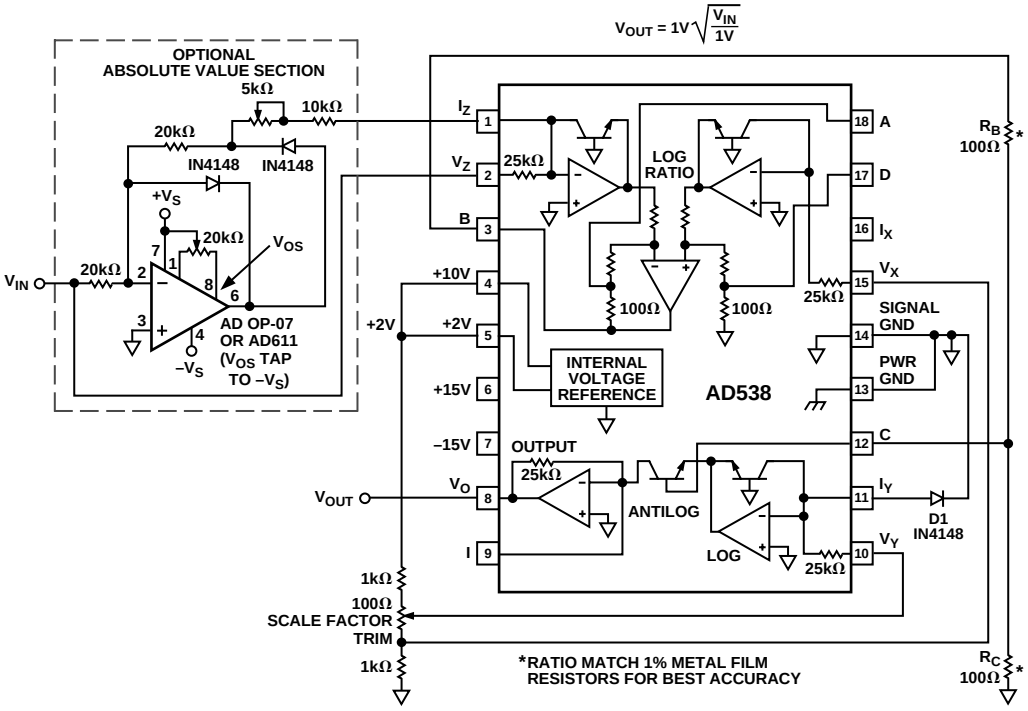


Figure 16. Square Root Circuit

TRANSDUCER LINEARIZATION

Many electronic transducers used in scientific, commercial or industrial equipment monitor the physical properties of a device and/or its environment. Sensing (and perhaps compensating for) changes in pressure, temperature, moisture or other physical phenomenon can be an expensive undertaking, particularly where high accuracy and very low nonlinearity are important. In conventional analog systems accuracy may be easily increased by offset and scale factor trims, however, nonlinearity is usually the absolute limitation of the sensing device.

With the ability to easily program a complex analog function, the AD538 can effectively compensate for the nonlinearities of an inexpensive transducer. The AD538 can be connected between the transducer preamplifier output and the next stage of monitoring or transmitting circuitry. The recommended procedure for linearizing a particular transducer is first to find the closest function which best approximates the nonlinearity of the device and then, to select the appropriate exponent resistor value(s).

ARC-TANGENT APPROXIMATION

The circuit of Figure 17 is typical of those AD538 applications where the quantity V_Z/V_X is raised to powers greater than one. In an approximate arc-tangent function, the AD538 will accurately compute the angle that is defined by X and Y displacements represented by input voltages V_X and V_Z. With accuracy to within one degree (for input voltages between 100 µV and 10 volts), the AD538 arc-tangent circuit is more precise than conventional analog circuits and is faster than most digital techniques. For a direct arc-tangent computation that requires fewer external components, refer to the AD639 data sheet. The circuit shown is set up for the transfer function:

$$V_\theta = \left(V_{\theta REF} - V_\theta\right)\left[\frac{\left(V_Z\right)}{\left(V_X\right)}\right]^{1.21}$$

where:

$$\theta = Tan^{-1}\left(\frac{Z}{X}\right)$$

The $(V_{\theta REF} - V_\theta)$ function is implemented in this circuit by adding together the output, V_θ, and an externally applied reference voltage, $V_{\theta REF}$, via an external AD547 op amp. The 1 µF capacitor connected around the AD547's 100 kΩ feedback resistor frequency compensates the loop (formed by the amplifier between V_θ and V_Y).

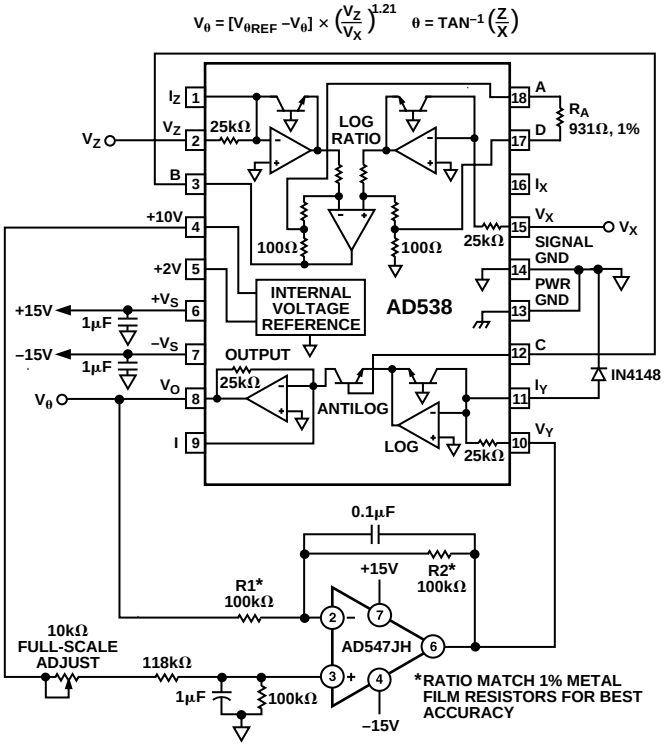


Figure 17. The Arc-Tangent Function

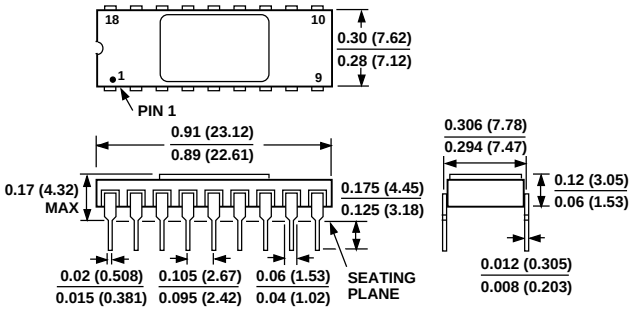
The V_B/V_A quantity is calculated in the same manner as in the one-quadrant divider circuit, except that the resulting quotient is raised to the 1.21 power. Resistor R_A (nominally 931 Ω) sets the power or *m* factor.

For the highest arc-tangent accuracy the external resistors R1 and R2 should be ratio matched; however, the offset trim scheme shown in other circuits is not required since nonlinearity effects are the predominant source of error. Also note that instability will occur as the output approaches 90° because, by definition, the arc-tangent function is infinite and therefore, the AD538's gain will be extremely high.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Side-Brazed Ceramic DIP
(D-18)



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