
YAMAHA® LSI

YM2151

FM Operator Type-M(OPM)

■ OUTLINE

The YM2151 is an FM-type sound generator equipped with an 8 bit bus line and capable of producing superb audio quality via a microprocessor program. When this IC is used in tandem with the specially-developed YM3012D/A converter, you can obtain 8-note, left-right/2-channel audio signals.

In addition, this unit is equipped with noise, vibrato, an amplitude modulation circuit, a sound effects circuit, and timer.

The package is a 24-pin dual in-line package.

■ FEATURES

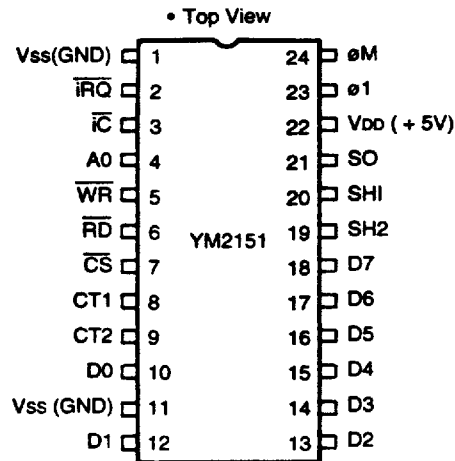
- Generate up to 8 notes.
- Generate noise.
- Timbre can be altered temporally.
- High harmonic can be de-harmonized from the base frequency.
- De-harmonize between octaves.
- Interval setting of up to 1.6 cents.
- Add vibrato and amplitude modulation.
- Generate a variety of sound effects by extreme de-harmonization of the high harmonic from the base frequency and massive vibrato and amplitude modulation.

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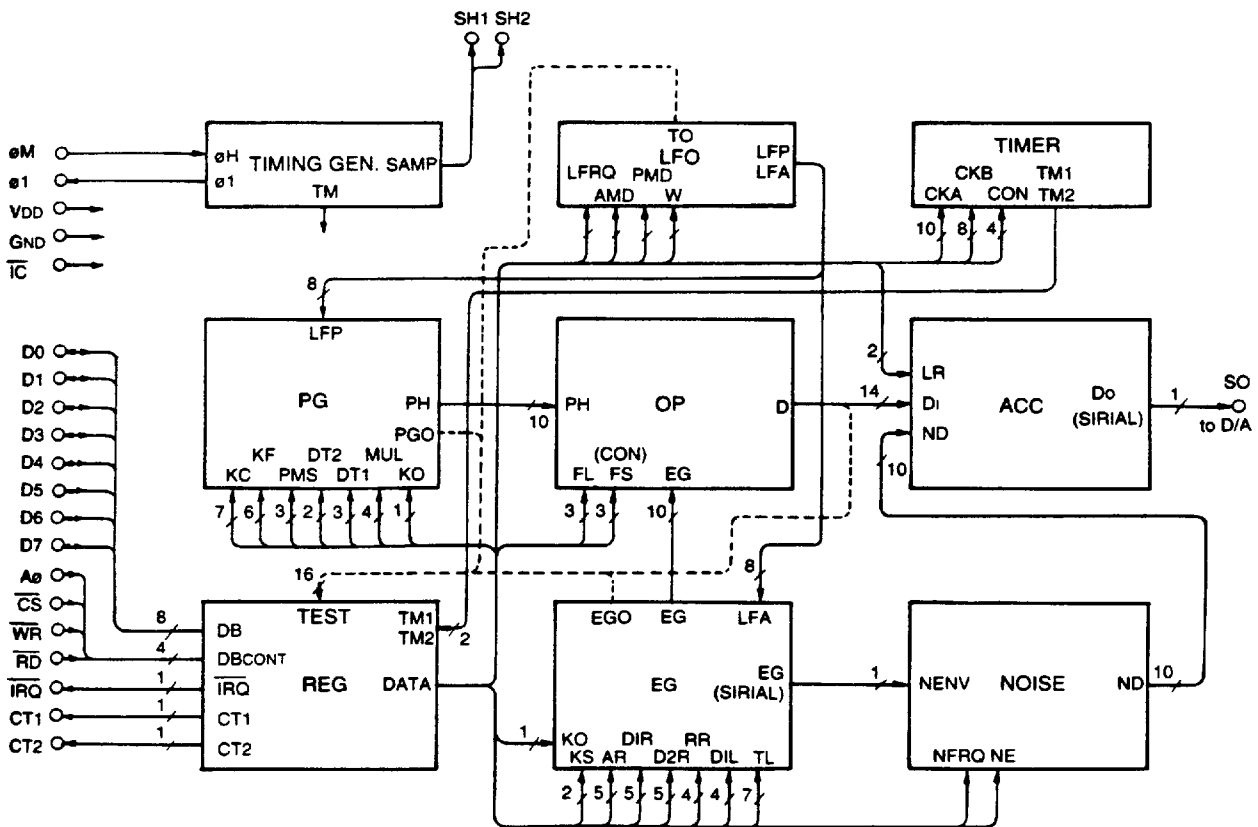
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YM2151 CATALOG
CATALOG No.:LSI-2121512
1991. 12

■ TERMINAL DIAGRAM



■ BLOCK DIAGRAM



■ DESCRIPTION OF TERMINAL FUNCTION

- **D₀ ~ D₇: Address/Data Bus (input/output high impedance)**
A multiplex bus that can be used for both address and data; inputs an 8-bit parallel signal between an external device and the internal register.
- **A0: Address/Data Select (Input)**
When A0 = "0", the D₀ ~ D₇ signal is process as address signal; when A0 = "1", the D₀ ~ D₇ signal is processed as data.
- **$\overline{\text{WR}}$: Write (Input)**
When $\overline{\text{WR}}$ = "0", the signals in the bus can be entered.
- **$\overline{\text{RD}}$: Read (Input)**
When $\overline{\text{RD}}$ = "0", the internal signals can be read out via the bus.
- **$\overline{\text{CS}}$: Chip Select (Input)**
When there is a chip select signal, the A0, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ signals become operative and the D₀ ~ D₇ bus data can be entered in the internal register or internal data can be read out on the D₀ ~ D₇ bus.
- **$\overline{\text{IC}}$: Initial clear (Input)**
Internal registers and circuits are initialized when this terminal reads "0".
- **$\overline{\text{iRQ}}$: Interrupt request (Output: Open drain)**
If either of the 2 types of timer counters begins a carry out, this signal will read out a "0" level and request an interrupt from the CPU. Then, with the CPU's readout of the data, the unit will determine from which timer the interrupt request has been made and will process the interrupt.
- **CT1, CT2: Control 1, Control 2 (Output)**
This is the terminal that is used to control an external device and should read "0" level when at initial condition.
- **SO: Serial Output (Output)**
Takes the tone signal divided between the 2 left and right channels, outputs it as serial data, and sends it to the YM3012 D/A converterter specially developed for use with the YM2151.
- **SH1, SH2: Sample and hold**
Used to pick up the serial data supplied to the YM3012 D/A converter, and for sampling hold after analog conversion.
- **ϕM : System clock (Input)**
Inputs the clock ϕM that drives the YM2151, which is internally broken down to and used at 1/2 the frequency. The ϕM is the reference for the tone signal.
- **ϕ1 : Clock for D/A (output)**
This clock drives the D/A and operates at the same frequency as the clock inside the YM2151. Also, when the ϕ1 level shifts from "1" to "0", the $\overline{\text{iRQ}}$, CT1, CT2, TO, SH1, SH2, and SO signals all change.
- **V_{DD}: Power Supply (Input)**
Normally supplies at + 5V.
- **V_{SS}: Grand (Input)**
Conects the system grand.

***WRITE DATA**

Address Map (1); WRITE MODE

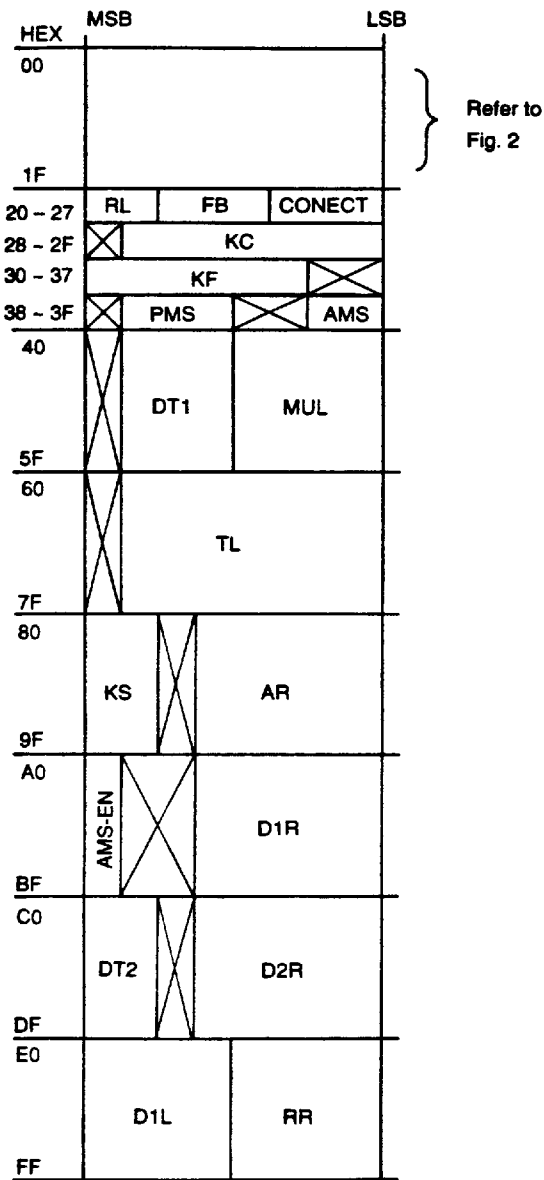
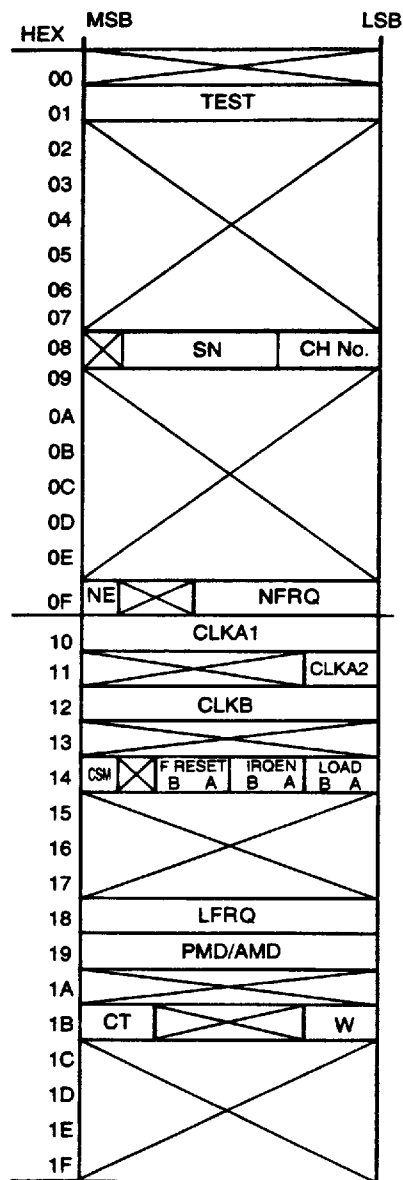


Fig (1)

Address Map (2); WRITE MODE



*F RESET = FLAG RESET

Fig (2)

Address Map (3); READ MODE

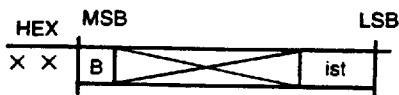
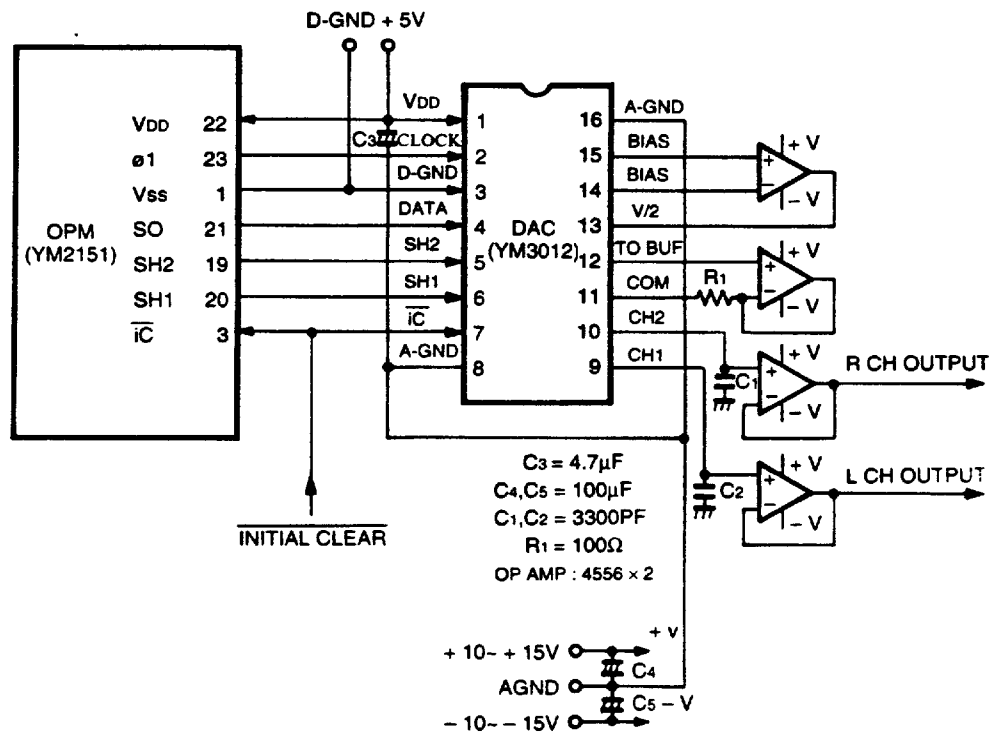


Fig (3)

■ EXAMPLE OF BASIC CIRCUIT



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

ITEM	RATING	UNIT
Voltage Range	- 0.3 - + 7	V
Operating temperature	0 - 70	$^{\circ}\text{C}$
Storage temperature	- 50 - + 125	$^{\circ}\text{C}$

2. Recommended Operation Conditions

ITEM	SYMBOL	MIN.	STD.	MAX.	UNIT
Operating supply voltage	V_{DD}	4.75		5.25	V
Power supply current	I_{DD}			120	mA
Power dispersion (at $V_{DD} = 5.25\text{V}$)	P_D			630	mW

Electrical Characteristics

1. Clock

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Voltage level	"0"		- 0.3		0.8	V
Voltage level	"1"		20		V _{DD}	V
Rise time	T _r	Fig-1			50	ns
Fall time	T _f	Fig-1			50	ns
ON time	T _{ON}	Fig-1	100			ns
Frequency	øM		3.0	3.58	4.0	MHz
Input capacitance	CøM				10	pF

2. ø1

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Rise time	T _{r1}	Fig-3			180	ns
Fall time	T _{f1}	Fig-3			120	ns
Load capacitance	CL				100	pF

3. $\overline{\text{IRQ}}$, CT1, CT2, SO, SH1, SH2

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Rise time	T _{r2}	Fig-4			250	ns
Fall time	T _{f2}	Fig-4			250	ns
Load capacitance	CL				100	pF

4. Write/Read Timing

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Address Set-up Timing	T _{AS}	Fig-2	10			ns
Address Hold Timing	T _{AH}	Fig-2	10			ns
$\overline{\text{CS}}$ WRITE WIDTH	T _{CW}	Fig-2	100			ns
$\overline{\text{WR}}$ WRITE WIDTH	T _{WW}	Fig-2-1	100			ns
WRITE DATA Set-up Time	T _{DS}	Fig-2-1	50			ns
WRITE DATA Hold Time	T _{DHW}	Fig-2-1	10			ns
READ DATA ACCESS Time	T _{ACC}	Fig-2-2			180	ns
READ DATA Hold Time	T _{DHR}	Fig-2-2	10			ns

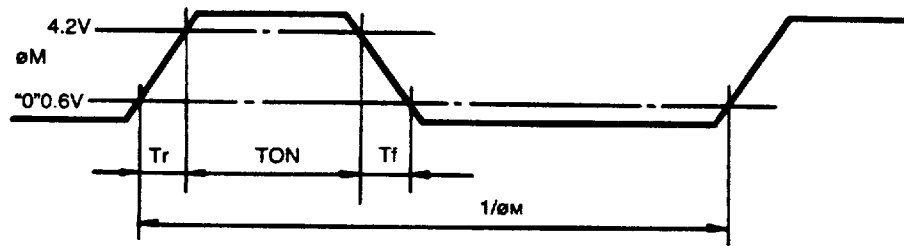


Fig-1 PHASE DATA

5. All Input

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Voltage level	"0"		-0.3		0.8	V
Voltage level	"1"		2.0		V _{DD}	V

6. All Output

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Voltage level	"0"		-0.3		0.4	V
Voltage level	"1"		2.4		V _{DD}	V

7. A0, \overline{WR} , \overline{RD} , \overline{CS} , ϕM

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Input Leak Current	I_L	at 25°C $V_i = 10V$			0.1	μA

8. \overline{IC}

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Input Current	I_{i0}	$V_{DD} = 5V$	10		60	μA

9. \overline{IRQ}^* , CT1, CT2, D0-D7, SH1 SH2, SO, $\phi 1$

ITEM	SYMBOL	CONDISIONS	MIN.	STD.	MAX.	UNIT
Load Current	I_D	$V_{Lo} = 0.4V$			2.1	mA

*OPEN DRAIN

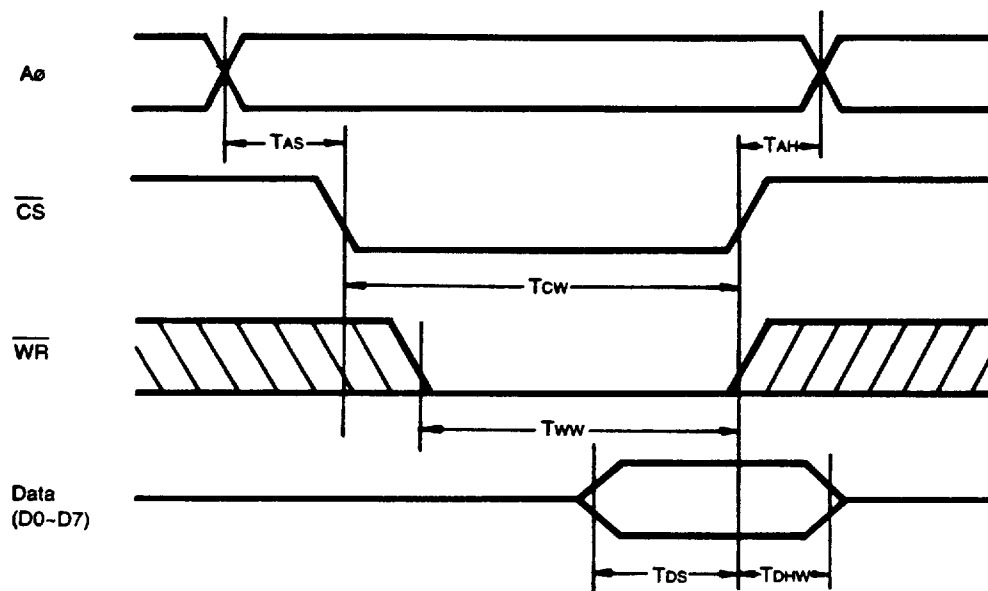


Fig 2-1 WRITE TIING

NOTE: T_{DS} and T_{DHW} use as a reference either \overline{CS} or \overline{WR} , whichever has attained High Level.

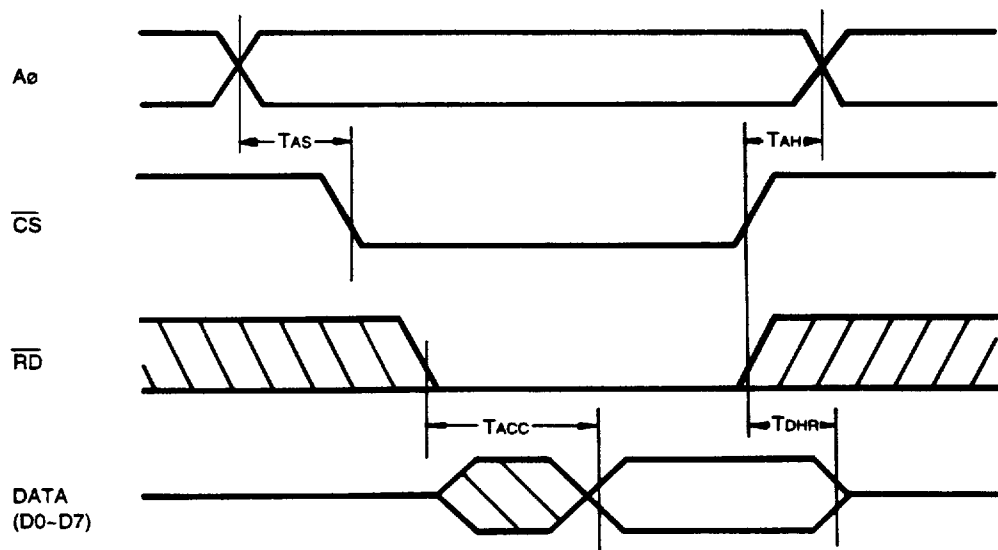


Fig 2-2 READ TIMING

NOTE: T_{ACC} use as a reference either \overline{CS} or \overline{RD} , whichever is the last to attain Low Level. T_{DHR} uses as a reference either \overline{CS} or \overline{RD} , whichever has attained High Level.

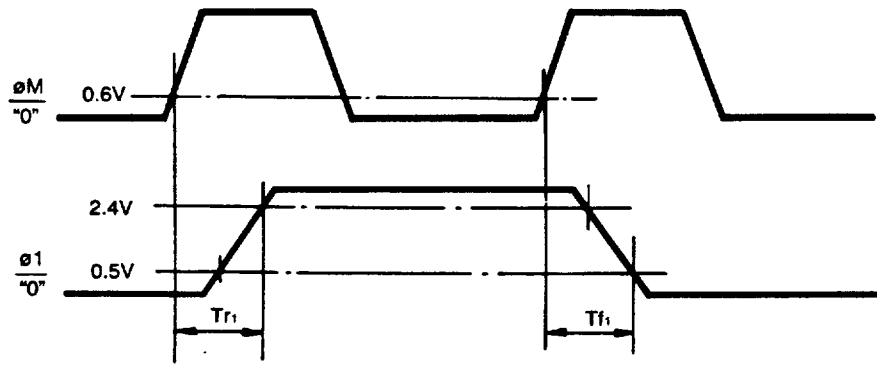


Fig-3

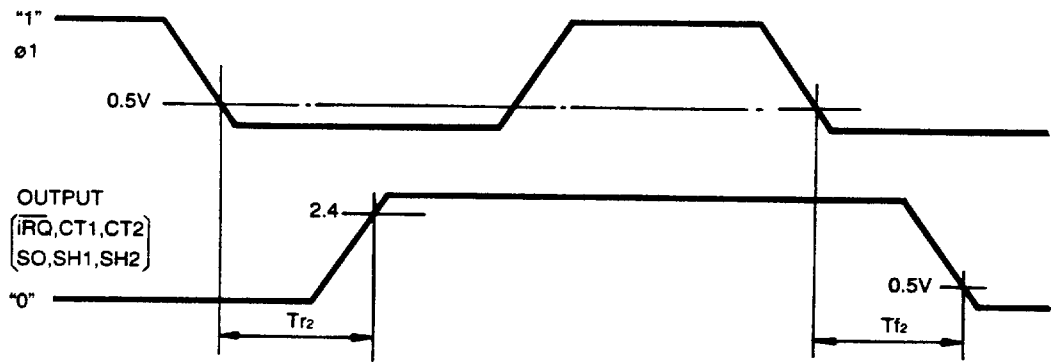


Fig-4

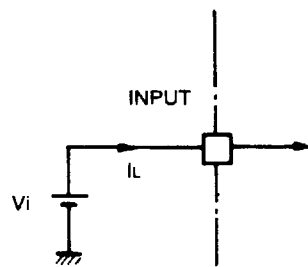


Fig-5

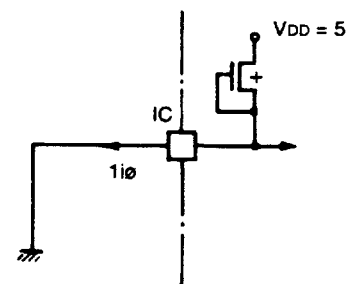


Fig-6

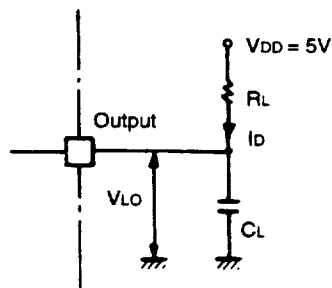
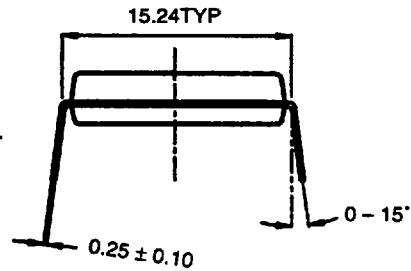
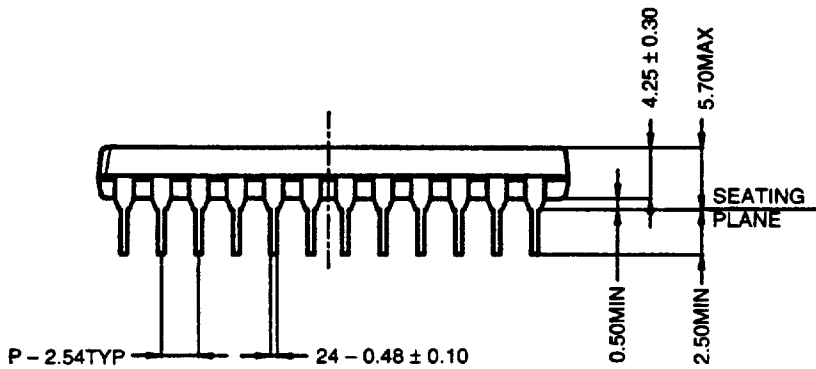
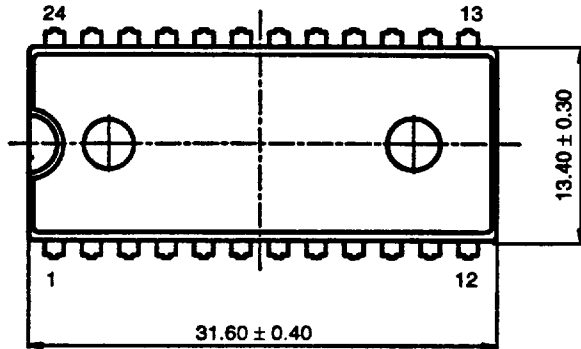


Fig-7

EXTERNAL DIMENSIONS



UNIT : mm (millimeters)

The specifications of this product are subject to improvement changes without prior notice.

_____ AGENCY _____

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