CMOS 4-BIT MICROCONTROLLER

TMP47C210AN, TMP47C410AN
TMP47C210AF, TMP47C410AF

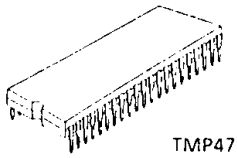
The 47C210A/410A have high breakdown voltage outputs based on the TLCS-47 CMOS series.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C210AN	2048 × 8-bit	128 × 4-bit	SDIP42	TMP47C991E
TMP47C210AF			QFP44	TMP47C991G
TMP47C410AN	4096 × 8-bit	256 × 4-bit	SDIP42	TMP47C991E
TMP47C410AF			QFP44	TMP47C991G

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.9μs (at 4.2 MHz)
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max.
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (36 pins)
  - Input 2 ports 5 pins
  - Output 5 ports 20 pins
  - I/O 3 ports 11 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, and leading/trailing edge mode
- ◆High breakdown voltage outputs
  VFT direct drive capability (max. 42V × 20bits)
- ◆Hold function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM4721A

SDIP42

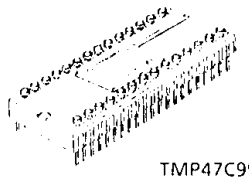


TMP47C210AN
TMP47C410AN

QFP44

TMP47C210AF
TMP47C410AF

SDIC42



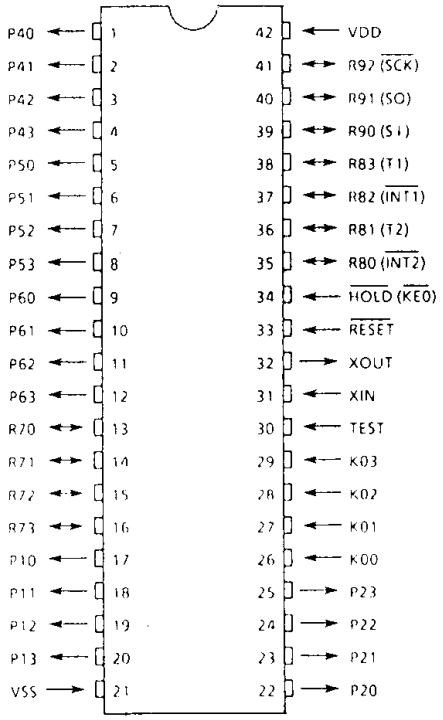
TMP47C991E

QFC44

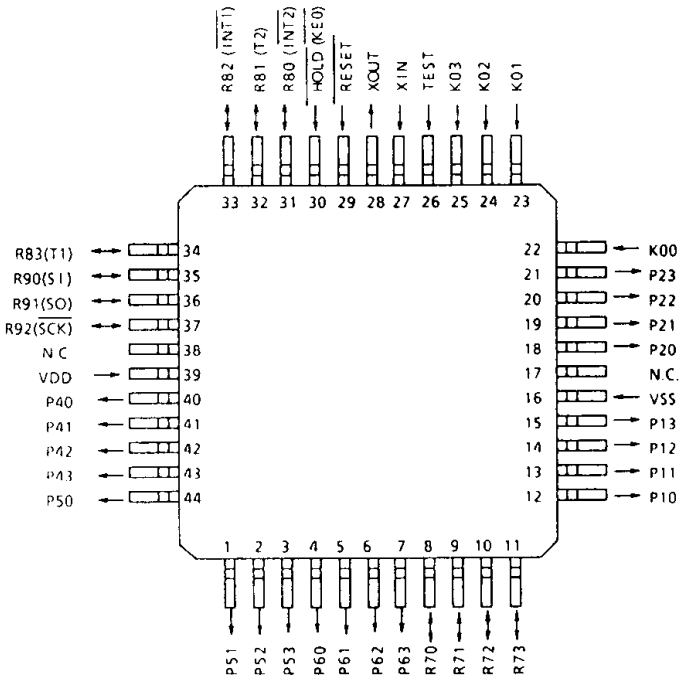
TMP47C991G

PIN ASSIGNMENT (TOP VIEW)

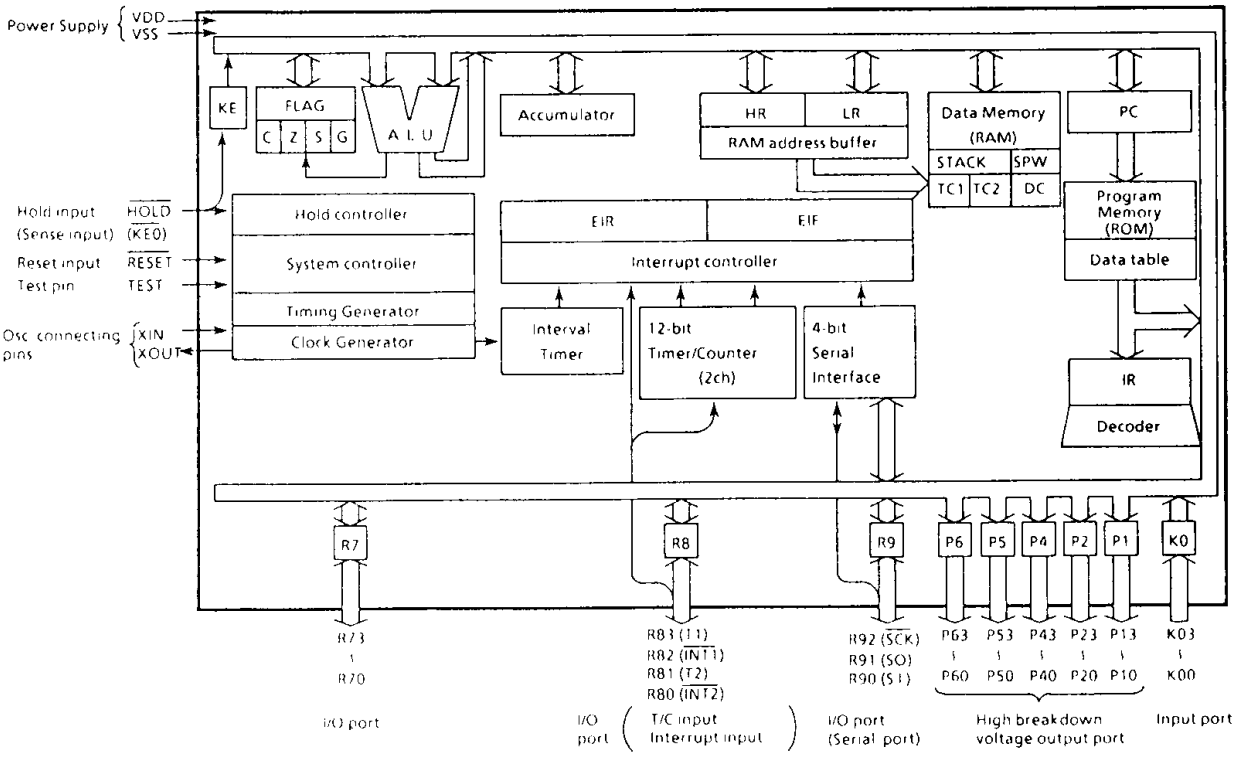
(1) SDIP42



(2) QFP44



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch (High breakdown voltage outputs). 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 - P20			
P43 - P40	Output	4-bit output port with latch (High breakdown voltage outputs)	
P53 - P50			
P63 - P60			
R73 - R70	I/O	4-bit I/O port with latch. When using as input port, the latch must be set to "1"	
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1"	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test, Be opened or fixed to low lovel.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

The 47C210A/410A are the chip with high breakdown voltage outputs for the TLCS-47 CMOS series. As the function and instruction are equivalent to 47C200A/400A except the high breakdown voltage outputs, the technical data sheets for the 47C200A/400A shall also be referred to.

1. I/O PORTS

The 47C210A/410A have I/O ports (36pins) each as follows :

(1) K0	;	4-bit input
(2) P1, P2	;	4-bit output (High breakdown voltage output)
(3) P4, P5, P6	;	4-bit output (High breakdown voltage output)
(4) R7	;	4-bit input/output
(5) R8	;	4-bit input/output (Shared by external intterrupt input and timen/counter input)
(6) R9	;	3-bit input/output (Shared by serial part)
(7) KE	;	1-bit sense input (Shared by hold request/release signal input)

This section describes ports of (2), (3) which are changed from the 47C200A/400A.

Table 1-1 lists the port address assignments and the I/O instructions that can access the ports.

1.1 Ports P1/P2 and Ports P4/P5/P6

These are 4-bit high breakdown voltage output ports with latch capable of directly driving vacuum fluorescent tubes (VFT). The latch data are read when an input instruction is executed. During reset, the latch is initialized to "0".

8-bit data can be output through ports P1 and P2 by using the 5-bit to 8-bit data conversion instruction; therefore, these ports can also be effectively utilized as segment output pins.

Ports P4, P5 and P6 can be set and cleared in 1-bit units using the L-register indirect addressing bit manipulation instruction; therefore, these ports can also be effectively utilized as digit output pins.

Figure 1-2 shows an example of driving a vacuum fluorescent tube 8-segment x 12-digit display.

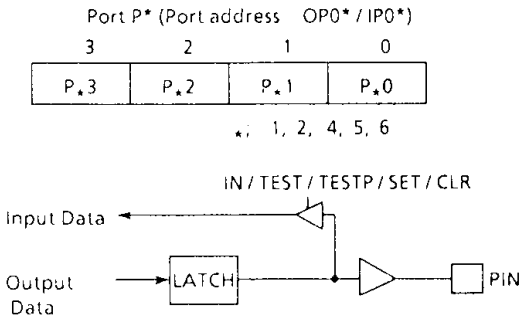


Figure 1-1. Ports P1, P2, P4, P5, P6

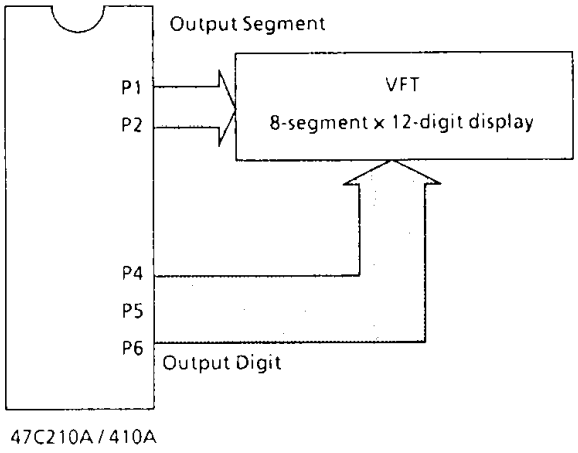


Figure 1-2. Example of driving VFT

port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	-	-	-	-	○	-
01	P1 output latch	P1 output port	○	○	○	○ (Note2)	○	○	-
02	P2 output latch	P2 output port	○	○	○	○	○	○	-
03	——	——	-	-	-	-	-	-	-
04	P4 output latch	P4 output port	○	○	○	-	○	○	○
05	P5 output latch	P5 output port	○	○	○	-	○	○	○
06	P6 output latch	P6 output port	○	○	○	-	○	○	○
07	R7 input port	R7 output port	○	○	○	-	○	○	○
08	R8 input port	R8 output port	○	○	○	-	○	○	-
09	R9 input port	R9 output port	○	○	○	-	○	○	-
0A	——	——	-	-	-	-	-	-	-
0B	——	——	-	-	-	-	-	-	-
0C	——	——	-	-	-	-	-	-	-
0D	——	——	-	-	-	-	-	-	-
0E	SIO, Hold status	——	○	-	-	-	-	○	-
0F	Serial receive buffer	Serial transmit buffer	○	○	○	-	-	-	-
10_H	Undefined	Hold operating mode control	-	○	-	-	-	-	-
11	Undefined	——	-	-	-	-	-	-	-
12	Undefined	——	-	-	-	-	-	-	-
13	Undefined	——	-	-	-	-	-	-	-
14	Undefined	——	-	-	-	-	-	-	-
15	Undefined	——	-	-	-	-	-	-	-
16	Undefined	——	-	-	-	-	-	-	-
17	Undefined	——	-	-	-	-	-	-	-
18	Undefined	——	-	-	-	-	-	-	-
19	Undefined	Interval Timer interrupt control	-	○	-	-	-	-	-
1A	Undefined	——	-	-	-	-	-	-	-
1B	Undefined	——	-	-	-	-	-	-	-
1C	Undefined	Timer/Counter 1 control	-	○	-	-	-	-	-
1D	Undefined	Timer/Counter 2 control	-	○	-	-	-	-	-
1E	Undefined	——	-	-	-	-	-	-	-
1F	Undefined	Serial interface control	-	○	-	-	-	-	-

Note 1. "——" means the reserved state. Unavailable for the user programs.

Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 1-1. Port Address Assignments and Available I/O Instructions

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 10	
	V_{OUT3}	Source open drain pin	− 35 to V_{DD} + 0.5	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	− 2	mA
	I_{OUT2}	Ports P4, P5, P6	− 25	
	I_{OUT3}	Ports R7, R8, R9	3.5	
Output Current (Total)	ΣI_{OUT2}	Ports P4, P5, P6	− 100	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the Hold mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO1}	Port R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
	I_{LO2}	Port P (open drain)	V_{DD} = 5.5V, V_{OUT} = − 32V	−	−	− 2	
Output High Voltage	V_{OH2}	Ports P1, P2	V_{DD} = 4.5V, I_{OH} = − 1.6mA	2.4	−	−	V
	V_{OH3}	Ports P4, P5, P6	V_{DD} = 4.5V, I_{OH} = − 10mA	2.4	−	−	
Output Low Voltage	V_{OL}	Ports R7, R8, R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3V / 0.2V
The K0 port is opened when the pull-up/pull-down resistor is contained.
The voltage applied to the R port within the valid V_{IL} or V_{IH}.

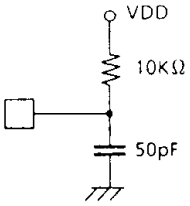
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

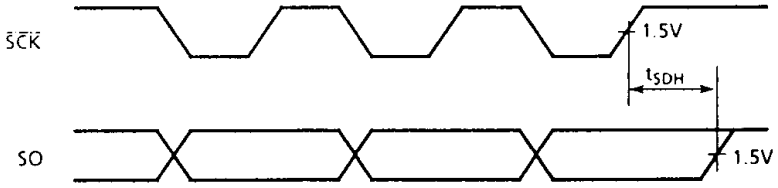
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	–	20	μs
High Level Clock Pulse Width	t_{WCH}	For External Clock Operation	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (complation of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

(1) 4MHz

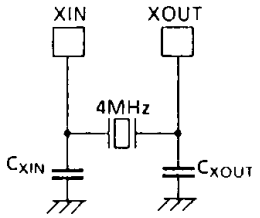
Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

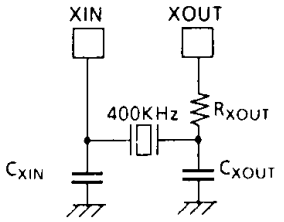


(2) 400KHz

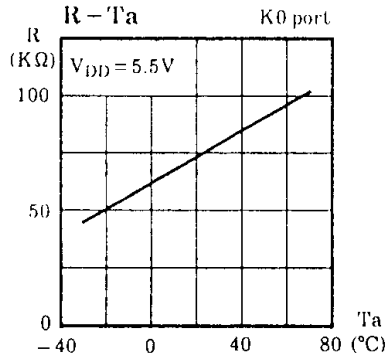
Ceramic Resonator

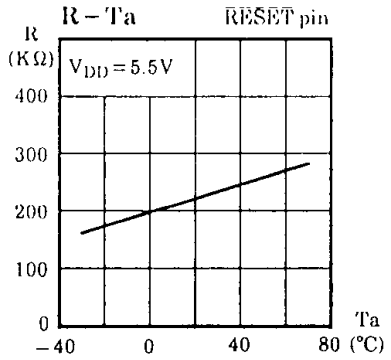
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ

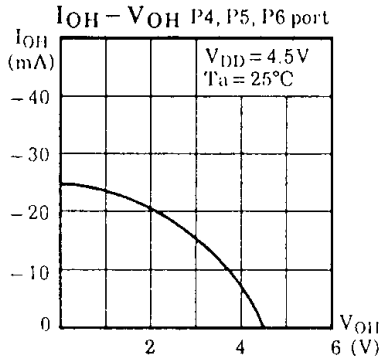
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

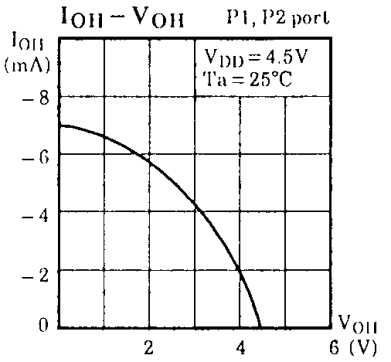


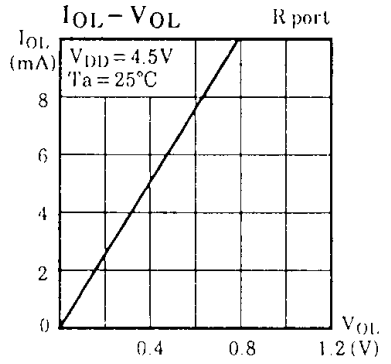
TYPICAL CHARACTERISTICS

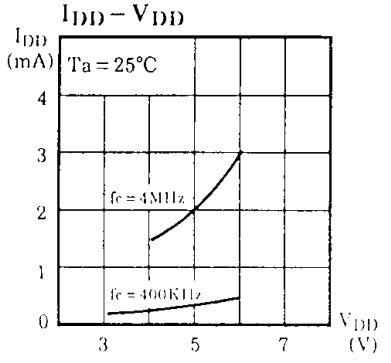


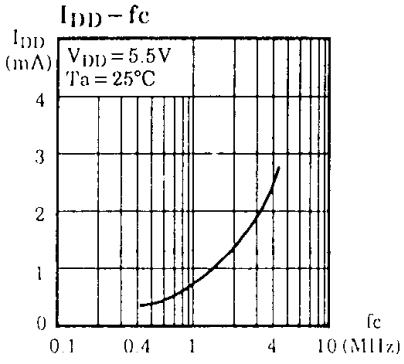








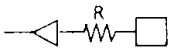
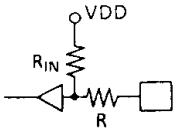
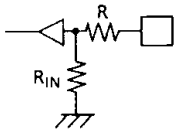
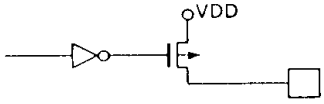
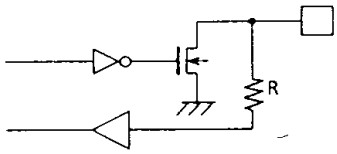
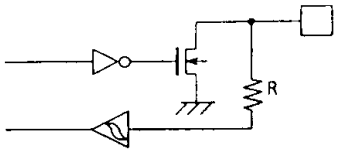




INPUT/OUTPUT/CIRCUITRY

(1) Control pins
The input/output circuitries of the 47C210A/410A control pins are similar to those of the 47C200A/400A.

(2) I/O ports
The input/output circuitries of the 47C210A/410A I/O ports are shown below, any one of the circuitries can be chosen by a code (HA, HB, HC) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		HA	HB	HC	
K0	Input				Pull-up/pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P1 P2 P4 P5 P6	Output				Source open drain Initial "Hi-Z" High breakdown Voltage
R7	I/O				Sink open drain Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O				Sink open drain Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)

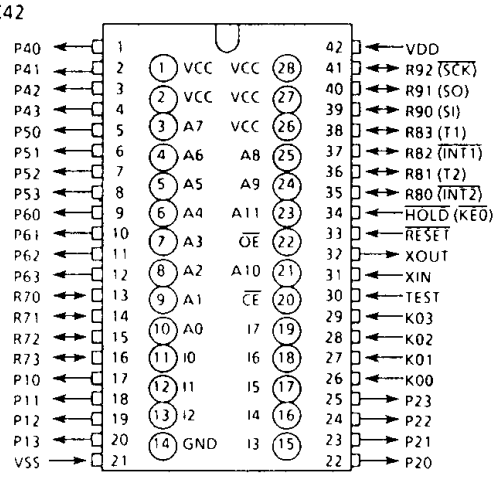
CMOS 4-BIT MICROCONTROLLER

TMP47C991E
TMP47C991G

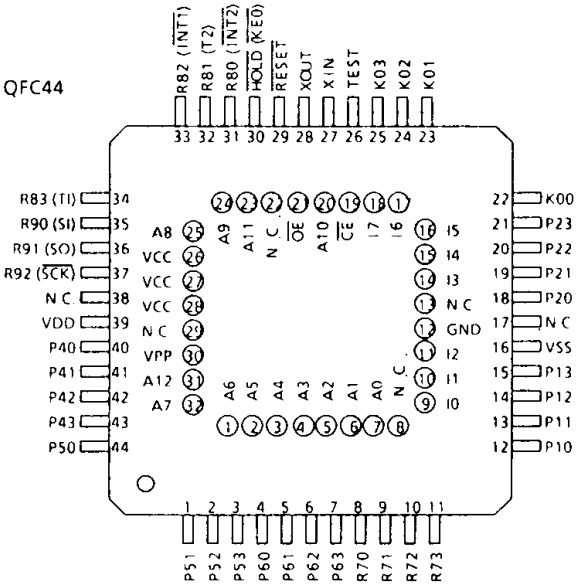
The 47C991, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C210A/410A application systems (programs).
The 47C991 is pin compatible with the 47C210A/410A which are mask-programed ROM devices.
The 47C991 is also used for evaluator of 47C212A/412A.

PIN ASSIGNMENT (TOP VIEW)

SDIC42



QFC44



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V	-	-	150	ns
Data Setup Time	t_{IS}	C_L = 100pF	150	-	-	ns
Data Hold Time	t_{IH}	Topr = - 30 to 70°C	50	-	-	ns

NOTES FOR USE

(1) Program memory

The program area depends on the capacity of EPROM. See Figure 1.

When this chip is used as evaluator of the 47C210A/212A, data conversion table for [OUTB @HL] instruction must be allocated at two areas and they must be the same contents as shown in Figure 1 (a). When a 32K EPROM is used, the pins of 1, 2, 27, and 28 on the package are not used.

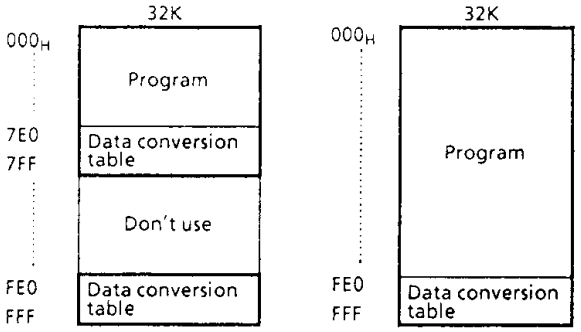


Figure 1. Program area

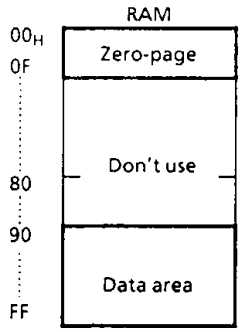


Figure 2. RAM addressing

(2) Data memory

The 47C991 contains 256 x 4-bit data memory. When the 47C991 is used as the 47C210A evaluator, programming should be performed assuming that the RAM is assigned to addresses 00_H - $0F_H$ and 90_H - FF_H as shown in Figure 2.

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C991 are similar to the code HA of the 47C210A/410A. When this chip is used as evaluator with other I/O code, it is necessary to provide the external resistors.

Figure 3. I/O code and external circuitry

(4) In case using evaluator for the 47C212A/412A

The 47C991 can be used as the 47C212A/412A evaluator by connecting an external resistor to ports P1, P2 and P4 through P6. Note that, since the 47C212A/412A have no R73 pins, "1" is read out when the input instruction is executed.

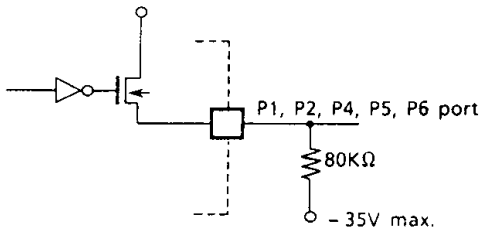


Figure 4. For the 47C212A / 412A