MITEL
SEMICONDUCTOR

PDSP16116

16 X 16 Bit Complex Multiplier

Supersedes October 1996 version, DS3707 - 4.2

DS3707 - 5.3 October 1997

The PDSP16116 contains four 16×16 array multipliers, two 32-bit adder/subtractors and all the control logic required to support Block Floating Point Arithmetic as used in FFT applications.

The PDSP16116A variant will multiply two complex (16+16) bit words every 50ns and can be configured to output the complete complex (32+32) bit result within a single cycle. The data format is fractional two's complement.

In combination with a PDSP16318A, the PDSP16116A forms a two-chip 20MHz complex multiplier accumulator with 20-bit accumulator registers and output shifters. The PDSP16116A in combination with two PDSP16318As and two PDSP1601As forms a complete 20MHz Radix 2 DIT FFT butterfly solution which fully supports block floating point arithmetic. The PDSP16116 has an extremely high throughput that is suited to recursive algorithms as all calculations are performed with a single pipeline delay (two cycle fall-through).

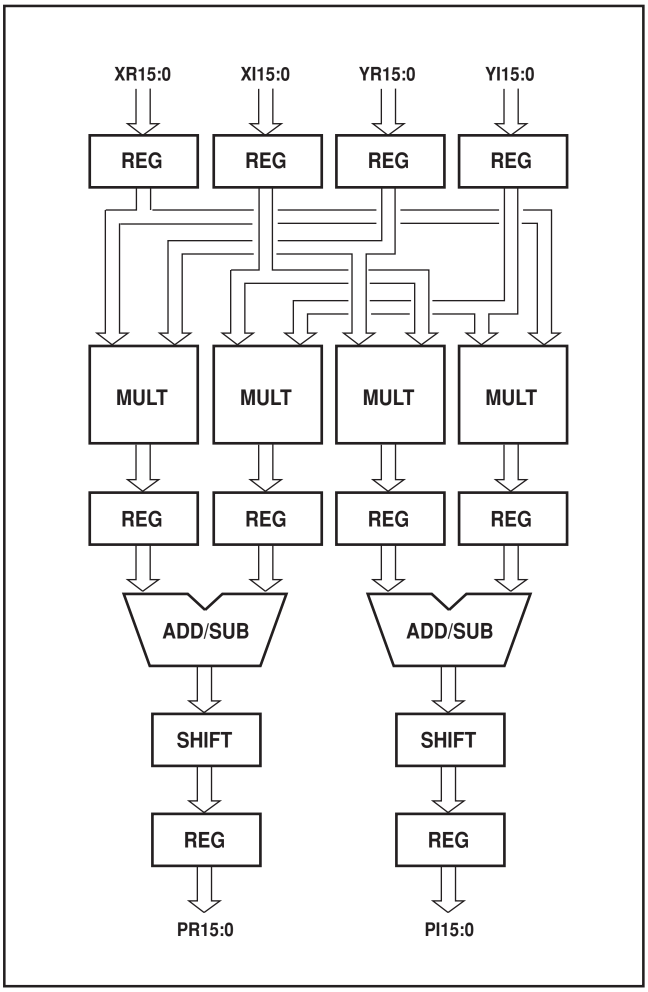


Fig. 1 Simplified block diagram

FEATURES

- Complex Number (16+16)×(16+16) Multiplication
- Full 32-bit Result
- 20MHz Clock Rate
- Block Floating Point FFT Butterfly Support
- (−1)×(−1) Trap
- Two's Complement Fractional Arithmetic
- TTL Compatible I/O
- Complex Conjugation
- 2 Cycle Fall Through
- 144-pin PGA or QFP packages

APPLICATIONS

- Fast Fourier Transforms
- Digital Filtering
- Radar and Sonar Processing
- Instrumentation
- Image Processing

ORDERING INFORMATION

PDSP16116 MC GGDR	10MHz MIL-883 screened
PDSP16116A B0 AC	20MHz Industrial
PDSP16116A A0 AC	20MHz Military
PDSP16116A B0 GG	20MHz Industrial
PDSP16116A MC GGDR	20MHz MIL-883 screened
PDSP16116B B0 AC	25MHz Industrial
PDSP16116D B0 GG	31·5MHz Industrial

ASSOCIATED PRODUCTS

PDSP16318/A	Complex Accumulator
PDSP16112/A	(16+16)×(12+12) Complex Multiplier
PDSP16330/A	Pythagoras Processor
PDSP1601/A	ALU and Barrel Shifter
PDSP16350	Precision Digital Modulator
PDSP16256	Programmable FIR Filter
PDSP16510	Single Chip FFT Processor

SYSTEM FEATURES

The PDSP16116 has a number of features tailored for system applications.

(−1)×(−1) Trap

In multiply operations using two's complement fractional notation, the (−1)×(−1) operation forms an invalid result because +1 is not representable in the fractional number range. The PDSP16116 eliminates this problem by trapping the (−1)×(−1) operation and forcing the multiplier result to become the most positive representable number.

Complex Conjugation

Many algorithms using complex arithmetic require conjugation of complex data stream. This operation has traditionally required an additional ALU to multiply the imaginary component by -1. The PDSP16116 eliminates this requirement by offering on-chip complex conjugation of either of the two incoming complex data words with no loss in throughput.

Easy Interfacing

As with all PDSP family members the PDSP16116 has registered I/O for data and control. Data inputs have independent clock enables and data outputs have independent three state output enables.

Signal	Type	Description	Normal mode configuration
XR15:0	Input	16-bit input for real X data	
XI15:0	Input	16-bit input for imaginary X data	
YR15:0	Input	16-bit input for real Y data	
YI15:0	Input	16-bit input for imaginary Y data	
PR15:0	Output	16-bit output for real P data	
PI15:0	Output	16-bit output for imaginary P data	
CLK	Input	Clock; new data is loaded on rising edge of CLK	
$\overline{\text{CEX}}$	Input	Clock, enable X-port input register	
$\overline{\text{CEY}}$	Input	Clock, enable Y-port input register	
CONX	Input	Conjugate X data	
CONY	Input	Conjugate Y data	
ROUND	Input	Rounds the real and imaginary results	
MBFP	Input	Mode select (BFP/Normal)	Tie low
$\overline{\text{SOBFP}}$	Input	Start of BFP operations (see Note 1)	Tie low
$\overline{\text{EOPSS}}$	Input	End of pass (See Note 1)	Tie low
AR15:1 3	Input	3 MSBs from real part of A-word (See Note 1)	Tie low
AI15:1 3	Input	3 MSBs from imaginary part of A-word (See Note 1)	Tie low
WTA1:0	Input	Word tag from A-word	Tie low
WTB1:0	Input	Word tag from B-word/shift control (See Note 2)	
WTOUT1:0	Output	Word tag output (See Note 1)	
SFTA1:0	Output	Shift control for A-word / overflow flag (See Note 2)	
SFTR2:0	Output	Shift control for accumulator result (See Note 1)	
GWR4:0	Output	Global weighting register contents (See Note 1)	
OSEL1:0	Input	Selects the desired output configuration	
$\overline{\text{OER}}$, $\overline{\text{OEI}}$	Input	Output enables	
V_{DD}	Power	+5V Supply (See Note 3)	
GND	Power	0V Supply (See Note 3)	

NOTES
1. Used only in BFP mode
2. Performs different functions in BFP/Normal modes
3. All supply pins must be connected

Table 1 Signal descriptions

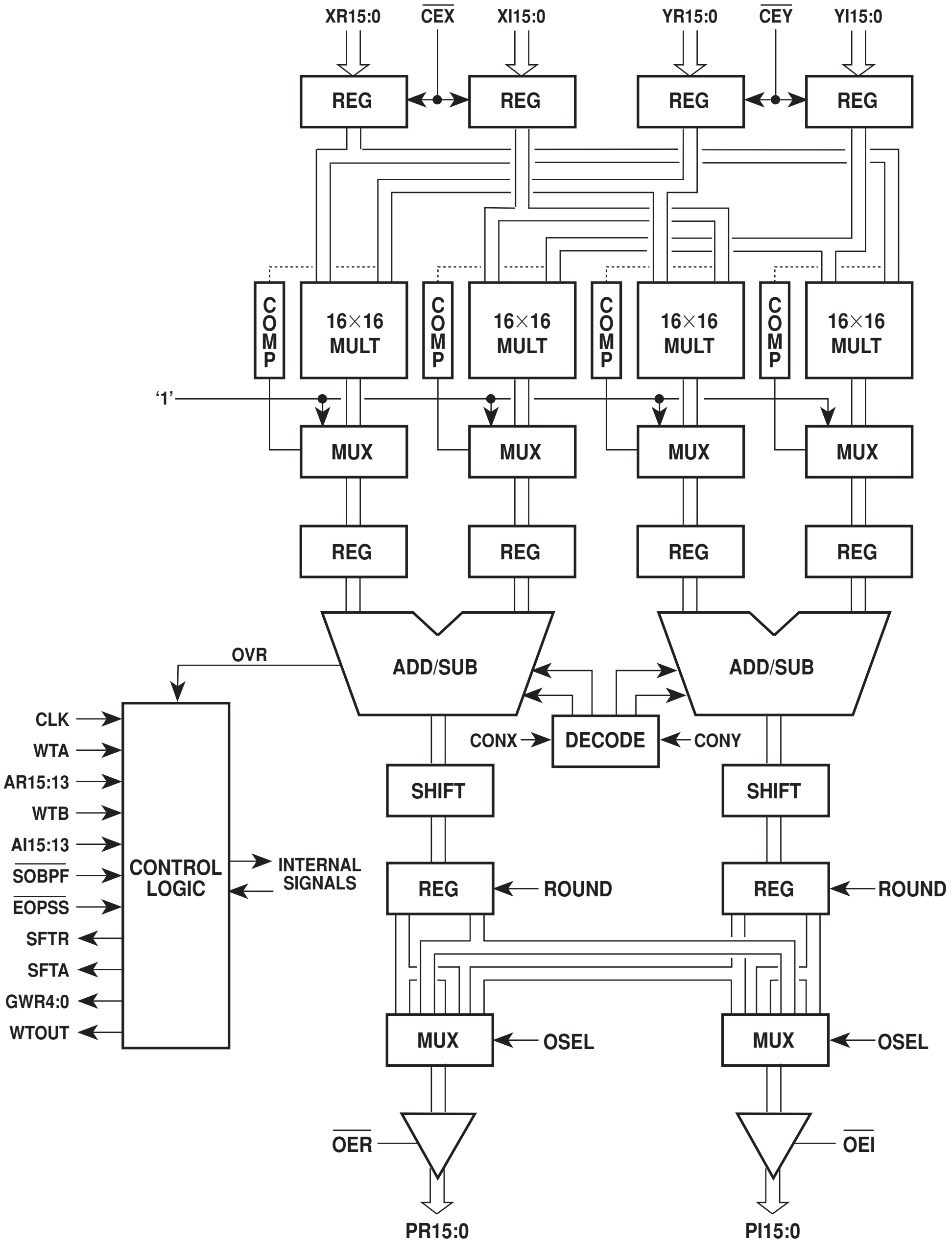
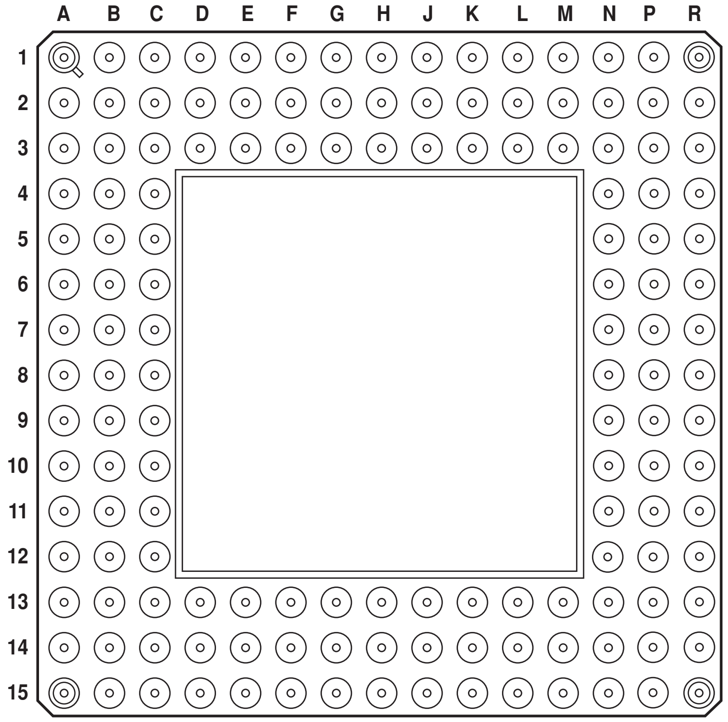
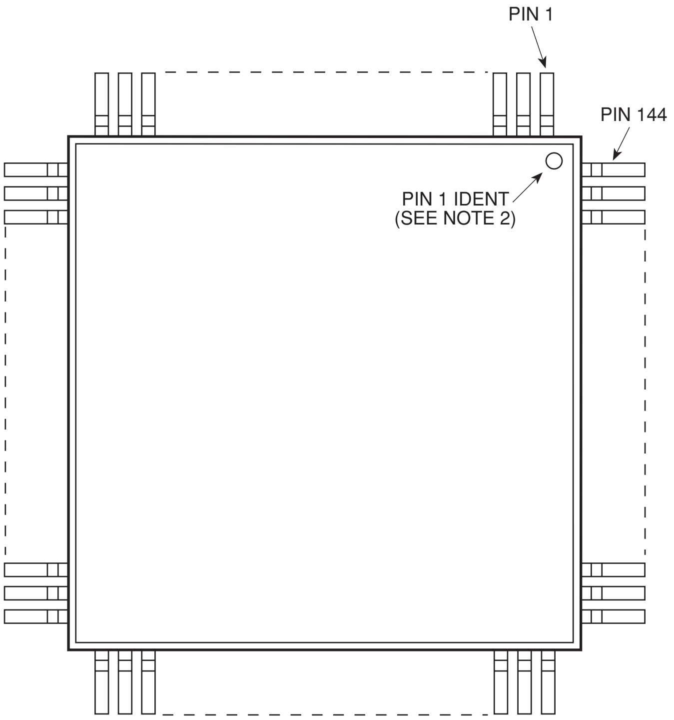


Fig. 2 PDSP16116 Block diagram



AC144 (POWER)

Fig. 3a Pin connections for 144 I/O power pin grid array package (bottom view)



GG144

Fig. 3b Pin connections for 144 I/O ceramic quad flatpack (top view)

Fig. 3 Pin connection diagrams (not to scale). See Table 1 for signal descriptions and Table 2 for pinouts.

GG	AC	Signal	GG	AC	Signal	GG	AC	Signal	GG	AC	Signal
1	D3	PI14	37	N4	XI1	73	P2	GND	109	N14	V_{DD}
2	C2	PI15	38	P3	XI2	74	R1	V_{DD}	110	M13	GND
3	B1	WTOUT1	39	R2	XI3	75	P15	YR12	111	A14	PR13
4	D2	WTOUT0	40	P4	XI4	76	M14	YR11	112	B12	PR12
5	E3	SFTR0	41	N5	XI5	77	L13	YR10	113	C11	PR11
6	C1	SFTR1	42	R3	XI6	78	N15	YR9	114	A13	PR10
7	E2	SFTR2	43	P5	XI7	79	L14	YR8	115	B11	PR9
8	D1	$\overline{\text{OEI}}$	44	R4	XI8	80	M15	YR7	116	A12	PR8
9	F2	CONY	45	N6	XI9	81	K13	YR6	117	C10	PR7
10	F3	CONX	46	P6	XI10	82	K14	YR5	118	B10	PR6
11	E1	ROUND	47	R5	XI11	83	L15	YR4	119	A11	PR5
12	G2	AI13	48	P7	XI12	84	J14	YR3	120	B13	GND
13	G3	AI14	49	N7	XI13	85	J13	YR2	121	C12	V_{DD}
14	F1	AI15	50	R6	XI14	86	K15	YR1	122	A10	PR4
15	G1	AR13	51	R7	XI15	87	J15	YR0	123	A9	PR3
16	H2	AR14	52	P8	$\overline{\text{CEY}}$	88	H14	$\overline{\text{EOPSS}}$	124	B8	PR2
17	H1	AR15	53	R8	$\overline{\text{CEX}}$	89	H15	V_{DD}	125	A8	PR1
18	H3	YI15	54	N8	XR15	90	H13	$\overline{\text{SOBFP}}$	126	C8	PR0
19	J3	YI14	55	N9	XR14	91	G13	WTB1	127	C7	PI0
20	J1	YI13	56	R9	XR13	92	G15	WTB0	128	A7	PI1
21	K1	YI12	57	R10	XR12	93	F15	WTA1	129	A6	PI2
22	J2	YI11	58	P9	XR11	94	G14	WTA0	130	B7	PI3
23	K2	YI10	59	P10	XR10	95	F14	MBFP	131	B6	PI4
24	K3	YI9	60	N10	XR9	96	F13	CLK	132	C6	V_{DD}
25	L1	YI8	61	R11	XR8	97	E15	OSEL1	133	A5	PI5
26	L2	YI7	62	P11	XR7	98	E14	OSEL0	134	B5	GND
27	M1	YI6	63	R12	XR6	99	D15	$\overline{\text{OER}}$	135	A4	PI6
28	N1	YI5	64	R13	XR5	100	C15	SFTA0	136	A3	PI7
29	M2	YI4	65	P12	XR4	101	D14	SFTA1	137	B4	PI8
30	L3	YI3	66	N11	XR3	102	E13	GWR0	138	C5	PI9
31	N2	YI2	67	P13	XR2	103	C14	GWR1	139	B3	PI10
32	P1	YI1	68	R14	XR1	104	B15	GWR2	140	A2	PI11
33	M3	YI0	69	N12	XR0	105	D13	GWR3	141	C4	PI12
34	N3	XI0	70	N13	YR15	106	C13	GWR4	142	C3	PI13
35	B2	GND	71	P14	YR14	107	B14	PR15	143	B9	GND
36	A1	V_{DD}	72	R15	YR13	108	A15	PR14	144	C9	V_{DD}

NOTE. All GND and V_{DD} pins must be used

Table 2 Pin connections for AC144 (Power) and GG144 packages

NORMAL MODE OPERATION

When the MBFP mode select input is held low the 'Normal' mode of operation is selected. This mode supports all complex multiply operations that do not require block floating point arithmetic.

Complex two's complement fractional data is loaded into the X and Y input registers via the X and Y Ports on the rising edge of $\overline{\mathrm{CLK}}$. The X and Y port registers are individually enabled by the $\overline{\mathrm{CEX}}$ and $\overline{\mathrm{CEY}}$ signals respectively. If the registers are required to be permanently enabled, then these signals may be tied to ground.

The Real and Imaginary components of the fractional data are each assumed to have the following format:

Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Weighting	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Where S = sign bit, which has an effective weighting of -2^0

The value of the 16-bit two's complement word is $(-1\times S)+(\text{bit}14\times 2^{-1})+(\text{bit}13\times 2^{-2})+(\text{bit}12\times 2^{-3})\ \ldots$

Multiplier Stage

On each clock cycle the contents of the input registers are passed to the four multipliers to start a new complex multiply operation. Each complex multiply operation requires four partial products (XR×YR), (XR×YI), (XI×YR), (XI×YI), all of which are calculated in parallel by the four 16×16 multipliers. Only one clock cycle is required to complete the multiply stage before the multiplier results are loaded into the multiplier output registers for passing on to the adder/ subtractors in the next cycle. Each multiplier produces a 31-bit result with the duplicate sign bit eliminated. The format of the output data from the multipliers is:

Bit Number	30	29	28	27	26	25	24		7	6	5	4	3	2	1	0
Weighting	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}		2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^0

Adder/Subtractor Stage

The 31-bit real and imaginary results from the multipliers are passed to two 32-bit adder/subtractors. The adder calculates the imaginary result [(XR × YI) + (XI × YR)] and the subtractor calculates the real result (XR × YR) = (XI × YI). Each adder/subtractor produces a 32-bit result with the following format:

Bit Number	31	30	29	28	27	26		8	7	6	5	4	3	2	1	0
Weighting	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}		2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^1

Rounding

The ROUND control when asserted rounds the most significant 16 bits of the full 32-bit result from the shifter. If the ROUND signal is active (high), then bit 16 is set to '1', rounding the most significant 16 bits of the shifted result. (The least significant 16 bits are unaffected). Inserting a '1' ensures that the rounding error is never greater than 1 LSB and that no DC bias is introduced as a result of the rounding processes. The format of the rounded result is:

Bit Number	31	30	29	28	27		18	17	16	15	14	13		2	1	0
Weighting	S	2^{0}	2^{-1}	2^{-2}	2^{-3}		2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}		2^{-28}	2^{-29}	2^{-30}

$\longleftarrow$ **ROUNDED VALUE** $\longrightarrow$ $\longleftarrow$ **LSBs** $\longrightarrow$

The effective weighting of the sign bit is -2^1

Result Correction

Due to the nature of the fraction two's complement representation it is possible to represent -1 exactly but not $+1$. With conventional multipliers this causes a problem when -1 is multiplied by -1 as the multiplier produces an incorrect result. The PDSP16116 includes a trap to ensure that the most positive number (value = $1{\cdot}2^{-30}$, hex = 7FFFFFFF) is substituted for the incorrect result. The multiplier result is therefore always a correct fractional value. Fig.2 shows the value '1' being multiplexed into the data path controlled by four comparators.

Complex Conjugation

Either the X or Y input data may be complex conjugated by asserting the CONX or CONY signals respectively. Asserting either of these signals has the effect of inverting (multiplying by -1) the imaginary component of the respective input. Table 3 shows the effect of CONX and CONY on the X and Y inputs.

CONX	CONY	Function	Operation
Low	Low	X × Y	(XR + XI)×(YR + YI)
High	Low	Conj. X × Y	(XR − XI)×(YR + YI)
Low	High	X × Conj. Y	(XR + XI)×(YR − YI)
High	High	Invalid	Invalid

Table 3 Conjugate functions

Shifter

Each of the two adder/subtractors are followed by shifters controlled via the WTB control input. These shifters can each apply two different shifts; however, the same shift is applied to both real and imaginary components. The four shift options are:

1. WTB1:0 = 11 Shift complex product one place to the left, giving a shifter output format:

Bit Number	31	30	29	28	27	26	25		7	6	5	4	3	2	1	0
Weighting	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}		2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}

The effective weighting of the sign bit is -2^0

2. WTB1:0 = 00 No shift applied, giving a shifter output format:

Bit Number	31	30	29	28	27	26		8	7	6	5	4	3	2	1	0
Weighting	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}		2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^1

3. WTB1:0 = 01 Shift complex product one place to the right, giving a shifter output format:

Bit Number	31	30	29	28	27	26	25	24		6	5	4	3	2	1	0
Weighting	S	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}		2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}

The effective weighting of the sign bit is -2^2

4. WTB1:0 = 10 Shift complex product two places to the right, giving a shifter output format:

Bit Number	31	30	29	28	27	26	25	24		6	5	4	3	2	1	0
Weighting	S	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}		2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}

The effective weighting of the sign bit is -2^3

Overflow

If the left shift option is selected and the adder/subtractor contains a 32-bit word, then an invalid result will be passed to the output. An invalid output arising from this combination of events will be flagged by the SFTA0 flag output. The SFTA0 flag will go high if either the real or imaginary result is invalid.

Output Select

The output from the shifters is passed to the output select mux, which is controlled via the OSEL inputs. These inputs are not registered and hence allow the output combination to be changed within each cycle. The full complex 64-bit result from the multiplier may therefore be output within a single cycle. The OSEL control selects four different output combinations as summarised in Table 4.

OSEL1	OSEL0	PR	P1
0	0	MSR	MSI
0	1	LSR	LSI
1	0	MSR	LSR
1	1	MSI	LSI

Table 4 Output selection

MSR and LSR are the most and least siginificant 16-bit words of the real shifter output, MSI and LSI are the most and least significant 16-bit words of the imaginary shifter output.

The output select options allow two different modes for extracting the full 32-bit result from the PDSP16116. The first mode treats the two 16-bit outputs as real and imaginary ports, allowing the real and imaginary results to be output in two halves on the real and imaginary output ports. The second mode treats the two 16-bit outputs as one 32-bit output and allows the real and imaginary results to be output as 32-bit words.

PIN DESCRIPTIONS

XR, XI, YR, YI

Data inputs, 16 bits. Data is loaded into the input registers from these ports on the rising edge of CLK. The data format is fractional two's complement, where the MSB (sign bit) is bit 15. In normal mode the weighting of the MSB is -2^0 i.e. -1.

PR, PI

Data outputs, 16 bits. Data is clocked into the output registers and passed to the PR and PI outputs on the rising edge of CLK. The data format is fractional two's complement. The field of the internal result selected for output via PR and PI is controlled by signals OSEL1:0 (see Table 4).

CLK

Common clock to all internal registers

$\overline{\text{CEX}}$, $\overline{\text{CEY}}$

Clock enables for X and Y input ports. When low these inputs enable the CLK signal to the X or Y input registers, allowing new data to be clocked into the Multiplier.

CONX, CONY

Conjugate controls. If either of these inputs is high on the rising edge of CLK, then the data on the associated input has its imaginary component inverted (multiplied by -1), see Table 3. CONX and CONY affect data input on the same clock rising edge.

ROUND

The ROUND control pin is used to round the most significant 16 bits of the output register. The ROUND input is not latched and is intended to be tied high or low depending upon the application.

MBFP

Mode select. When high, block floating point (BFP) mode is selected. This allows the device to maintain the dynamic range of the data using a series of word tags. This is especially useful in FFT applications. When low, the chip operates in normal mode for more general applications. This pin is intended to be tied high or low, depending on application.

$\overline{\text{SOBFP}}$ (BFP Mode Only)

Start of BFP. This input should be held low for the first cycle of the first pass of the BFP calculations (see Fig.7). It serves to reset the internal registers associated with BFP control. When operating in normal mode this input should be tied low.

$\overline{\text{EOPSS}}$ (BFP Mode Only)

End of pass. This input should be held low for the last cycle of each pass and for the lay time between passes. It instructs the control logic to update the value of the global weighting register and prepare the BFP circuitry for the next pass. When operating in normal mode this input should be tied low.

AR15:13 (BFP Mode Only)

Three MSBs of the real part of the A-word. These are used in the FFT butterfly application (see Fig. 4) to determine the magnitude of the real part of the A-word and, hence, to determine if there will be any change of word growth in the PDSP16318 Complex Accumulator. When operating in normal mode, these inputs are not used and may be tied low.

AI15:13 (BFP Mode Only)

Three MSBs of the imaginary part of the A-word. Used in the same fashion as AR15:13.

SFTR2:0 (BFP Mode Only) Accumulator result shift control. These pins should be linked directly to the S2:0 pins on the PDSP16318 Complex Accumulator. They control the accumulator's barrel shifter (see Table 5). The purpose of this shift is to minimise sign extension in the multiplier or accumulator ALUs. In normal mode, SFTR2:0 are not used and should be left unconnected.

SFTR2:0	Function
000	Reserved
001	Reserved
010	Reserved
011	Shift right by one
100	No shift
101	Shift left by one
110	Shift left by two
111	Reserved

Table 5 Accumulator shifts (BFP mode)

GWR4:0 (BFP Mode Only)

Contents of the global weighting register. The GWR stores the weighting of the largest word present with respect to the weighting of the original input words. Hence, if the contents of the GWR are 00010, it indicates that the largest word currently being processed has its binary point two bits to the right of the original data at the start of the BFP calculations.

The contents of this register are updated at the end of each pass, according to the largest value of WTOUT occuring during that pass. For example, if WTOUT = 11, then GWR will be increased by 2 (see Table 6). The GWR is presented in two's complement format. In normal mode, GWR4:0 are not used and should be left unconnected.

WTOUT1:0 (BFP Mode Only)

Word tag output. This tag records the weighting of the output words from the current cycle relative to the current global weighting register (see Table 6). It should be stored along with the A′ and B′ words as it will form the input word tags, WTA and WTB, for each complex word during the next pass. In normal mode, WTOUT1:0 are not used and should be left unconnected.

WTOUT1:0	Weighting of the output relative to the current global weighting register
00	One less
01	The same
10	One more
11	Two more

Table 6 Word tag weightings

WTA1:0 (BFP Mode Only)

Word tag from the A-word. This word records the weighting of the A-word relative to the global weighting register on the previous pass. Although the A-word itself is not processed in the PDSPl 6116, this information is required by the control logic for the radix 2 butterfly FFT application. These inputs should be tied low in normal mode.

WTB1:0 (BFP and Normal Modes)

In BFP mode, this is the word tag from the B-word. This is operated in the same manner as WTA but for the B-word. The value of the word tags are used to ensure that the binary weighting of the A-word and the product of the complex multiplier are the same at the inputs to the complex accumulator. Depending on which word is the larger, the weighting adjustment is performed using either the internal shifter or an external shifter controlled by SFTA. The word tags are also used to maintain the weighting of the final result to within plus two and minus one binary points relative to the new GWR. (On the first pass all word tags will be ignored). In normal mode. these inputs perform a different function. They directly control the internal shifter at the output port as shown in Table 7.

WTB1:0	Function
11	Shift complex product 1 place to the left
00	No shift applied
01	Shift complex product 1 place to the right
10	Shift complex product 2 places to the right

Table 7 Normal mode shift control

SFTA1:0 (BFP and Normal Modes)

In BFP mode, these signals act as the A-word shift control. They allow shifting from one to four places to the right, (see Table 8). Depending on the relative weightings of the A-words and the complex product, the A-word may have to be shifted to the right to ensure compatible weightings at the inputs to the PDSP16318 complex accumulator. The two words must have the same weighting if they are to be added.

In normal mode, SFTA0 performs a different function. If WTB1:0 is set to implement a left shift, then overflow will occur if the data is fully 32 bits wide. This pin is used to flag such an overflow. SFTA1 is not used in normal mode.

SFTA1:0	Function
00	Shift A-word 1 place to the right
01	Shift A-word 2 places to the right
10	Shift A-word 3 places to the right
11	Shift A-word 4 places to the right

Table 8 External A-word shift control

OSEL1 :0

The outputs from the device are selected by the OSEL0 and OSEL1 instruction bits. These controls allow selection of the output combination during the current cycle (they are not registered). There are four possible output configurations that allow either complex outputs of the most or least significant bytes, or real or imaginary outputs of the full 32-bit word (see Table 4). OSEL0 and OSEL1 should both be tied low when in BFP mode.

BFP MODE FFT APPLICATION

The PDSP16116 may be used as the main arithmetic unit of the butterfly processor, which will allow the following FFT benchmarks:

- 1024-point complex radix 2 transform in 517µs
- 512-point complex radix 2 transform in 235µs
- 256-point complex radix 2 transform in 106µs

In addition, with pin MBFP tied high, the BFP circuitry within the PDSP16116 can be used to adaptively rescale data throughout the course of the FFT so as to give high-resolution results. The BFP system on the PDSP16116 can be used with any variation of the radix 2 decimation-in-time (DIT) FFT, for example, the constant geometry algorithm, the in-place algorithm etc. An N-point Radix 2 DIT FFT is split into log(N) passes. Each pass consists of N/2 'butterflies', each performing the operation:

$$A' = A + BW$$
$$B' = A - BW$$

Where W is the complex coefficient and A and B are the complex data. Fig.4 illustrates how a single PDSP16116 may be combined with two PDSP1601s and two PDSP16318s to form a complete BFP butterfly processor. The PDSP16318s are used to perform the complex addition and subtraction of the butterfly operation, while the PDSP1601s are used to match the data path of the A-word to the pipelining and shifting operations within the PDSP16116.

For more information on the theory and construction of this butterfly processor, refer to application note AN59.

BFP MODE OPERATION

The BFP mode on the PDSP16116 is intended for use in the FFT application described above, that is, it is intended to prevent data degradation during the course of an FFT calculation. The operation of the PDSP16116-based BFP buttertly processor (see Fig.4) is described below.

The Block Floating Point System

A block floating point system is essentially an ordinary integer arithmetic system with some additional logic, the purpose of which is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in perlormance.

The initial data used by the FFT should all have the same binary arithmetic weighting. In other words, the binary point should occupy the same position in every data word as is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited. In the BFP system used in the PDSP16116, there are, within any one pass of the FFT, four possible positions of the binary point wihin the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass the following four positions of binary point may be available, each denoted by a certain value of word:

XX·XXXXXXXXXXXX word tag = 00
XXX·XXXXXXXXXXX word tag = 01
XXXX·XXXXXXXXXX word tag = 10
XXXXX·XXXXXXXXX word tag = 11

At the end of each constituent pass of the FFT, the positions of the binary point supported may change to reflect the trend of data increase or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may be changed to:

XX·XXXXXXXXXXXX word tag = 00
XXX·XXXXXXXXXXX word tag = 01
XXXX·XXXXXXXXXX word tag = 10
XXXXX·XXXXXXXXX word tag = 11

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the GWR. Thus, the position of the binary point can be determined relative to its initial position by modifying the value of GWR by WTOUT for a given word as shown in Table 6. As an example, if GWR=01001 and WTOUT=10 then the binary point has moved 10 places to the right of its original position.

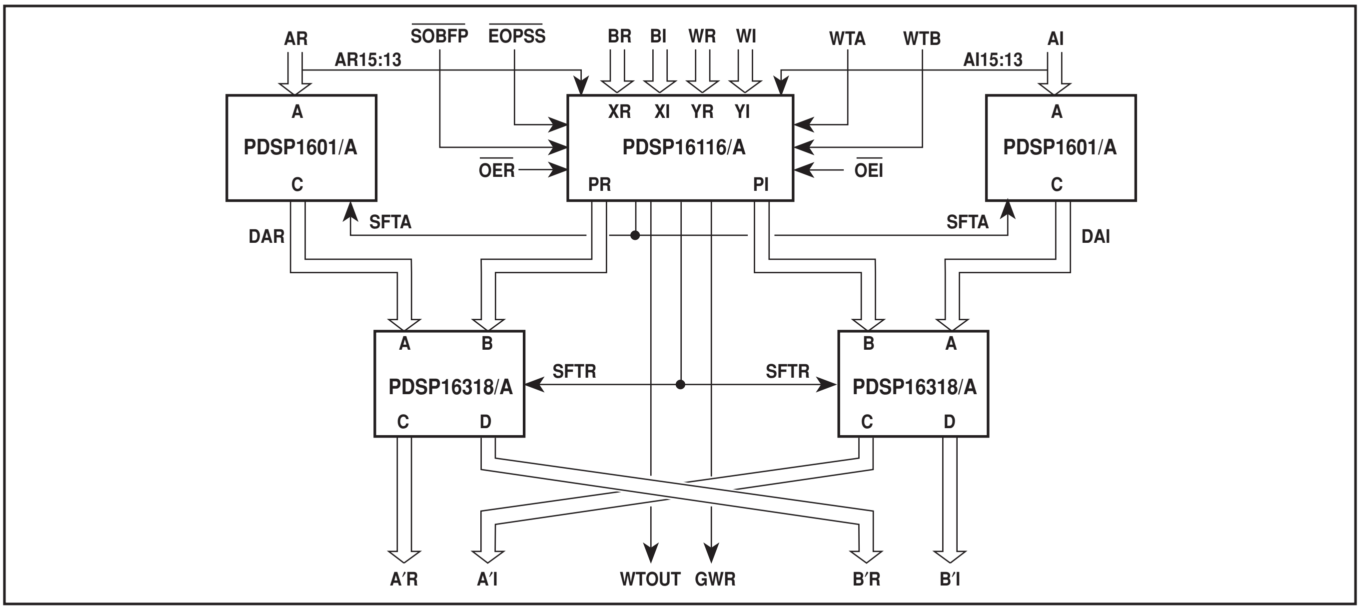


Fig. 4 FFT butterfly processor

The butterfly operation

The butterfly operation is the arithmetic operation which is repeated many times to produce an FFT. The PDSP16116- based butterfly processor performs this operation in a low power high accuracy chip set.

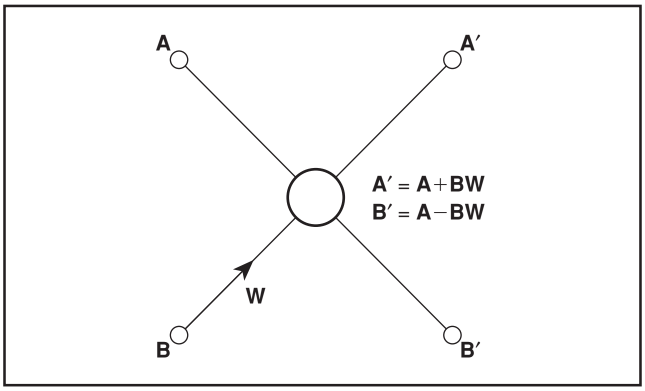


Fig. 5 Butterfly operation

A new butterfly operation is commenced each cycle, requiring a new set ot data for B, W, WTA and WTB. Five cycles later, the corresponding results A′ and B′ are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601/A and PDSP16318/A. The timing of the data and control signals is shown in Fig.6.

The results (A′ and B′) of each butterfly calculation in a pass must be stored to be used later as the input data (A and B) in the next pass. Each result must be stored together with its associated word tag, WTOUT. Although WTOUT is common to both A′ and B′, it must be stored separately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A word is known as WTA and the word tag associated with the B word is known as WTB. Hence, the WTOUTs from one pass will become the WTAs and WTBs for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data initially has the same weighting. Hence, during the first pass alone, the inputs WTA and WTB are ignored.

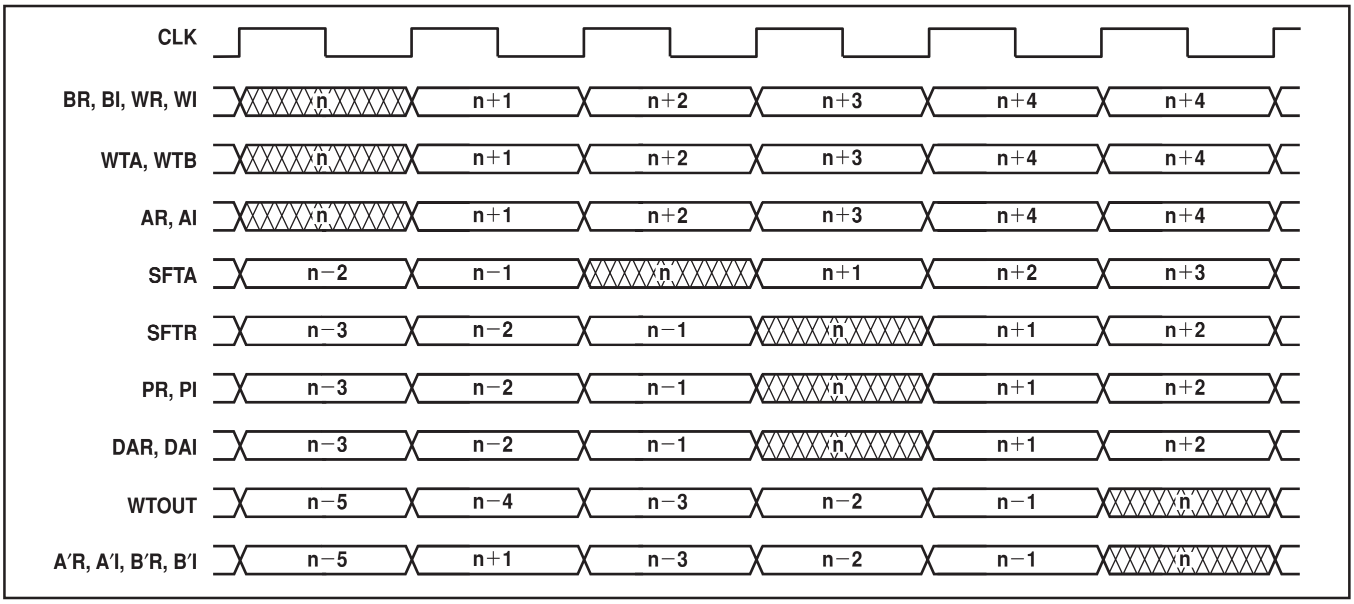


Fig. 6 Butterfly data and control signals

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided:

$\overline{\text{SOBFP}}$ - start of the FFT
$\overline{\text{EOPSS}}$ - end of current pass

These inform the PDSPI 6116/A when an FFT is starting and when each pass is complete. Fig.7 shows how these signals should be used and a commentary is provided below.

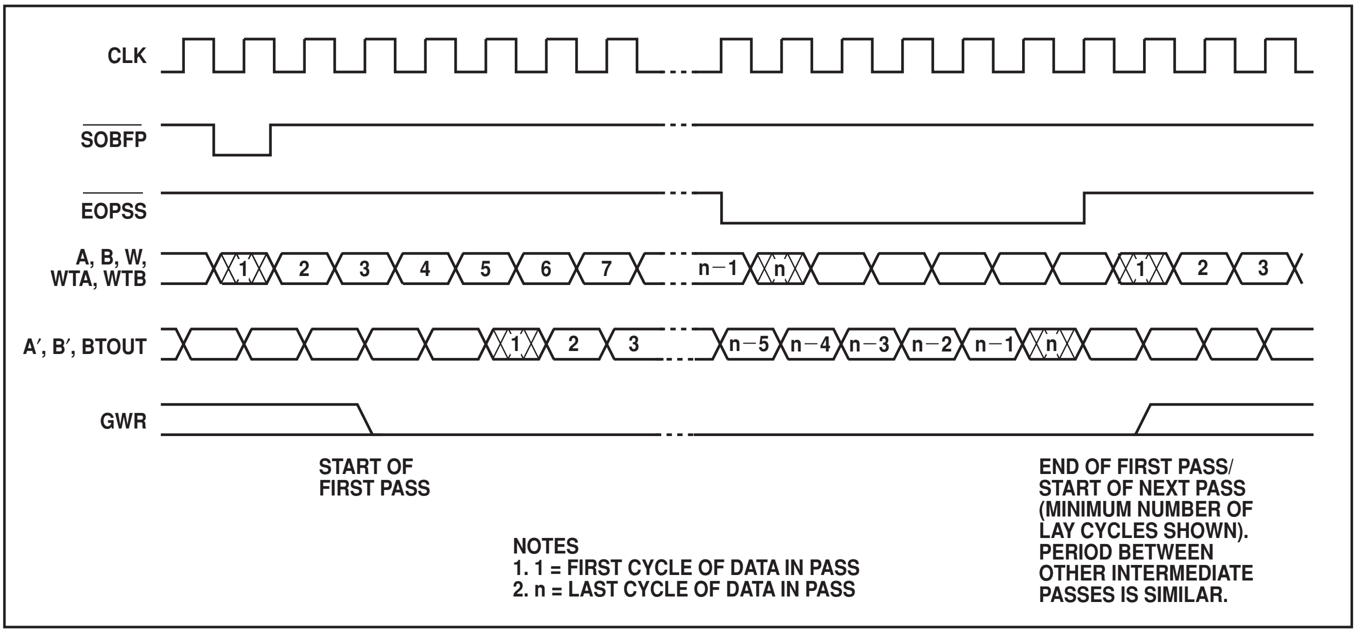
To begin the FFT, the signal $\overline{\text{EOPSS}}$ should be set high (where it will remain for the duration of the pass). $\overline{\text{SOBFP}}$ should be pulled low during the initial cycle when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle $\overline{\text{SOBFP}}$ must be pulled high where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the $\overline{\text{EOPSS}}$ should be pulled low and held low for a minimum of five cycles, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before beginning the following pass.

Should a longer pause be required between passes – to arrange the data for the next pass, for example – then $\overline{\text{EOPSS}}$ may be kept low as long as necessary; the next pass cannot commence until it is brought high again. On the initial cycle of each new pass, the signal $\overline{\text{EOPSS}}$ should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

FFT Output Normalisation

When an FFT system outputs a series of FFT results for display, storage or transmission, it is essential that all results are compatible, i.e. with the binary point in the same position. However, in order to preserve the dynamic range of the data in the FFT calculation, the PDSP1601/A employs a range of different weightings. Therefore, data must be re-formatted at the end of the FFT to the pre-determined common weighting. This can be done by comparing the exponent of given data word with the pre-determined universal exponent and then shifting the data word by the difference. The PDSP1601/A, with its multifunction 16-bit barrel shifter, is ideally suited to this task.

According to theory, the largest possible data result from an FFT is N times the largest input data. This means that the binary point can move a maximum of $\log_2(N)$ places to the right. Hence, if the universal exponent is chosen to be $\log_2(N)$ this should give a sufficient range to represent all data points faithfully.



START OF FIRST PASS

END OF FIRST PASS/ START OF NEXT PASS (MINIMUM NUMBER OF LAY CYCLES SHOWN). PERIOD BETWEEN OTHER INTERMEDIATE PASSES IS SIMILAR.

NOTES
1. 1 = FIRST CYCLE OF DATA IN PASS
2. n = LAST CYCLE OF DATA IN PASS

Fig. 7 Use of the BFP control signals

In practice, data output may never approach the theoretical maximum. Hence, it may be worthwhile to try various universal exponents and choose the one best suited to the particular application.

Data is output from the butterfly processor with a two-part exponent: the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual dataword. To find the complete exponent for a given word, the GWR for that FFT must be modified by its WTOUT as shown in Table 6. The result is the number of places the binary point has shifted to the right during the course of the FFT.

This value must be compared with the universal exponent to determine the shift required. This is done by subtracting it from the universal exponent. The number of places to be shifted is equal to the difference between the two exponents. The shift can be implemented in a PDSP1601/A (the shift value is fed into the SV port).

As FFT data consists of real and imaginary parts, either two PDSP1601/As must be used (controlled by the same logic) or a single PDSP1601/A could be used handling real and imaginary data on alternate cycles (using the same instructions for both cycles).

An example of an output normalisation circuit is shown in Fig.8. Only 4-bit data paths are used in calculating the shift. This means that we must be able to trap very small values negative of GWR and force a 15-bit right shift in such cases.

NB It is easier to simply add the word tag to the exponent for the purpose of determing the shift required, instead of modifying it according to Table.6. To compensate for this, the universal exponent may be increased by one.

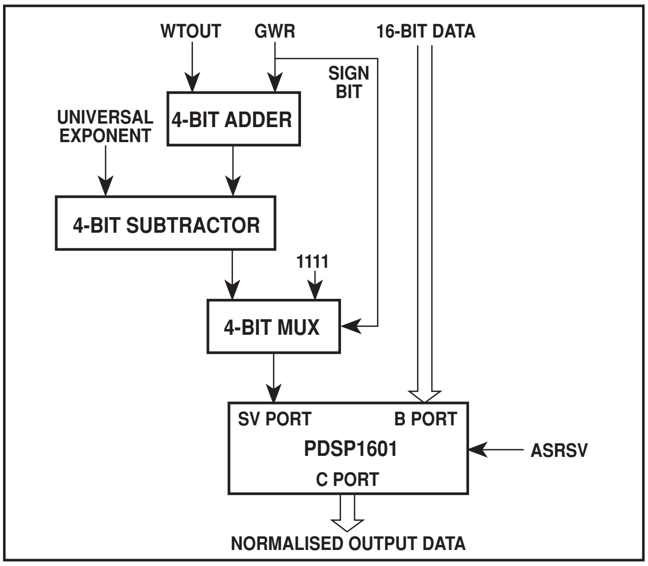


Fig. 8 Output normalisation circuit

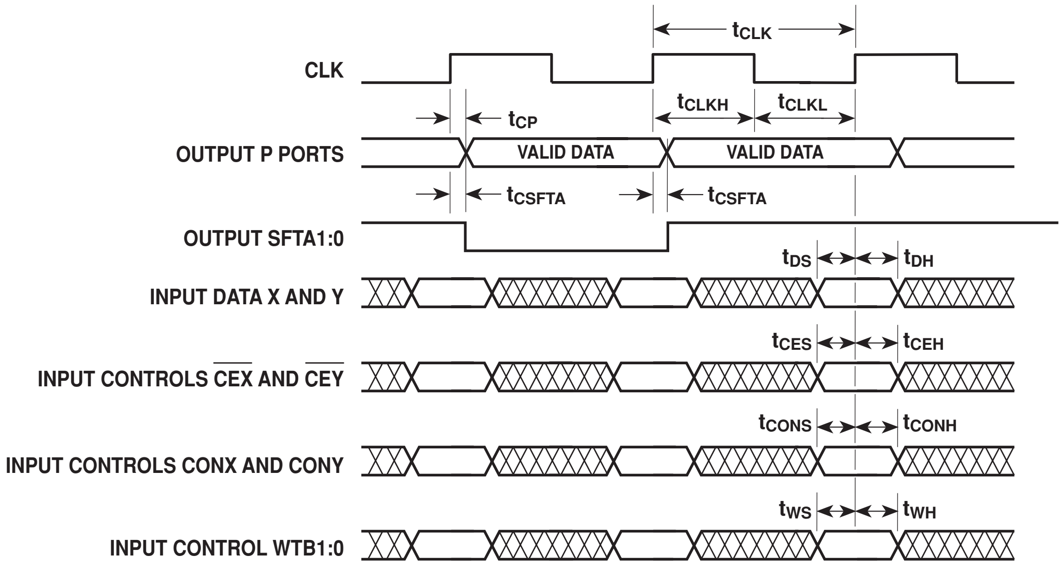


Fig. 9 Normal mode timing

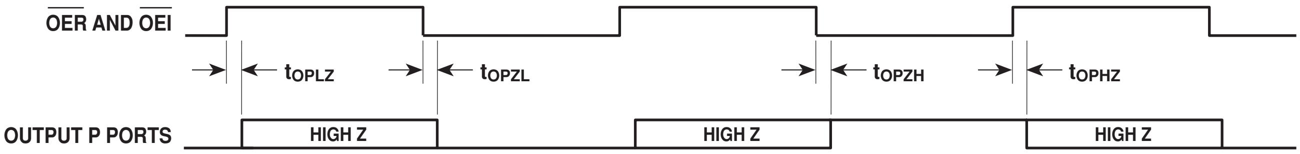
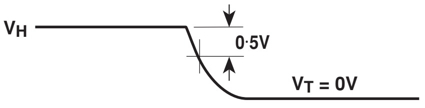
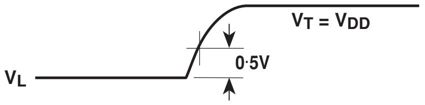
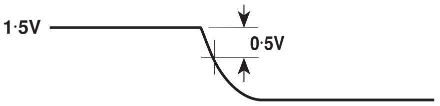
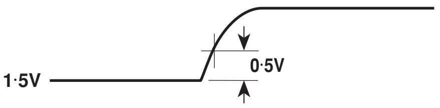
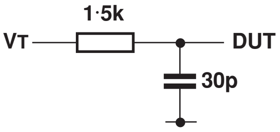


Fig. 10 Output tristate timing

Test	Waveform measurement level
Delay from output high to output high Z (t_{OPHZ})	
Delay from output low to output high Z (t_{OPLZ})	
Delay from output high Z to output low (t_{OPZL})	
Delay from output high Z to output high (t_{OPZH})	
V_H is the voltage reached when the output is driven high V_L is the voltage reached when the output is driven low	



Three state delay measurement load

Fig. 11 Three state delay measurement

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions, unless otherwise stated:

V_{DD} = +5V±10%, GND = 0V, T_{AMB} (Industrial) = −40°C to +85°C, T_{AMB} (Military) = −55°C to +125°C

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2·4		-	V	I_{OH} = 8mA
Output low voltage	V_{OL}	-		0·4	V	I_{OL} = −8mA
Input high voltage	V_{IH}	3·0		-	V	CLK input only
Input high voltage	V_{IH}	2·2		-	V	All other inputs
Input low voltage	V_{IL}	-		0·8	V	GND < V_{IN} < V_{DD}
Input leakage current	I_{IN}	−10		+10	µA	
Input capacitance	C_{IN}		10		pF	GND < V_{OUT} < V_{DD}
Output leakage current	I_{OZ}	−50		+50	µA	V_{DD} = +5·5V
Output short circuit current	I_{OS}	10		300	mA	

Switching Characteristics

Characteristic	Symbol	PDSP16116		PDSP16116A		PDSP16116D		Units	Conditions	Fig.
		Min.	Max.	Min.	Max.	Min.	Max.			
P ports setup time	t_{CP}	5	45	5	23	5	23	ns	30pF	9
WTOUT1:0 setup time	t_{CW}	5	30	5	20	5	20	ns	30pF	
GWR4:0 setup time	t_{CG}	5	30	5	20	5	20	ns	30pF	
SFTA1:0 setup time	t_{CSFTA}	5	60	5	30	5	30	ns	30pF	9
SFTR2:0 setup time	t_{CSFTR}	5	50	5	28	5	28	ns	30pF	
$\overline{\text{CEX}}$ or $\overline{\text{CEY}}$ setup time	t_{CES}	11	-	8	-	8	-	ns		9
$\overline{\text{CEX}}$ or $\overline{\text{CEY}}$ hold time	t_{CEH}	-	0	-	0	-	0	ns		9
X or Y ports setup time	t_{DS}	11	-	8	-	8	-	ns		9
X or Y ports hold time	t_{DH}	-	2	-	0	-	2	ns		9
WTA, WTB, $\overline{\text{SOBFP}}$ or $\overline{\text{EOPSS}}$ setup time	t_{WS}	14	-	8	-	8	-	ns		9
WTA, WTB, $\overline{\text{SOBFP}}$ or $\overline{\text{EOPSS}}$ hold time	t_{WH}	-	0	-	0	-	0	ns		9
CONX or CONY setup time	t_{CONS}	14	-	8	-	8	-	ns		9
CONX or CONY hold time	t_{CONH}	-	0	-	0	-	0	ns		9
AR15:13 or AI15:13 setup time	t_{AS}	14	-	8	-	8	-	ns		
AR15:13 or AI15:13 hold time	t_{AH}	-	0	-	0	-	2	ns		
OSEL to valid P ports	t_{OP}	-	35	-	20	-	20	ns	30pF	
$\overline{\text{OER}}$ or $\overline{\text{OEI}}$ high to PR or PI high to high Z	t_{OPHZ}	-	35	-	25	-	25	ns		10, 11
$\overline{\text{OER}}$ or $\overline{\text{OEI}}$ low to PR or PI low to high Z	t_{OPLZ}	-	45	-	25	-	25	ns		10, 11
$\overline{\text{OER}}$ or $\overline{\text{OEI}}$ low to PR or PI high Z to high	t_{OPZH}	-	22	-	18	-	18	ns		10, 11
$\overline{\text{OER}}$ or $\overline{\text{OEI}}$ high to PR or PI high Z to low	t_{OPZL}	-	24	-	18	-	18	ns		10, 11
CLK frequency	f_{CLK}		10		20		31·5	MHz		
CLK period	t_{CLK}	100	-	50	-	31·7	-	ns		9
CLK high time	t_{CLKH}	30	-	12	-	12	-	ns		9
CLK low time	t_{CLKL}	20	-	12	-	12	-	ns		9
V_{DD} current (CMOS input levels)	I_{DDC}	-	60	-	80	-	80	mA	See Note 1	
V_{DD} current (TTL input levels)	I_{DDT}	-	100	-	130	-	130		See Note 1	

NOTES
1. V_{DD} = +5·5V, outputs unloaded, clock frequency = Max.
2. The PDSP16116B is specified as the PDSP16116A except that the maximum clock frequency is guaranteed at 25MHz, with a minimum clock period of 40ns.

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

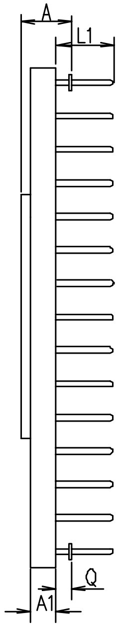
Supply voltage, V_{DD}	−0·5V to +7·0V
Input voltage, V_{IN}	−0·5V to V_{DD} +0·5V
Output voltage, V_{OUT}	−0·5V to V_{DD} +0·5V
Clamp diode current per pin, I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature, T_S	−65°C to+150°C
Ambient temperature with power applied, T_{AMB}	
Military grade	−55°C to+125°C
Industrial grade	−40°C to+85°C
Junction temperature	120°C
Package power dissipation	1000mW
Thermal resistances	
Junction-to-case, θ_{JC}	12°C/W
Junction-to-ambient, θ_{JA}	29°C/W

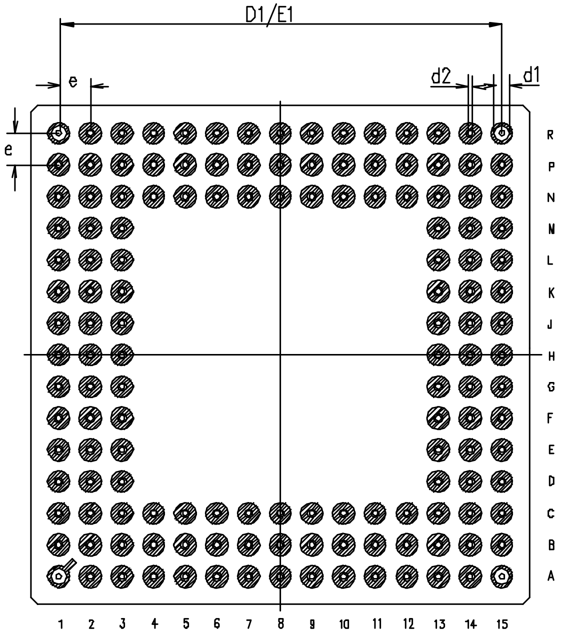
NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation should not be exceeded for more than1 second, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.

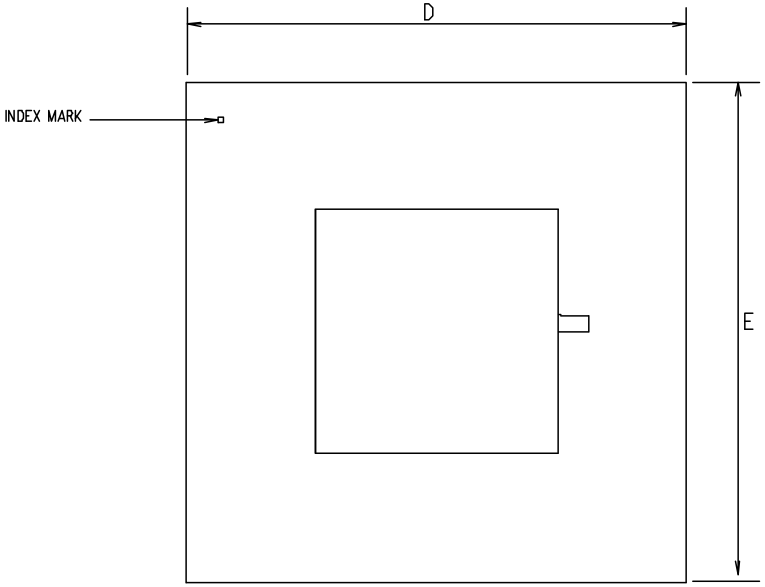
WIRE BOND PAD / CONNECTOR PIN INTERCONNECTION PLAN

W/B NO.	PIN NO.
1	A1
2	B1
3	D3
4	C2
5	C1
6	D2
7	E3
8	D1
9	E2
10	E1
11	F3
12	F2
13	F1
14	G2
15	G3
16	G1
17	H2
18	H1
19	H3
20	J1
21	J2
22	K1
23	J3
24	K2
25	L1
26	K3
27	L2
28	M1
29	L3
30	M2
31	N1
32	N2
33	M3
34	P1
35	P2
36	N3
37	R1
38	R2
39	N4
40	P3
41	R3
42	P4
43	N5
44	R4
45	P5
46	R5
47	N6
48	P6
49	R6
50	P7
51	N7
52	R7
53	P8
54	R8
55	N8
56	R9
57	P9
58	R10
59	N9
60	P10
61	R11
62	N10
63	P11
64	R12
65	N11
66	P12
67	R13
68	P13
69	N12
70	R14
71	P14
72	N13
73	R15
74	P15
75	M13
76	N14
77	N15
78	M14
79	L13
80	M15
81	L14
82	L15
83	K13
84	K14
85	K15
86	J14
87	J13
88	J15
89	H14
90	H15
91	H13
92	G15
93	G14
94	F15
95	G13
96	F14
97	E15
98	F13
99	E14
100	D15
101	E13
102	D14
103	C15
104	C14
105	D13
106	B15
107	B14
108	C13
109	A15
110	A14
111	C12
112	B13
113	A13
114	B12
115	C11
116	A12
117	B11
118	A11
119	C10
120	B10
121	A10
122	B9
123	C9
124	A9
125	B8
126	A8
127	C8
128	A7
129	B7
130	A6
131	C7
132	B6
133	A5
134	C6
135	B5
136	A4
137	C5
138	B4
139	A3
140	B3
141	C4
142	A2
143	B2
144	C3

S/R	NC
D/A	NC







Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	3.35		4.14		0.132		0.163
A1	1.93		2.39		0.076		0.094
Q	1.14		1.40		0.045		0.055
D	39.60		40.41		1.559		1.591
D1		35.56				1.400	
E	39.60		40.41		1.559		1.591
E1		35.56				1.400	
e	2.54 BSC.				0.100 BSC.		
d1	1.14		1.40		0.045		0.055
d2	0.41		0.51		0.016		0.020
L1	4.45		4.70		0.175		0.185
	Pin features						
N	144						
NOTE	SQUARE						

NOTES:

1 INDEX MARK INDICATES A1 REF CORNER & CAN BE ANY SHAPE

2 PLATING BARS CAN APPEAR IN VARIOUS POSITIONS & SHOULD NOT BE USED FOR ORIENTATION PURPOSES

This drawing supersedes 418/ED/39506/006 issue 4 (Swindon)

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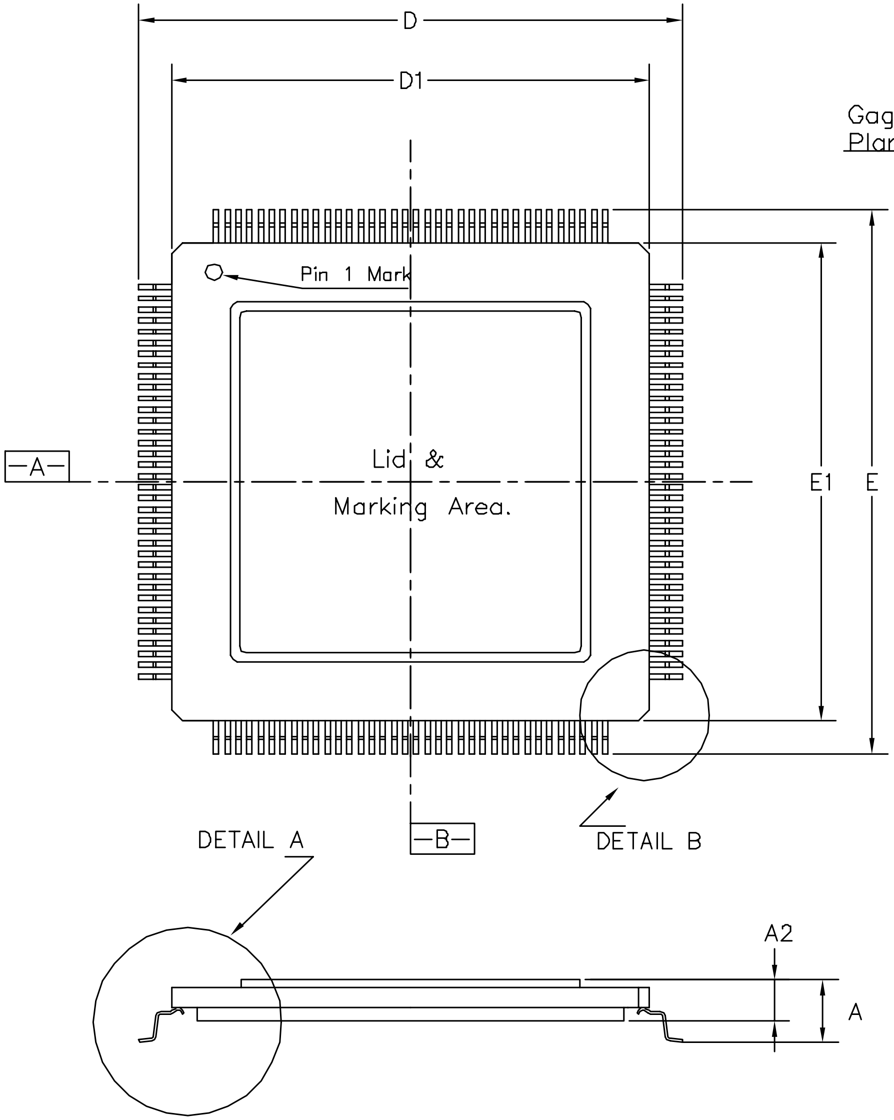
ORIGINATING SITE: SWINDON

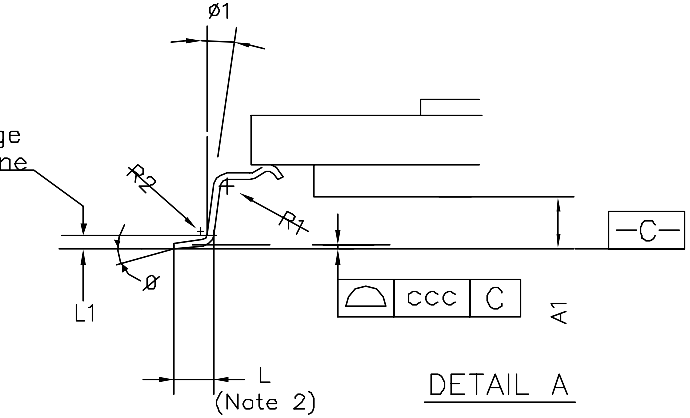
ISSUE	1	2			
ACN	201920	203636			
DATE	16JAN97	2DEC97			
APPD.					

MITEL SEMICONDUCTOR

Title: Outline Drawing for 144 PGA (AC)

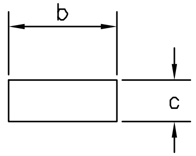
Drawing Number GPD00286

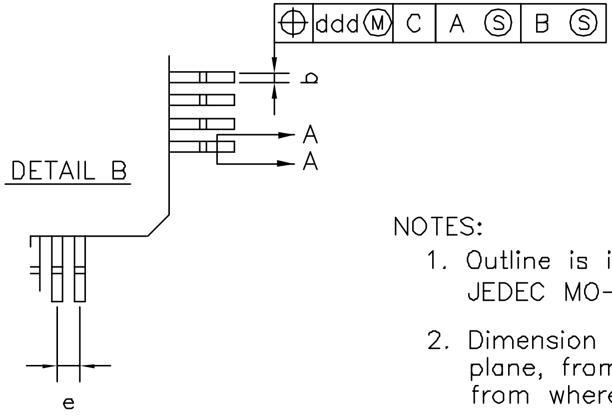




DETAIL A

SECTION A–A





DETAIL B

CONTROL DIMENSIONS (mm)			
SYMBOL	MIN.	NOM.	MAX.
A			4.07
A1	0.25		
A2	2.10	2.50	2.80
D	31.90 BSC.		
D1	28.00 BSC.		
D2	22.75 BSC.		
D3	25.00 BSC.		
E	31.90 BSC.		
E1	28.00 BSC.		
E2	22.75 BSC.		
E3	25.00 BSC.		
e	0.65 BSC.		
b	0.22		0.38
c	0.11		0.23
R1	0.13		
R2	0.13		0.3
ø	0°		7°
ø1	0°		
L	0.73		1.03
L1	0.25BASIC		
ccc		0.10	
ddd		0.12	

NOTES:

1. Outline is intended to be footprint compatible with JEDEC MO–112 variation DC–1
2. Dimension 'L' is obtained by measuring, in a horizontal plane, from lead outer end to a perpendicular dropped from where 'Gage Plane' crosses lead inner edge.

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ORIGINATING SITE: SWINDON

ISSUE	1	2	3		
ACN	202480	204413	207309		
DATE	2MAY97	21APR98	19AUG99		
APPRD.					

MITEL SEMICONDUCTOR

Title: Customer Outline Drawing for
144 Lead CQFP (GC)
(28 x 28 x 2.5)mm, Body+3.9mm

Drawing Number
GPD00343

MITEL
SEMICONDUCTOR

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